Fully-VCO-based 0-2 MASH CT $\Delta\Sigma$ ADC

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A fully-voltage-controlled oscillator (VCO)-based continuous-time (CT) Delta-Sigma ($\Delta\Sigma$) analogue-to-digital converter (ADC) is reported, implementing second-order noise shaping without any analogue integrators. Traditional power-hungry front-end analogue integrator is replaced by a highly-digital power-efficient VCO-based integrator, which is constructed by a VCO, a phase detector and a charge pump. The quantisation is executed by a VCO-based quantiser with intrinsic noise shaping. Taking advantage of the mostly-digital and high-order structure, a spurious-free dynamic range of 74 dB and a figure-of-merit of 52 fJ/step over a 40 MHz bandwidth are achieved by a 0.2 multi-stage shaping (MASH) demonstration in 40 nm CMOS.

Introduction: Scaling friendly with the reduced voltage headroom and the increased time resolution, voltage-controlled oscillator (VCO)-based quantisers with first-order noise shaping have recently been exploited in continuous-time (CT) Delta-Sigma ($\Delta\Sigma$) analogue-to-digital converters (ADCs) [1, 2]. The analogue integrator in the high-order $\Delta\Sigma$ loop, however, still difficult to be implemented with CMOS technology scaling and consumes a large amount of power. Different techniques have been developed to replace the power-hungry analogue integrator with other power-efficient blocks. A cascade of two VCO-based quantisers and a digital-to-analogue converter (DAC) is proposed as a second-order $\Delta\Sigma$ ADC [3]. A noise-shaping time-to-digital converter is inserted between a VCO-based quantiser and a feedback DAC to implement second-order shaping without analogue amplifier [4]. Also a pulse-width modulation (PWM)-controlled charge pump is proposed as a substitute of front-end analogue integrator [5]. In [6, 7], VCOs and digital counters are used to build high-order amplifier-free $\Delta\Sigma$ ADCs.

Conceptually, a VCO accumulates the excess phase like an ideal integrator. It is beneficial to shift the analogue integrator to the time domain as well [8]. Another advantage of this kind of VCO-based integrator is that a VCO theoretically has an infinite DC gain, which is power-efficient and independent with the supply voltage. In this Letter, we propose a fully-VCO-based high-order CT $\Delta\Sigma$ ADC with VCO-based integrator and quantiser, including no analogue amplifier. Taking advantage of the mostly-digital structure and high-order noise shaping, moderate accuracy and excellent power efficiency have been achieved.

Fully-VCO-based 0-2 MASH $\Delta\Sigma$ ADC architecture: In Fig. 1, the block diagram and its corresponding clock timing of the fully-VCO-based 0-2 multi-stage shaping (MASH) CT $\Delta\Sigma$ ADC are shown. The key point is that the front-end integrator is implemented by a VCO, a phase detector (PD) and a charge pump (CP), without an analogue amplifier. The first VCO-based-quantiser is adopted to solve the VCO non-linearity issue, as the signal transfer function of the second stage is equal to 1 [2]. An input-feedforward structure is adopted for the second stage to improve the cancellation. As the second stage only processes the quantisation noise of the first stage, its input voltage swing is largely reduced. Therefore, the VCOs in the integrator and the second stage quantiser do not limit the linearity performance.

Fig. 1 Block diagram and corresponding timing of the fully-VCO-based 0-2 MASH $\Delta\Sigma$ ADC

In Fig. 1, all the non-linear harmonics generated in the first quantiser due to the VCO's non-linear behaviour D_{Q1} is cancelled by the gain product K_{DAC}/K_{Q2} and shaped by the VCO-based loop filter $H_{INT(s)} = (K_{VCO,INT}K_{PD}K_{CP})/s$:

$$D_{Q1} \frac{1 - K_{DAC,I} K_{Q2}}{1 + (K_{DAC,G} K_{Q2} K_{VCO,INT} K_{PD} K_{CP}/2)}$$

In behavioural simulations, the proposed ADC achieves 78 dB spurious-free dynamic range (SFDR) within $\pm 10\%$ gain variations of K_{DAC}, K_{Q2} and 81 dB SFDR within $\pm 10\%$ gain variations of $K_{\text{VCO,INT}}$.

ADC building blocks design: The schematic diagram of the VCO-based integrator is presented in Fig. 2, the VCO integrates the input voltage and transfers it to the phase domain, the following PD detects the phase information and then the CP recovers it back to the voltage domain. The N -stage ring oscillator modulates the input with a carrier frequency f_C , which needs to be sufficiently higher than the sampling frequency to avoid spurs folding back into the baseband. In this design, an f_C of 3.5 GHz is achieved with 24 stages and a 145 MHz oscillation frequency f_{VCO} and is filtered out by the subsequent VCO-based quantiser due to its inherent anti-aliasing property. The simulated phase noise is -125 dBc/Hz at 10 MHz offset frequency, which does not limit the ADC performance. The two-state PD illustrated in Fig. 2 is selected instead of an XOR to increase the linear input range. In this design, since the input swing of the second stage is very small, the phase differences always stay in the linear range, and the PD output pulses are duty cycled around 50%. The non-linearity caused by the finite rise/fall time of the PWM signals is greatly reduced [6]. In addition, the barrel shifting property of the multi-level PWM signals offers an implicit dynamic element matching (DEM) of the CP cells.

Fig. 2 Single-ended schematic of the VCO-based integrator

Simulations show that the power-supply sensitivity (13.6%/V) and the temperature sensitivity (2.1%/°C) of the VCOs' gain in the integrator and the quantisers are robust enough for the 12-bit ADC accuracy in this design. In addition, 3-bit binary current-trimming cells are utilised to tune the VCOs' biasing current to accommodate the impact of the process variations. The pseudo-differential 5-bit quantisers in the two stages are clocked at 1.6 GHz. Each single-ended ring VCO contains 15 current-starved delay cells, nominally operating at about 400 MHz. The DACs are implemented using a non-return-to-zero current-steering structure. The implicit DEM obtaining from the VCO-based quantisers greatly relaxes the matching requirement of the DAC cells [1].

Experimental results: The prototype design of the presented fully-VCO-based MASH $\Delta\Sigma$ ADC has been fabricated in 40 nm CMOS technology with a 0.9 V supply voltage. Fig. 3 shows the chip micrograph. The averaged 16,384-point measured power spectral density (PSD) with a 4 MHz -2.5 dBFS $0.4 V_{PP}$ input signal is shown in Fig. 4, a second-order noise shaping is clearly observed, validating the VCO's integration function. The signal-to-noise ratio (SNR)

is about 66.7 dB and the SFDR is 74 dB. The measured SNR/SNDR performance as a function of the input level is shown in Fig. 5. The peak SNR/SNDR of 65.5 dB/62.7 dB is achieved over a 40 MHz signal bandwidth. The total power consumption is 4.6 mW, resulting in a figure-of-merit (FoM) ($\text{power}/2 \times \text{BW} \times 2\text{ENOB}$) of 52 fJ/step. A comparison of this design with the state-of-the-art is shown in Table 1. The presented design achieves an excellent FoM and scales more effectively into newer technology.

Fig. 3 Chip micrograph of the fully-VCO-based 0-2 MASH $\Delta\Sigma$ ADC

Fig. 4 Measured 16,384-point averaged PSD of the ADC output

Fig. 5 Measured ADC SNR/SNDR versus input signal (8 MHz) amplitude

Table 1: Performance comparison to prior time-domain ADCs

Specs	[2]	[7]	JSSC 2015	This work
Architecture	VCO + analogue	VCO + counter	VCO	VCO
Shaping order	2nd	3rd	1st	2nd
Process (nm)	90	65	40	40
Fs (GHz)	0.6	1.0	1.6	1.6
BW (MHz)	10	10	40	40
SNR (dB)	79.1	60.5	60.7	65.5
SNDR (dB)	78	60	59.5	62.7
Power (mW)	16	1.48	2.57	4.6
FoM (fJ/Conv)	125	158.5	42	52

Conclusion: Accumulating the excess phase, a VCO-based integrator is more digitally-oriented and power-efficient than traditional analogue integrators. A high-order CT $\Delta\Sigma$ ADC with fully-VCO-based integrator and quantisers has been proposed and presented, without any analogue amplifier. Benefiting from the second-order noise shaping from the

VCOs and mostly-digital architecture, an SNR of 65.5 dB and a state-of-the-art FoM of 52 fJ/step have been achieved over a 40-MHz signal bandwidth by a 0-2 MASH ADC prototype in 40 nm CMOS. This scaling-friendly ADC architecture is expected to improve the power efficiency further in more advanced CMOS technologies.

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