Dangling bond defects in silicon-passivated strained-Si_{1-x}Ge_x channel layers

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Abstract

Dangling bond defects (DBs) in silicon-passivated (1- or 3-nm thick Si cap) strained-(100)Si_{1-x}Ge_x (x=0.25-0.55) layers at interfaces with 1.8-nm thick HfO₂ gate dielectric are studied by means of Electron Spin Resonance (ESR) spectroscopy. The results suggest a dominant contribution of Si DBs (P_{b0} centers), a considerable fraction of which is located at the interface between the Si substrate crystal and the pseudomorphic Si_{1-x}Ge_x film. The density of Si DBs in the Ge containing samples is significantly lower than at the reference (100)Si/ HfO₂ interface and decreases below the ESR detection limit ($\approx 1 \times 10^{11} \text{cm}^{-2}$) with increasing thickness and Ge concentration in the Si_{1-x}Ge_x layer. However, the beneficial effect of Ge becomes less pronounced when the thickness of the Si cap is reduced to 1 nm or in the case of direct deposition of HfO₂ on top of uncapped Si_{1-x}Ge_x. From these observations we conclude that DBs are eliminated due to in-diffusion of Ge from the Si_{1-x}Ge_x channel into Si, bringing the concentration of Ge to the range in which generation of Si DBs becomes energetically unfavourable, in agreement with previous observations on condensation-grown Si_{1-x}Ge_x layers.

I. Introduction

Interface dangling bonds (DBs) critically affect the operation of metal-insulator-semiconductor (MIS) field-effect transistors (FETs) by providing charge traps that impair electron transport in the near-interface region of the semiconductor. Only upon inactivation of these traps by passivation of the DBs by hydrogen [1] functional MISFETs can be fabricated which is usually realized by annealing in a hydrogen-containing ambient, e. g., in forming gas (90% N₂ + 10% H₂). However, in the course of MISFET operation some of these DBs may become re-activated due to interaction with mobile charge carriers and/or hydrogen species released in the gate stack [2-5] leading to the device degradation. This degradation is particularly pronounced upon bias-temperature stressing (BTS) of silicon MISFETs when a voltage of a given polarity is applied to the transistor gate at an elevated (≥ 100 °C) temperature. The re-activated DBs account for the permanent component of the generated traps which remain active after the stress is terminated [6]. Obviously, the rate of the stress-induced device degradation correlates with the density of the DBs initially present at the semiconductor/insulator interface. This density is primarily determined by two factors: The first one concerns the DBs introduced during semiconductor/insulator interface formation as a result of structural mismatch between two phases and the developed strain [7]. The second one is termed “the processing-induced” degradation and represents generation of additional DBs upon gate stack processing, e.g., upon annealing in an oxygen-deficient ambient [8,9]. The latter factor becomes increasingly important when making the transition from the traditional SiO₂-based gate insulators to high-permittivity (high-k) insulators with metal gate electrodes. This is particularly relevant to the “oxygen scavenging” process [10], which consists in elimination of the SiO₂-like interlayer (IL) under annealing in O-free ambient by an O-absorbing layer introduced in the metal gate electrode. Whereas this treatment appears efficient in terms of the equivalent oxide thickness (EOT)

reduction, however, it degrades the lifetime of the Si MISFETs determined by the BTS-induced instability [10,11]. The degraded reliability is seen as the “showstopper” of EOT reduction in Si-based gate stacks and, as a whole, as the practical limit of the Si MISFET downscaling.

Nevertheless, it is found that addition of germanium to the Si channel layer significantly improves the reliability and the lifetime of high-k MIS transistors, thus enabling the fabrication of technologically-relevant devices in the 14-nm node and beyond it [12-14]. In the current study we have attempted to get a fundamental insight in the atomic nature of this beneficial effect: We analyzed DBs in silicon-passivated (1- or 3-nm thick Si cap) strained-(100)Si_{1-x}Ge_x ([Ge]=x=0.25-0.55) channel layers at interfaces with a 1.8-nm thick HfO₂ gate dielectric by using Electron Spin Resonance (ESR) spectroscopy. The results suggest a dominant contribution of Si DBs (P_{b0} centers) located at the interface between the Si substrate crystal and the Si_{1-x}Ge_x film. The resulting density of Si DBs in the Ge containing channels becomes significantly lower than at the reference (100)Si/ HfO₂ interface and with increasing thickness and Ge goes below the ESR detection limit ($\approx 1 \times 10^{11} \text{cm}^{-2}$). However, the beneficial effect of Ge appears less pronounced when the thickness of the Si cap is reduced to 1 nm or in the case of direct growth of HfO₂ on top of the Si_{1-x}Ge_x channel. These observations suggest that Si DBs are probably eliminated due to diffusion of Ge from the Si_{1-x}Ge_x channel region into silicon. This Ge in-diffusion brings the concentration of Ge in Si to the range in which formation of Si DBs becomes energetically less favourable in – agreement with the earlier reported observations on condensation-grown Si_{1-x}Ge_x films [15].

II. Experimental

Sample preparation for ESR analysis follows as close as possible the production process used in Ref.14, yet without patterning and source/drain implants, in order to obtain defect density estimates relevant to the studied Si and SiGe MISFETs. In short, starting from 300 mm

(100)-oriented p-Si wafers (B-doped, $\approx 10^{15} \text{B/cm}^3$) the devices were formed by epitaxial growth of a reference Si surface channel or, else, of pseudomorphic strained SiGe channel layers (10 nm thick for $[\text{Ge}]=0.25$; 7 nm thick for $[\text{Ge}]=0.45$; 5 or 7 nm thick for $[\text{Ge}]=0.55$) followed by capping by a 1- or 3-nm thick Si layer deposited at 450 °C from SiH_4 . Next, after IMEC cleaning (finished by ozonated water rinse) of the Si surface [16], a gate insulator was grown on top by atomic-layer deposition (ALD) of HfO_2 ($\text{HfCl}_4 + \text{H}_2\text{O}$ at 300 °C, 36 cycles correspond to a physical thickness of ≈ 1.8 nm). Subsequently, after physical vapour deposition of a 5 nm TiN/5 nm Si top electrode, an “oxygen scavenging” spike (1.5 s) annealing was carried out at 1035 °C (for Si and $\text{Si}_{1-x}\text{Ge}_x$ channels with $[\text{Ge}]=0.25$ or 0.45) or at 1000 °C for channels with high ($[\text{Ge}]=0.55$) Ge content which brings the EOT down to $\approx 0.6\text{-}0.7$ nm. Finally, all the samples were capped with a p^+ -doped polycrystalline Si electrode (50 nm thick) and a top 200 nm Ni silicide layer. In this way the fab-grade processing flow is reproduced on the large-area samples enabling device-relevant defect characterization. The process flow and the resulting sample structure are schematically illustrated in Fig. 1 while the strained $\text{Si}_{1-x}\text{Ge}_x$ channel composition, Si passivation cap thickness, top insulator film and the applied anneal temperature (T) are listed in Table 1.

Samples for ESR analysis were first thinned down to ≈ 100 μm remaining thickness by etching off Si from the backside of the wafer. Next, the metallic gate stack layers which preclude meaningful ESR measurements were removed by using exclusively the wet etching route to avoid semiconductor/insulator interface damage as indicated in Fig. 1. The absence of damage to the few-nm thick HfO_2 layer and the semiconductor/insulator interface of this critical etching step was assessed by comparing capacitance-voltage (CV) curves measured on the capacitors with patterned original TiN/Si/Poly-Si/NiSi electrodes to the “replacement gate” capacitors fabricated by thermoresistive evaporation of chemically inert (Au) metal electrodes on top of the 1.8-nm thick HfO_2 insulator exposed after etching off the original multilayer metal gate. Since the

DBs in the Si/ Si_{1-x}Ge_x channel region were exposed to hydrogen during the gate stack processing steps, they need to be de-passivated in order to allow detection by ESR. This was achieved by exposing the sample surface to 10-eV photons emitted by a resonant Kr discharge lamp through MgF₂ window (photon flux $\approx 10^{15} \text{cm}^{-2} \text{s}^{-1}$) for 600 s.

Table 1. Sample structure and the density of Si DB defects detected by ESR as P_{b0} centers.

Sample	Channel	Si capping	Insulator	Anneal T(°C)	[P _{b0}] (10 ¹² cm ⁻²)
S01	Si	none	1.8 nm ALD HfO ₂	1035	3.8 ± 0.5
S02	10 nm Si _{0.75} Ge _{0.25}	none	1.8 nm ALD HfO ₂	1035	0.9 ± 0.1
S03	7 nm Si _{0.55} Ge _{0.45}	1 nm Si	1.8 nm ALD HfO ₂	1035	< 0.08*
S04	5 nm Si _{0.45} Ge _{0.55}	1 nm Si	1.8 nm ALD HfO ₂	1000	0.9 ± 0.1
S05	5 nm Si _{0.45} Ge _{0.55}	1 nm Si	5 nm PECVD SiO ₂	1000	0.8 ± 0.1
S06	5 nm Si _{0.45} Ge _{0.55}	3 nm Si	1.8 nm ALD HfO ₂	1000	< 0.08*
S07	7 nm Si _{0.45} Ge _{0.55}	1 nm Si	1.8 nm ALD HfO ₂	1000	1.8 ± 0.5
S08	7 nm Si _{0.45} Ge _{0.55}	3 nm Si	1.8 nm ALD HfO ₂	1000	< 0.08*

*- estimated limit of experimental sensitivity.

Figure 1. Schematics of the fabrication process flow and the structure of the studied samples. The indicated top metallization stack was removed prior to the ESR analysis.

ESR analysis was carried out on stacks of 15-20 sample slices using a K-band (≈ 20.5 GHz) spectrometer driven in the adiabatic slow passage mode. First absorption-derivative ESR spectra, $dP_{\mu r}/dB$ (where $P_{\mu r}$ is the reflected microwave power) were measured at 4.3 K for various orientations of the applied magnetic field $\mathbf{B}$, at angle φ_B with the [100] sample normal, in the $(0\bar{1}1)$ Si plane [17]. The amplitude B_m of the applied harmonic magnetic field modulation (~ 100 kHz) and incident microwave power P_{μ} were carefully limited so as to avoid any noticeable signal distortion. The densities of ESR-active centers were determined by making use of a co-mounted calibrated Si:P marker sample [$g(4.2\text{ K})=1.99869\pm 0.00002$; spin $S=1/2$) through double numerical

integration of the, generally computer-simulated, $dP_{\mu r}/dB$ spectra. The obtained absolute and relative accuracies are estimated at $\sim 20\%$ and 10% , respectively. Reliable assignment and discrimination of overlapping signals is obtained through making full use of field angular dependent measurements, that is, exploiting the difference between anisotropic (e.g., P_{b0} center) and isotropic signals (e.g., D-line pertaining to the DBs in the disordered silicon regions).

III. Results and Discussion

The impact of the negative BTS on the interface trap density is well reflected in the interface trap density energy profiles shown in Fig. 2 measured on reference Si/HfO₂/Au capacitors before (black symbols) and after (red symbols) subjection to a 3 h BTS at 100 °C under application of -2.5 Volt bias to the top metal electrode. The interface trap density was determined using the ac conductance method but only a limited range of trap energies close to Si midgap was probed because of excessive tunnelling current through the 1.8-nm thin HfO₂ insulator at higher gate bias values. Nevertheless, one can recognise the rapid increase in trap density starting from ~ 100 meV below Si midgap –a feature known from the literature [18-20] as corresponding to energy distribution of interface traps associated with DBs of the interfacial Si atoms, which have previously been correlated with ESR active P_{b0} centres at the (100)Si/SiO₂ interface; The contribution of the P_{b1} centers to the gap states at this interface was shown to be undetectable [21]. Unfortunately, limited energy range of these ac conductance measurements makes reliable quantification of interface DBs impossible. Furthermore, the ac conductance method cannot be applied to the structures with p-type Si_{1-x}Ge_x channel because the ac response in this case is dominated by the Si_{1-x}Ge_x quantum well [22] formed because of the energy offset between the valence bands in Si and Si_{1-x}Ge_x [23]. As a result, we will address only the ESR results in the further discussion.

Figure 2. Interface trap energy distributions as measured by using the ac conductance method on the reference (100)Si/HfO₂(1.8 nm)/Au capacitors (sample S01) prior (black ■, ◆ symbols) and after (red ▲, ◆ symbols) BTS at the indicated conditions. Measurement results for two different capacitors are shown for reasons of comparison.

Examples of the absorption-derivative ESR spectra obtained from the optically-depassivated reference Si/HfO₂ sample S01 and from sample S04 with 5-nm thick Ge-rich Si_{0.45}Ge_{0.55} channel capped with a 1-nm thick Si overlayer are compared in Fig. 3. A drastic lowering of the Si DB signal (P_{b0}) intensity in the case of the Ge-doped channel is obvious. To study this effect in more detail, we analyzed the behaviour of the P_{b0} center densities at channel interface with HfO₂ as a function of the channel thickness and Ge content as well of the Si capping presence and its thickness.

Figure 3. K-band absorption-derivative ESR spectra observed for magnetic field $\mathbf{B}$ oriented along the normal to the sample surface $\mathbf{n}$ using $P_\mu = 16$ nW and $B_m = 0.85$ G, on the reference (100)Si/HfO₂ sample (S01) and on the (100)Si/Si_{0.45}Ge_{0.55}(5 nm)/Si (1 nm)/HfO₂ sample (S04) after photo-dissociation of the passivating hydrogen atoms.

The results of the ESR-active P_{b0} centers density measurements, summarized in Table 1, are illustrated in Fig. 4 showing the density as a function of the *total* areal density of Ge atoms in the channel layer (target values). Besides the general trend of the DB density lowering upon introduction of Ge, there are several additional noteworthy observations. First, the “omission” of the entire Si cap in sample S02 does not lead to the elimination of the Si DBs (cf. red arrow in Fig. 4) indicating that a considerable density of Si DBs is located the interface between the Si substrate crystal and the epitaxial Si_{0.75}Ge_{0.25} channel. The P_{b0} density in this case appears to be

close to that in the (100)Si/Si_{0.45}Ge_{0.55}(5 nm)/Si (1 nm)/HfO₂ sample (S04) which contains approximately the same amount of Ge. Second, the samples with a 3-nm thick Si cap (S06, S08), expected to behave similarly as the bulk Si reference sample S01, show no presence of P_{b0}-centers within the sensitivity limit of $\approx 8 \times 10^{10} \text{ cm}^{-2}$ (cf. green circle in Fig. 4). Remarkably, in the sample S07 with a 7- nm thick Si_{0.45}Ge_{0.55} channel and a 1 nm Si cap, the P_{b0} density increases considerably as compared to its counterpart S04 with only a 5-nm thick Si_{0.45}Ge_{0.55} layer. The latter may be due to relaxation of the thicker Ge-rich channel upon high-temperature anneal leading to the generation of mismatch-induced DBs at the interface between Si_{0.45}Ge_{0.55} and the Si substrate.

Figure 4. Areal density of Si DBs detected by ESR as P_{b0} centers as a function of total (target) Ge atoms areal density in the channel region.

In looking for a rational explanation for the observed density reduction, or even elimination of Si DBs, in the studied Si/Si_{1-x}Ge_x/Si channel structures, it may be useful to recall the results of previous ESR analysis of SiO₂/Si_{1-x}Ge_x/SiO₂ structures synthesized using the Ge condensation technique [15,24]. Despite most of the attention devoted there was to the investigation of the Ge-P_{b1} centre, it has not been left unnoticed that in a certain range of Ge concentration ($\approx 0.23 < [\text{Ge}] < \approx 0.54$) *neither Ge nor Si DBs* are observable in the ESR spectra. This leads us to the hypothesis that, as opposed to the case of pure Si, for Si_{1-x}Ge_x layers with Ge concentration in the indicated range, a kind of interface strain/mismatch relief mechanism prevents “accumulation” of interface energy required for the DB generation. This mechanism pertains to the Si_{1-x}Ge_x itself and cannot be associated with the formation of Ge oxides as these are unstable under conditions of high-temperature (1000 or 1035 °C) annealing used in the present work.

Therefore, it is possible to propose that out-diffusion of Ge from the Si_{1-x}Ge_x channel towards the Si substrate and the Si capping layer will allow for the mismatch-induced strain relaxation without formation of DBs as long as the Ge concentration in Si remains high enough, i.e., above $x=0.2$ or similar to this value. This Ge out-diffusion process is well documented in the literature [25-27] and under usual processing thermal budgets, Ge in-diffusion depth ranges from several nm to few tens of nm. This mechanism allows us to explain the major experimental observations made in the present study if assuming that the oxide insulator represents a *sink* of the Ge atoms diffusing in from the Si_{1-x}Ge_x channel region due to the high Ge solubility in the oxide. The absence of the Si capping (otherwise acting as a diffusion barrier) will lead to a lower amount of Ge diffusing into the Si substrate while a reduced “efficiency” of the 1-nm thick Si capping in terms of DB elimination might be due to the porosity of the cap as revealed in independent electron microscopy studies [28]. Finally, relaxation of the channel region in sample

S07 may also cause the Si cap rupture leading to a higher DB density than in the case of an unrelaxed (thinner) $\text{Si}_{1-x}\text{Ge}_x$ layer.

Worth of mentioning here also is the effect of residual strain on the Ge diffusivity upon annealing [29,30], which is expected to increase with increasing Ge concentration as well as with growing SiGe film thickness [31,32]. The strain distribution is also expected to be sensitive to the Si cap thickness which makes detailed analysis of the strain distribution rather complicated. Nevertheless, taken together, the experimental observations made in the present study and the results of previous works allow us to designate the process of Ge alloying with Si as the technologically feasible method allowing for reduction of interface DB density and improving MISFET reliability.

VI. Conclusions

To summarize, the presented results of ESR analysis on Si and $\text{Si}_{1-x}\text{Ge}_x$ MIS structures manufactured along the fab-level MISFET-like process flow, with incorporation of an ultra-thin (1.8 nm) HfO_2 insulator and oxygen scavenging indicate that incorporation of Ge leads to significant reduction of the electrically detrimental interfacial silicon DB defects detected as P_{b0} centers by ESR. The proposed explanation of this beneficial effect is based on strain relaxation in the Ge doped Si regions given way by out-diffusion of Ge from the $\text{Si}_{1-x}\text{Ge}_x$ channel layer. This beneficial effect of Ge allows for improved reliability of the devices and projects the possibility of further EOT scaling using the oxygen scavenging approach without impairing the interface quality.

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