A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS

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Abstract—A fault tolerant, radiation hardened Clock and Data Recovery (CDR) architecture is presented for high-energy physics and space applications. The CDR employs a novel soft-error tolerant Voltage Controlled Oscillator (VCO) and includes a high-speed feed-forward path to stabilize the CDR to compensate for an additional pole in the VCO to harden it against ionizing particles. The CDR has a data rate of 2.56 Gbps and uses In-Phase/Quadrature (IQ) clocks in combination with a frequency detector (FD) to increase the pull-in range. The circuit was designed in a 65 nm CMOS technology and has a core power consumption of only 34 mW.

Index Terms—CDR, Single-Event Upsets, Radiation hardening, jitter, phase noise, clock recovery.

I. INTRODUCTION

HIGH speed serial communication links are mandatory in nearly all high-performance systems. However, several applications require ultra-reliable communication links which may operate in relatively harsh environments. One major contribution to soft errors is ionizing radiation that may originate from cosmic rays, natural effects or artificially created high-energy particles. The latter specifically applies to particle accelerators and detectors such as the Large Hadron Collider (LHC) at CERN where high levels of ionizing particles are present. In other environments such as space applications (e.g. SpaceFibre links) or even reliable terrestrial electronics such as automotive circuits, soft errors became more important as technology nodes have scaled down. Ionizing radiation can introduce Single-Event Effects when energetic particles interact with a silicon substrate [1]. This creates transients in analog and digital circuits and results in soft-errors in digital logic structures. In serial communication circuits, encoding is used to reduce bit error rates due to errors related to transmission. This can significantly reduce the bit error rate due to thermal noise contributions or single soft-error upsets in an encoded frame. However, the timing generator of a serializer/deserializer (SERDES) has been known to be prone to single-event upsets since it contains significant amounts of analog blocks and can result in loss of lock [2]. While digital circuitry can be hardened using redundancy, analog blocks

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Fig. 1. a) Conventional VCO tuning. b) Radiation hardened VCO tuning circuit. [5]

remain sensitive. In general the Voltage Controlled Oscillator is the most sensitive circuit [3]. In [4], a comparison was made between ring-oscillators and integrated LC-tank oscillators. While ring-oscillators severely suffer from degradation due to total ionizing dose effects (TID), LC-tanks do not since the frequency depends only on the resonance between passive components. However, a classical LC-tank oscillator has a significantly larger cross section compared to ring oscillators. With proper radiation hardening techniques, LC-tanks can be made radiation hardened by design [5].

In LC-integrated oscillators, the varactors' junctions contribute most to single-event transients since it can introduce voltage jumps at the tuning node leading to frequency errors [5]. In Fig. 1a, a traditional LC oscillator is shown that is sensitive to radiation at the tuning node junction. The varactor is implemented as a moscap (metal-oxide-semiconductor capacitor) in an n-well. The n-well to p-substrate junction can collect a significant amount of charge. By rearranging the varactor tuning topology (Fig. 1b), the sensitive junctions of the n-well moscaps in the latter circuit are shorted at the ground terminal and cannot collect charge anymore. Radiation experiments with heavy-ions showed no upsets or latch-up up to an LET of 62 MeV.cm²/mg. Therefore, fully radiation hardened CDRs with triplicated digital logic can be designed with this approach [5]. During these measurements, ion strikes

Fig. 2. Architecture of the CDR circuit.

on the VCO showed no measurable frequency deviations. This can be explained since there is no charge collection junction at the frequency tuning node of the VCO, resulting in no frequency deviation. This circuit has also been verified with protons and laser experiments and showed no sensitive spots.

This paper is organized as follows: Section II introduces the CDR architecture. In Section III, the implementation details are discussed. In Section IV, the results are discussed and Section V shows a conclusion.

II. CIRCUIT ARCHITECTURE

A. CDR topology

The CDR architecture is based on a non-linear bang-bang phase detector Phase-Locked Loop (PLL) that provides early-late corrections to the loop through a proportional and integral path as is shown in Fig. 2. An additional frequency detector is added to extend the pull-in range of the CDR during acquisition. This Frequency Detector (FD) is based on a 4-quadrant sampling method [6][7] and is extended with a pulse

time-amplifier to limit the required charge-pump current of the FD. The VCO runs at 5.12 GHz to create I and Q clocks at 2.56 GHz for the CDR clock recovery. The proportional and integral path of the CDR is split to reduce the capacitor area of the loop filter while respecting the noise requirements of the loop resistor [8]. The proportional path corrects the CDR instantaneously while the integral path tracks slowly varying offsets. In [9], a similar charge-pump and loop filter was used previously which showed no transients during heavy-ion experiments. Due to the low bandwidth of the VCO, fast transient on the proportional path will marginally propagate to the output.

The oscillator that was discussed in Section I has shown extensive resistance against single-event effects since the varactor is AC coupled to the oscillator's tank and is unable to collect charges. However, the biasing resistor R_b introduces an additional pole in the loop with a cut-off frequency of

$$f_{-3dB} = \frac{1}{2\pi R_b(C_v + C_c)}. \quad (1)$$

In this design, the oscillator had a tuning varactor of nominally 1.5 pF and a coupling capacitor of 10 pF with a bias resistance of 600 Ω . Therefore, the parasitic pole has a cut-off frequency of 23 MHz which limits the tuning bandwidth of the VCO. In linear PLL clock generators, this pole is generally not an issue since the gain-bandwidth product of a PLL loop is typically well below this frequency such that it only marginally affects the stability of the loop. However, in CDRs, the required loop corrections are orders of magnitude faster compared to linear PLLs and the stability of the loop is degraded due to this additional pole. The reason for this can be found in the non-linear limit cycle of a bang-bang CDR. The phase detector only detects early or late pulses. To meet the required standards such as Jitter Tolerance (JTOL), large

Fig. 3. Phase overshoot due to a limited VCO tuning bandwidth.

Fig. 4. Phase domain model of feed-forward compensation.

proportional gains are required. However, to limit the limit-cycle jitter, corrections to the VCO need to be adequately fast. When the additional slow pole is introduced in the CDR, the limit cycle jitter may exceed the requirements significantly. An example of this issue is shown in Fig. 3. Here, the phase detector provides a correction voltage to the VCO. However, the low pass filtering of the VCO tuning stage decays slowly such that the phase error overshoots resulting in large limit cycle jitter. To overcome this issue, a high-speed feed forward path is added to stabilize the CDR in locked operation.

B. Feed Forward Compensation

The core of this path is an additional charge-pump which acts as an integrator and controls a voltage controlled delay cell (VCDC) at the data input and compensates for fast adjustments that would be required by the proportional path but are filtered by the VCO. A VCO acts as an integrator and integrates the phase detector's control signals to phase. The fast feed-forward compensation performs this integration internally and adds an additional delay using a voltage-controlled delay cell to convert the integrated voltage to phase. To overcome saturation, the integrator is made lossy with an average voltage of $V_{dd}/2$. A phase domain model of this approach is shown in Fig. 4. The corner frequency of the lossy integrator is chosen such that it aligns with the cut-off frequency of the VCO. Therefore, below the corner frequency, the VCO can process the CDR's proportional path corrections. Above, the feed-forward path will correct the CDR by adjusting the VCDC's delay, controlled by the integrated voltage that emulates the VCO integration. From a loop perspective, the pole is canceled by the feed-forward path which operates complementarily. Therefore, the limit cycle is highly stabilized. In Fig. 4, the correction path interacts with the VCO's output phase. However, an inverse correction can be applied to the CDR's input phase which is practically beneficial and used in this design. Additionally, the output phase of the VCO has reduced high-frequency spurs originating from the bang-bang limit cycle which are now intrinsically filtered by the VCO.

III. IMPLEMENTATION

The Alexander PD and divide-by-2 prescaler were implemented with Current-Mode-Logic (CML) logic. For the phase detector, this was mainly done to prevent hysteresis by using differential signaling. The prescaler uses redundancy to prevent SEUs in the divider. The phase detector does not

Fig. 5. Voltage-controlled delay cell implementation.

Fig. 6. Delay curve with differential control voltage input.

include triplication to save power since errors only result in a temporal phase deviation during one bit period which is filtered by the loop. The voltage-controlled delay cell in the feed-forward path is implemented differentially and has differential tuning voltages (Fig. 2 shows a simplified single-ended tuning path). The charge-pump in Fig. 2 is therefore duplicated to allow a complementary operation. The circuit of the delay cell is shown in Fig. 5. The cell has a constant current bias and its delay is controlled through Tune+ and Tune-. The circuit's delay is increased by adding a cross coupled NMOS pair to the output which reduces the transconductance during switching and counteracts on the input pair's strength. If Tune+ increases with respect to Tune-, this effect increases and the delay increases. The feedback resistors R_f are added to linearize the tuning characteristic. Since the tail current is constant, the swing of the cell is constant as well. Fig. 6 shows a simulation of the delay. The nominal differential charge-pump voltage bias is 0 V (0.6 V common mode) which results in a 40 ps/V gain (K_{vcdc}).

IV. RESULTS

The CDR lock acquisition is a combination of the frequency detector lock, phase detector pull-in and finally the feed-forward correction that acquires lock. The differential control voltages of the feed-forward voltage controlled delay cell are shown in Fig. 7. During the initial stage, the FD and

Fig. 7. Feed-forward delay cell control voltage during lock.

Fig. 8. Phase noise at the 5.12 GHz output with and without correction.

PD are pulling the VCO to the correct frequency which is a frequency acquisition. During frequency locking or coarse phase locking, the correction path is undetermined but does not impact the lock process since its range is limited to 20 ps. When the CDR is close to its final phase alignment, the feed-forward can converge. Due to the lossy integrator, the correction loop always settles to the same delay, independently of the frequency since the mean tuning voltage is constant.

The phase noise of the CDR in lock is shown in Fig. 8. It shows the noise at the VCO output with feed-forward correction enabled and disabled. When it is disabled, an unstable peak is observed which indicates that the limit cycle of the CDR is unstable and leads to a large limit cycle jitter. This is removed by enabling the feed-forward compensation that emulates fast proportional corrections of the VCO in its parallel path. The total integrated jitter (at the output of the VCO) is only 300 fs. In contrast, a >3 ps limit cycle jitter was observed without compensation which indicates a tenfold improvement.

Finally, the jitter tolerance of the CDR is shown in Fig. 9. The OC-48 spec mask is shown as a reference. The feed-forward compensation does not impact the JTOL. This is mainly since the cross-over frequency of the feed-forward compensation is well above the JTOL corner where the CDR does not track input phase changes anymore.

The loop dynamics of the CDR are highly programmable. Both the charge-pump current and loop resistor resistance can be digitally configured to compensate for deterministic process variations of the MOS, resistors and VCO gain. The temperature effects of the loop are explained in detail in [9].

V. CONCLUSION

In this paper, a radiation hardened Clock Data Recovery was presented with a 2.56 Gbps data rate in a 65 nm CMOS technology. The CDR includes a radiation hardened VCO with AC coupled varactors to prevent single-event effects in the oscillator with a tolerance to an LET of 62 MeV.cm²/mg. This structure introduces a low frequency pole that destabilizes the CDR loop. This is overcome by adding a high-speed feed-forward path that covers the high-frequency proportional corrections of the VCO by adding a voltage-controlled delay

Fig. 9. Jitter Tolerance (JTOL) of the CDR.

cell to the CDR. This complementary path ensures that the loop is stable and ensures fast corrections to the CDR. The CDR meets the OC-48 JTOL specifications and has an output jitter of only 300 fs with a 34 mW power consumption.

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