An SRAM Based Radiation Monitor with Dynamic Voltage Control in 0.18 μm CMOS technology

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Abstract—This paper presents a novel radiation monitor which is based on a custom SRAM (Static Random Access Memory) ASIC. Its sensitivity is adjustable through its core supply voltage and the radiation monitoring is based on the upset rate that is measured during a measurement-interval in the memory. The sensor has different supply voltages for the SRAM core and the interface logic to prevent incorrect digital signals during the measurement cycle. The memory was processed in a 0.18 μm CMOS technology and was tested with heavy ions with an LET from 1.8 - 60 $\text{MeV}\cdot\text{cm}^2/\text{mg}$, 24 GeV protons and a mixed radiation field. The memory cells were also verified with a Two-Photon Absorption (TPA) Laser. Furthermore, an analysis was made on Single-Event Upsets and multi-bit upsets.

Index Terms—Radiation sensors, Single-Event Upsets (SEUs), SRAM, Memory, Heavy Ion, Two-Photon Laser, CMOS

I. INTRODUCTION

RADIATION monitoring is essential in nuclear, space and high-energy physics experimental areas. Many methods exist to measure radiation levels and each of them is optimized for certain needs, depending on its application. The most famous type of radiation measurements is the dosimetry for people that operate in an active area. Generally, such dose rates are extremely low and sensitive detectors are used to measure the dose accurately. In such cases, pre-calibration is important since the actual dose is important. In other applications, the measurement of the energy spectrum is essential. Such circuits typically rely on semiconductor detectors with sensitive analog front-ends and a pulse-shaper to measure the energy that is deposited by the particles. The granularity of the sensor can range from 1 single detector up to 256x256 pixels or even more [1]. The disadvantage is the complexity and the analog components of the system that may be prone to degradation [2] and process variations. In other cases, the instantaneous flux is correlated with electronic faults as well [3] to enhance fault models in space systems. MOSFETS and more specific RADFETS [4] can be used to determine the radiation dose by measuring the degradation of the devices and can be possible candidates for a monolithic integration of the sensor with the readout interface and processing elements. Furthermore, different approaches are used to measure energetic particles but typically, they rely on the conversion of the radiation energy to another form which can be measured with electronic components such as scintillators and gaseous detectors [5] which tend to be very bulky compared to semiconductor detectors.

The drawback of all these types of detectors is that they require different technologies that need to be combined and

typically require highly analog and sensitive interfaces. In the past, a few successful experiments were performed with SRAM memories as a radiation monitoring device [6]. For example, the Radmon devices at CERN are used to monitor the radiation in the accelerator complex [7][8][9][10]. The upset rate was monitored to estimate the fluence of the radiation. The RadMon system was based on a commercial 0.4 μm SRAM [7] and a new candidate for RadMon is based on 90 nm SRAM devices [11][12]. In [7], experiments were performed to test the response of a Toshiba SRAM under different supply voltages against thermal neutrons and high energy hadrons. Several tests in the past years have been carried out in order to characterize those memories together with FLUKA simulations. However, such devices using old technologies may become obsolete. For more advanced SRAM chips, MBUs (multi-bits upset) are likely to happen since SRAM cells are much smaller. In [12], different types of MBUs and SEU bursts were studied on a 90 nm SRAM, and provide solutions to correct different types of MBUs. However, more advanced commercial SRAM memories tend to have an enhanced resistance against soft errors, making them less useful in radiation monitoring applications due to error correction techniques. With such MBU correction algorithm, this 90 nm SRAM [11] was calibrated under a mixed radiation environment at the LHC and showed that the cross section of thermal neutrons decreases compared to 0.4 μm SRAMs, used in RadMon. However, the reducing junction capacitances in advanced technologies are favorable for radiation detection applications [13]. A similar MBU analysis was done in [14]. Another concern is that the cross section of the devices may change during irradiation due to Total Ionizing Dose Effects (TID). However, in [15] and [11], practical experiments have shown that this is not the case on 90 nm CMOS SRAMs.

In this work, an SRAM memory was designed with an enhanced sensitivity to ionizing radiation. The effect of the supply voltage to the sensitivity to Single- and Multiple Event Upsets was studied in order to increase the sensitivity of the devices. Commercial SRAM memories have a shared supply voltage between the readout interface and the memory core. However, in this chip, the supply voltage of the SRAM cells and readout interface is completely separated. In this way, the core voltage of the SRAM devices can be adjusted without altering the core voltage of the address decoders and read-write interface. Even when the supply voltage is significantly reduced, the chip is not reset which would be the case in many commercial devices.

This paper consists of the following parts. Section II

Fig. 1: Architecture of the SRAM memory.

describes the architecture of the SRAM memory and the supply reduction cycle. In Section III the measurements of the memory in different environments is discussed. In section IV an application of the sensor is shown to measure the profile of a proton beam and section V contains the TPA laser experiments.

II. SRAM ARCHITECTURE

A. Memory organization

The SRAM memory is based on an array of 160x128 individual SRAM blocks. This size was chosen to fit the memory in an experimental silicon prototype and an architectural schematic is shown in Fig. 1. Vertically, each of the 160 rows can be selected by the row decoder which decodes the most significant bits (MSBs) of the address. Each row consists of 128 cells which are distributed among 16 bits. This leaves 8 columns per bit. The column decoder selects the correct column in each of the 16 bits based on the least significant bits (LSBs) in the address. A multiplexer connects the correct column to the read/write logic. The total area of the SRAM core was $700 \mu\text{m} \times 700 \mu\text{m}$.

In this design, the address/row decoders and the serial interface were triplicated in order to prevent false readouts due to upsets in this logic.

The memory can thus be accessed with 16 bits per read/write cycle. To facilitate the experiments, a serial interface is used to communicate with the chip.

The chip has 3 different power domains. One 3.3 V supply for the IO cells, one fixed 1.8 V for the core logic (decoders and read/write logic such as the sense amplifiers) and an adjustable 0 V-1.8 V supply for the SRAM core cells. It is essential to power the address logic and interface logic at a fixed voltage to prevent short and leakage currents in the digital standard cells.

Fig. 2: SRAM cell schematic

B. SRAM cells

The sensitivity of the sensor depends on the SRAM cells in the array. In this design, the SRAM cells are based on a 6T circuit as is shown in Fig. 2. The transistors are chosen to be minimum sized to achieve a good sensitivity since the parasitic capacitances are minimized. Some non-minimum cells may be more sensitive than minimum ones, like for instance one of the cells described in [16], (which is a cell with non-standard transistor sizes). Despite that, this work focuses on the study of the cell sensitivity in terms of supply voltage and only standard minimum cells are considered. The physical layout of the SRAM cell is shown in Fig. 3.

It is well-known [17] that cross coupled SRAM cells have a certain noise margin. The noise margin is the voltage that is required to flip a bit. In order for an ionizing particle to upset a memory cell, it has to overcome this noise margin. However, when the supply voltage is reduced, the noise margin significantly reduces. Fig. 4 shows the noise margin of a cell for high and low supply voltages. The noise margin is the square that fits within the area confined by the two transfer characteristics of the inverters. It becomes clear that this area shrinks proportionally with the supply voltage. This is an advantage for radiation sensing since the memory becomes more sensitive to incoming particles at such low voltages.

As discussed previously, smaller have reduced critical charge due to reducing parasitic capacitances. Therefore, it is expected that advanced nodes will show an increased sensi-

Fig. 3: SRAM cell layout

Fig. 4: SRAM cell noise margin with reduced supply voltage

Fig. 5: Cycle of the supply voltage for successive measurements.

tivity to injected charges [18]. However, smaller geometries will also collect less charge in deep sub- μm technologies. Therefore, careful TCAD simulations are required to study this competing mechanism. However, these simulations are time- and resource-consuming but several SRAM blocks can be simulated simultaneously [19].

C. Supply Cycle

In order to measure radiation quantities with the sensor, a predetermined cycle was used. An example is shown in Fig. 5. Initially, the full content of the memory is read as a reference. Usually, it is not required to write data to the cells since only the difference (XOR) is interesting. The read operation (and potentially writing) of the memory is always done at the full supply voltage in order to maximize the noise margins and to prevent destructive read operations. After the memory is read, the SRAM core is powered down to a lower supply voltage where it is more sensitive to upsets. After a certain measurement time and before reading the content of the device, the supply voltage is restored to its maximum value and the memory is read again. This process can be repeated to periodically read the memory.

In order to maximize the efficiency of the sensor, the measurement time should be significantly longer than the

readout time. Firstly, during reading, it may happen that an upset occurs in the sense amplifiers which contributes to false positives. Secondly if any bits are upset during that period, it may not correspond to the supply voltage that was previously set.

However, the measurement time cannot be set infinitely long. The longer the sensor is in its measurement stage, the higher the probability that a single bit flips twice. This would mask the event and would no longer lead to significant data. Statistically, if the memory is placed infinitely long in its measurement mode, half of the cells will be a logic one. Therefore, in our experiments, we have limited the measurement time in order to keep the upset rate of the memory below 5 % of the full array.

The Poisson distribution can be used to calculate the probability that a single bit is upset twice in a measurement interval. This probability is

$$P(k = 2, T) = \frac{(\lambda T)^k}{k!} e^{-\lambda T} \quad (1)$$

in which λ is the expected number of upsets per second and T is the aperture time of the sensor. More specifically

$$\lambda = F \cdot \phi_{bit} \quad (2)$$

in which F is the flux [$1/\text{cm}^2 \cdot \text{s}$] and ϕ_{bit} the cross section of one bit cell. For example, if a $10^5/\text{cm}^2 \cdot \text{s}$ heavy ion flux is used with a $1.46 \cdot 10^{-8} \text{cm}^2$ cross section per bit (see heavy ion tests in section III), the expected $\lambda = 0.0015/\text{s}$. If the aperture time is chosen to be 30s, the probability of a double bit upset is only 0.1 %. This aperture time is a reasonable compromise to reduce the overhead time to read the memory in the measurement setup (2 seconds in our case which is limited by our microprocessor setup).

This probability can also be seen as a trade off between the sensor interface data rate and the accuracy of the measurement. If the sensor readout time is neglected, the data rate of the memory is inversely proportional to the aperture time and thus the probability of double bit flips. Longer aperture times result in less data rate (and power) at the cost of higher double upset probabilities. In a practical case, this has to be evaluated with the expected flux and cross section.

III. EXPERIMENTAL RESULTS

A. Measurement setup

The SRAM circuit was manufactured in a $0.18 \mu\text{m}$ CMOS technology and packaged in a ceramic package. The setup is composed of 2 boards, one contains the SRAM sensor and CML drivers/receivers for the serial link and the second is a processing board with a microprocessor, power management and CML IO. CML differential signaling was chosen for the serial interface to prevent signal integrity issues since the cable lengths that are required in the IRRAD and CHARM facilities have a length of 30 m. The microprocessor and power management circuits are located outside the irradiation area.

Fig. 6: a-b) Low LET (1.8 MeV.cm²/mg) cross section. c-d) High LET (60 MeV.cm²/mg) cross section.

Fig. 7: Cross section for various supply voltages.

Fig. 8: Ratio of multi-bit upsets to single-bit upsets for small supply voltages.

B. Heavy-Ion Experiments

Heavy ion experiments were done at the RADEF facility in the University of Jyväskylä, Finland. The measurement time of one readout cycle was chosen to be 20 s and the flux was set so that the total upset count in the memory during one cycle was 5 % (1000 bits) to reduce the probability of double upsets. For each ion, different supply voltages were measured. For each supply voltage, 30 cycles of 20 s were performed.

The measured cross section across different supply voltages is shown in Fig. 6 for 1.8 and 60 MeV.cm²/mg respectively on a linear and logarithmic scale. From these measurements,

it is clear that the supply voltage has a significant effect on the sensitivity of the sensor. With additional post-processing, single-bit, double-bit and multi-bit upsets (Neighboring upsets) were analyzed. Particles with low LETs mainly induce single bits while the double- and multi-bit upset rate increases at high LETs, especially at small supply voltages. This is due to the larger charge deposition and range of the particles to neighboring cells. From the logarithmic plots, it is clear that the multi-bit upsets have a stronger dependency on the supply voltage than the single-bit upsets.

Fig. 9: Cross section, measured during high intensity proton tests.

The cross section for different LETs and various supply voltages is shown in Fig. 7. As expected, the cross section increases when the supply voltage is reduced.

The ratio of multi-bit upsets (2-bit + multi bit) to single-bit upsets in a measurement cycle reveals an interesting dependency on the LET, especially at small supply voltages. This ratio is shown in Fig. 8 for different LETs. The measurements show a linear dependency on the LET and the MBU-to-SEU ratio is of course independent on the flux on the sensor. Such an experiment can be useful to estimate the energy deposition of the particles in the sensor. In that case, the sensor output is not calculated as the number of upsets (which is proportional to the flux) but it is calculated as the ratio between two counts. However, this technique requires a processing circuit on the readout electronics or locally on the SRAM chip.

C. High-Energy Protons

The sensor was tested in the high-energy proton beam at the IRRAD facility at Cern. The 24 GeV PS (Proton Synchrotron) protons have a beam intensity of $1.2 \cdot 10^{11}$ particles/spill. This results in an extremely high upset rate per spill as is shown in Fig. 9. The upset rate can be reduced with different supply voltages but in this case, the multi-bit upset rate cannot be used since the bits cannot be clustered due to the high upset rate. However, the chip can be used to estimate the beam intensity with relevant calibration or by using a relative measurement as is discussed in the next section. Simultaneously, the proton beam is focused on a copper target at the CHARM facility [20], which is down the beam line of the IRRAD facility. This generates a mixed field of particles such as high-energy hadrons. The cross section, measured over several days is shown in Fig. 10 which shows the number of upsets per minute. During this experiment, the flux at the measurement position was relatively unsure. However, the results show again that the memory can be tuned by two orders of magnitude in sensitivity. Similarly to the heavy-ion experiments, the cross section of 2-bit and multi-bit upsets increases significantly with shrinking supply voltage. However, the cross section for

Fig. 10: Sensor counts during mixed field experiments at CHARM.

Fig. 11: Measurement of the horizontal beam profile of the PS proton beam at Cern.

multi-bit upsets for this mixed field environment was small resulting in few undetected evens above 0.5 V.

IV. BEAM PROFILE EXPERIMENT

As an application example, the profile of the 24 GeV proton beam of the PS at Cern was measured. The sensor was mounted to a frame that could be adjusted in the X and Y direction, perpendicularly to the beam. At specific locations, separated by 5 mm, the intensity of the beam was monitored. The number of upsets due to the proton beam in a PS spill were counted and were normalized. In the next step a Gaussian distribution was estimated. This normalized plot that represents the beam shape is shown in Fig. 11. The FWHM of 15.7 mm corresponds to the custom beam monitoring measurements in the facility that monitors the beam. This proves the usefulness of the device in practice.

Fig. 12: Error map for a) 500 pJ b) 1000 pJ c) 1500 pJ laser energy and 0.9 V supply voltage. The dark areas represent no errors occurred. Light areas identify single bit errors. Individual dots represent multi-bit upsets.

Fig. 13: Error map for a 500 pJ laser energy and a supply voltage of a) 0.9 V b) 0.6 V c) 0.3V.

Fig. 14: Sensor counts during mixed field experiments at CHARM.

V. LASER EXPERIMENTS

To precisely analyze the sensitive areas of the memory cells, our Two-Photon Laser (TPA) facility is used which is a fs-pulsed laser source with a 1550 nm wavelength. The

TPA laser has an advantage that the generated charge is more localized compared to single photon absorption [21]. The procedure to test the memory was as follows. The laser setup was configured to scan the area of several cells with a 100 nm XY step size. The measurement procedure is as follows. Each step, the system triggers the microprocessor to read part of the memory and reports the address of the soft error. Then, upset cells are reset such that each step, all bits are in a pre-configured state. The laser runs continuously with a 100 Hz refresh rate. Different bit patterns were configured as discussed below. A picture of part of the memory that was scanned is shown in Fig. 14. In this picture, the dark areas are active components (diffusion). The supply and ground rails are clearly visible. This picture is taken from the back side of the chip (through the substrate) where the laser is injected as well. The memory cells were organized as back-to-back sells, similarly to the placement of digital standard cells. The orientation can be seen on Fig. 14.

During the first test, a zero fill was done in the memory such that all bits have a logic zero. Physically, the nodes contain alternating logic one and logic zero (because each cell has a symmetrical storage element) from top to bottom. Horizontally, all node states are equal. Fig. 12a-c shows the

Fig. 15: 1010 pattern with 1000 pJ laser energy and 0.3 V supply voltage. a) Error map of multiple cells b) detailed scan of multi-bit upsets. The individual dots represent multi-bit upsets.

error map of a scan with a laser energy from 500 pJ up to 1500 pJ with a supply voltage of 0.9 V during the laser injection. The physical locations of the NMOS and PMOS devices is highlighted and the boundaries of each cells are shown as well. This result corresponds to the heavy ion tests and shows that the pmos devices are initially more sensitive to low energy upsets. However, at higher energies, the nmos transistors start to trigger soft-errors as well and even lead to multi-bit upsets. 12c shows a detailed drawing on the orientation of the cell. As is expected, only the nmos or pmos of each side of the cell is sensitive since a logic 0-to-1 transition can only be generated by a pmos device. Since each node stores an inverse state, the sensitivity is also inverted. The bit pattern can be clearly seen. Fig. 13a-c shows the error map for a 500 pJ laser scan with a 0.9 V - 0.3 V supply voltage. As was expected, the sensitivity and thus the cross section of the cell increases when the supply voltage is reduced. Also the sensitivity to multi-bit upsets increases with reducing supply voltage. The physical location of the devices is identical to Fig. 12. However, MBUs were not evenly distributed with the coarse XY scan step size. Therefore, a refined scan was done on a single supply voltage

Fig. 16: Error map with a checker pattern programmed with a 1000 pJ laser energy an 0.3 V supply voltage. Each color represents a different physical bit cell.

to clarify the MBU locations.

From the previous experiment, it could be noticed that multi-bit upsets occur between cells of adjacent rows. To identify multi-cell upsets between adjacent cells a 1010 pattern is programmed in the memory. In this case, either sensitive nmos or sensitive pmos devices are directly adjacent. The results can be seen in Fig. 15a which were scanned with a 1000 pJ laser energy. However, from these results, it is clear that the multi-cell upsets between adjacent cells is not sufficient to trigger multiple errors in this case. At higher energies, this will be the case but it can be concluded that multi-cell upsets are dominated by back-to-back cells which have closely spaced nmos devices. A detailed scan of these multi-cell upsets is shown in Fig. 15b. Since the memory content was dumped each time, the content of the errors could be analyzed. However, the value of the secondary upsets did not always correspond to any closeby cells. This means that the errors are caused during the read or write operation of the memory since the laser runs continuously.

The reason why the other side of the cell does not generate read/write errors is because all horizontal cells share the same read/write line. Since the value of this line is a logic zero. No errors can be generated at that side of the cells' access transistor. This can be made clear by configuring a checkerboard pattern. Now, a 1010 pattern is programmed in even columns while a 0101 pattern is programmed in odd columns. Now, each row does not have the same logic value. The result of this scan can be seen on Fig. 16 each bit is represented by a different color. Now, each horizontal bit cells contain both 1 and 0 states. Therefore, the access transistors become sensitive to generate errors during memory access.

While the laser experiments confirm the heavy ion and proton experiments that the cells become more sensitive at small supply voltages, these results reveal data dependent sensitivity patterns. However, in a practical case, the memory can be preset each aperture time. This will result in an a priori known sensitivity map. On the other side, one can rely on the fact that the memory upset is statistically random and the average upset rate is used to monitor the radiation activity. Therefore, these data dependent sensitivities are averaged. Furthermore, during the laser experiments, the memory read interval was long compared to the aperture time to reduce the time of the measurement. In reality, the access period of the memory is small (milliseconds) compared to the aperture time of several seconds to a minute. Therefore, we are confident that the errors due to the access transistors are practically irrelevant.

Fig. 17: Chip photograph.

VI. CONCLUSION

In this paper, a flexible and low-cost SRAM based radiation monitor is presented. The measurement is based on the upset-rate in the memory cells. To dynamically adjust the sensitivity of the sensor, the supply voltage of the SRAM core can be adjusted. Heavy-ion tests and proton test showed a large dependency of the cross section on the supply voltage. Moreover, at low supply voltages the ratio of multi-bit upsets to single-bit upsets can be used to estimate the LET of the ions that is not dependent on the flux of the beam. A detailed discussion is made on the cells' sensitivity patterns using a Two Photon Laser experiment. This experiment confirmed the sensitive area that was observed from the heavy ion experiments. The SRAM was manufactured in a $0.18\ \mu\text{m}$ CMOS technology and an application example was presented to monitor the PS proton beam shape. A chip photograph is shown in Fig. 17.

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