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Author contact	<p>bram.lips@esat.kuleuven.be</p> <p>+ 32 (0)16 327986</p>

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Fabrication and characterization of double curvature bendable silicon wafers

Bram Lips and Robert Puers

Kasteelpark Arenberg 10, Heverlee 3001, Belgium

E-mail: bram.lips@esat.kuleuven.be

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Abstract. We report the design and implementation of a unique, wafer sized stretchable and bendable monolithic silicon matrix structure. The achieved stretchability not only allows for one directional folding, but is capable to bend in two directions simultaneously, required to conform the structure to complex shapes such as spheres, tori, hyperboloids or a combination of them. Moreover, it also enables dynamic mechanical deformation of the structure to cope with a moving environment, like e.g. the wall of the heart muscle. The minimal measured bending radius is 8 mm, which is 20 % smaller than the current state of art. Furthermore, a new fabrication process is proposed that enables the use of common $\langle 100 \rangle$ wafers. This enables a broader and more accessible applicability compared to earlier work, that is based on non-standard $\langle 111 \rangle$ wafers, or the more expensive SOI wafers. The technique can lead to a revolutionary potential of applications, especially in the medical field, by enabling complex silicon monitoring systems to be linked to organs without hindering them.

Keywords: Stretchable, Flexible, Deep reactive ion etching, Silicon springs, Monolithic device

1. Introduction

Different approaches have already been reported in order to render an electronic system mechanically deformable [1–7]. This deformability can be bending, stretching or a complex combination of both, such as twisting. In general, bendable and stretchable systems are distinguished by their ability to deform around either a single axis or several axes, respectively. In this regards, bendable systems can be considered a subset of stretchable systems. Bendable systems can conform to developable surfaces. These are surfaces that can be flattened onto a plane without distortion, such as a cylinder or cone [8]. More complex surfaces such as spheres or tori, however, require distortion upon flattening. These can only be conformed by stretchable systems. Figure 1 illustrates the difference between bendability and stretchability. The exact deformability requirements

Figure 1: Difference in deformability between bendable and stretchable materials.

of a system depend on the target application. If only bending is required, often organic processing technology is used [9–13]. These electronics can be fabricated fairly inexpensively. However, their inherently low mobility compared to monocrystalline silicon, limited thermal stability, and incompatibility with traditional CMOS processing technology limit their applications. An alternative approach to provide bendability relies on the extreme thinning of silicon [4, 14, 15]. In [16] ribbons of only 400 nm thick are fabricated which can sustain a bending radius of less than 7.5 μm . Slightly thicker silicon can be used if the bending requirements are less stringent. This provides the added advantage that high performance CMOS electronics can be integrated with it. An example thereof is given in [3]. The main disadvantage, however, is the extreme fragility of thinned silicon. Usually this is circumvented by supporting the thinned silicon with a polymer or another bendable material. Evidently, appropriate transfer and bonding techniques are mandatory. Such assemblies, however, can bend in one direction only.

In order to make electronic systems even more deformable, stretchability must be incorporated. Literature proposes several ways to achieve this. All these can be divided in two major categories. One consists in attaching pre-fabricated rigid silicon components to a stretchable interconnect substrate. The stretchability is primarily determined by the substrate material. In the second category, the rigid silicon is micromachined to render it stretchable. Ref [17] is an example of the first category. Here, a thin polyimide network is partially bonded on top of a pre-stretched PDMS slab. Polyimide parts that are not bonded deflect out of plane upon release of the PDMS. As such, the bendable but unstretchable polyimide is transformed into a stretchable entity. Because silicon is incorporated at specific places in the polyimide, electronic circuits can be realized. The main disadvantages of this approach are the many complex, and dedicated, processing steps required in order to obtain the final device. Including transfer printing of thin fragile silicon ribbons for transistor fabrication. In this case, standard CMOS processing can not be exploited. The polymer materials involved restrict the processing temperature and prevent, for instance, the use of dry oxide for the gate dielectric. An example of the second category, where silicon itself is rendered stretchable, is given in [18]. Here, deep reactive ion etching (DRIE) is used to create silicon spiral springs with a minimum inner diameter of 200 μm . Compared to the first category, this approach is much more compatible with standard CMOS processing. Unfortunately, the process in [18] is based on SOI wafers. In combination with the

large silicon area that is etched away, only 13% of the total area remains for actual semiconductor devices, rendering it a rather expensive approach in terms of silicon surface efficiency. A common issue of both categories however, is the formation of a stretchable, mechanical interconnection network between the rigid silicon nodes.

In this paper, we elaborate the concept of processing silicon with DRIE in to render it both stretchable and bendable in all dimensions, similar to the method explained in [18, 19]. Yet without the need of expensive SOI wafers, so common $\langle 100 \rangle$ wafers are used. Moreover, in our design, a trade-off can be made between stiffness and the area of silicon used to fabricate active devices. The interconnect design is analyzed from a mechanical point of view. Further, we improve upon [19] by incorporating metal tracks on the spring structures, to electrically connect the different rigid islands. This is indeed essential when creating electronic systems where information and energy needs to be transferred to the individual islands. A double metal layer process is elaborated in this work.

2. Concept & Fabrication

Figure 2 illustrates the concept of the stretchable monolithic silicon structure. Conceptually, transducers and electronic circuitry can be built onto individual silicon islands. Metal tracks on top of the silicon springs provide the necessary electrical interconnects between the different islands. As mentioned before, the main technique

Figure 2: Conceptual illustration of the stretchable monolithic structure.

used to achieve this silicon structure is entirely based on deep reactive ion etching (DRIE). The processing starts with a standard $\langle 100 \rangle$ wafer. Expensive SOI, or high end CMOS incompatible $\langle 111 \rangle$ wafers are not required. Since the process starts from standard wafers, electronic circuits and even surface micromachined MEMS structures can be integrated on the still rigid wafer, prior to the final processing steps that provides full flexibility to the wafer. However, in this paper we focus primarily on the fabrication of the flexible silicon rather than the electronics on the islands. Nonetheless, to prove that an electrical interconnection between these is possible, we also include a double

metal layer stack on top of the wafer.

An overview of the process is given in Figure 3. First a wet oxide of 200 nm is

Figure 3: Fabrication process. (a) Oxidation and first metal layer deposition. (b) Deposition interlayer dielectric oxide. (c) Deposition of second metal layer. (d) Wafer backside grinding and polishing. (e) Wafer bonding on glass carrier substrate. (f) Through wafer DRIE. (g) Carrier release.

grown on a 3-inch $\langle 100 \rangle$ wafer. This oxide will serve as an isolation layer between the first metal layer and the substrate. A chromium-copper metal stack is deposited through RF sputtering and subsequently patterned with lift-off. The Cr and Cu have a thickness of 25 nm and 200 nm respectively. These form the first metal layer of the electrical interconnection network. Subsequently a 200 nm SiOx inter-layer dielectric is RF sputtered. This layer is selectively etched with HF to create via connections between the bottom and the top metal layer. At the same time, the SiOx and thermal oxide is removed in places where DRIE has to take place, to prevent these layers to act as an etch stop. The second metal layer is deposited and patterned the same way as the first. Consequently, the actual processing steps to render the wafer stretchable can be performed. This starts with backside grinding and polishing the wafer to a final thickness of approximately 100 μm . This thickness has an influence on the mechanical characteristics of the system as will be explained later. The thinned wafer is now temporarily bonded onto a glass carrier. A negative resist (AZ 125nXT) is spin coated and patterned as a mask for DRIE. For normal lithographic applications, the stripping of the resist is easily achieved with its designated stripper. However, due to the intense UV-exposure during DRIE, the resist is believed to crosslink further, making it impossible to strip the resist. Therefore, an additional sacrificial LOR layer was used. Now, only the LOR layer needs to be dissolved in order to strip the mask. DRIE parameters were optimized to etch through wafer with straight sidewalls and minimal photoresist mask erosion. A more detailed description hereof is given in [20]. Finally, the stretchable

silicon is released from the glass carrier by chemically dissolving the intermediate bond layer. Figure 4 shows a picture of the final result. The yield of the entire process strongly depends on the wafer thinning, and subsequent bonding step. If executed with enough care so the wafer does not fracture, an experimental yield of 90 % is achieved.

Figure 4: Final fabrication result. Backside illuminated (left). Front side illuminated (Right). Metal tracks vias are clearly visible.

3. Spring design

Silicon springs can be implemented in several ways [18, 21]. They all rely on long thin beams to minimize stresses and strains in the material while maximizing displacement for a given applied force. Since long beams are used, available space is often a serious design constraint. This is no different in the stretchable silicon. Figure 5 compares the spring length in rest position with the area and strain efficiency of the entire device.

Figure 5: Unstrained spring length versus area and strain efficiency.

The area efficiency is calculated as given in formula 1. This yields the fraction of the wafer area that actually can be used to integrate electronics. Strain efficiency, on the other hand, is calculated by formula 2. Since islands themselves do not strain, the maximum strain of the entire matrix will be less than the maximum strain of an individual spring. This difference depends on the spring length, as shown in Figure 5.

$$\text{Area efficiency} = \frac{\text{Total Island Area}}{\text{Total Area entire device}} \quad (1)$$

$$\text{Strain efficiency} = \frac{\max(\text{strain of individual spring})}{\max(\text{strain entire device})} \quad (2)$$

From Figure 5, it is clear that area and spring efficiency can be interchanged. In our final design, we chose to have both efficiencies around 40 %. Therefore, the spring length was fixed at 0.62 times the island length. By further requiring 100 islands on a $1 \text{ cm} \times 1 \text{ cm}$ unstretched area, the spring length can be no longer than $400 \mu\text{m}$. The best way to build spring structures out of stiff materials is the serpentine design [22], as depicted in Figure 6. Key design parameters are L , R , t , W and N . These are subjected

Figure 6: Serpentine spring with N sections. Other design parameters are beam width W , bending radius R , beam length L and beam thickness t .

to application specific constraints, such as spring constant and fracture resistance, as well as fabrication constraints. For example, the width W of the ribbons ideally needs to be as small as possible for maximum stretchability [23]. However, the width cannot approach zero due to limitations of fabrication resolution as well as electrical resistance considerations of the interconnecting layers on top of the spring structures. Figure 7(a) shows the maximum local strain in the silicon relative to the strain of the spring as a whole, for different combinations of L/R and W/R . This metric is preferably as low as possible. As such, a maximum spring strain can be achieved before fracture occurs. Figure 7(b) shows the spring constant for the same combinations of L/R and W/R . Analytical formulas used to generate these plots can be found in [23]. In order to

Figure 7: (a) Calculated maximum local strain in the silicon normalized to the equivalent spring strain for different combinations of L , R and W . (b) Calculated spring constant for different combinations of L , R and W .

achieve maximum stretchability with minimum spring constant, L/R should be as large as possible, while W/R should be as small as possible. Or in other words, L is chosen as large as possible and W is chosen as small as possible. The minimum width W , is limited by electrical resistance considerations as well as mask alignment errors. All the metal tracks need to be on the springs independent of alignment errors. Therefore, the lower bound of W was chosen to be $20\text{ }\mu\text{m}$. The maximum length L , on the other hand, is dependent on the choice of R . The spring width is $L + 2 \times (R + \frac{W}{2})$, and cannot exceed the width of the island. Otherwise, horizontal and vertical running springs would overlap. Whence it limits the maximum achievable length L . The choice of R not only affects the length L , but it also affects the number of segments N out of which the spring is made. This is made visible in Figure 8. A large R will result in relative few sections

Figure 8: Dependence of N and L on the choice of R for a fixed spring area.

N with shorter lengths L . W/R will be small as will be L/R . A small R on the contrary,

will result in many sections N with longer lengths L . W/R will therefore be large but L/R will be large as well. The crosses in Figure 9 show all feasible combinations of W/R and L/R . The numbers next to them represent the corresponding number of sections N . Figure 10 shows the same data on a two-dimensional graph to better depict the optimum.

Figure 9: All feasible combinations of W , R and L with their impact on (a) maximum strain in the silicon and (b) spring constant. The numbers next to the crosses indicated the amount of sections N that correspond to the chosen W , R and L .

Figure 10: Change of maximum strain in the silicon and normalized spring constant with respect to the number of meandering sections N in the spring.

For lowest spring constant, increasing the number of sections N is always better. However, increasing it to values above $N=5$ deteriorates the spring's maximum elongation. This is visible by the rise of the maximum local strain in the material

relative to the strain of the spring as a whole. Note that this optimum at $N=5$ is quite flat. Selecting a slightly different amount of sections N does have a limited impact on the maximum spring elongation. Exactly this is the reason why the spring in the final design has $N=6$ sections instead of $N=5$. This choice lowers the spring constant by almost 30 %, while the spring strain at fracture only deteriorates by 5 %. Choosing a dedicated value for the amount of sections N together with the spring length and width, inherently determines R as well as L .

The only design parameter that is still undetermined now, is the thickness t . From [23] we can state that the thickness does not affect the maximum material strain relative to the spring strain. However, the spring constant is linearly proportional to it. This dependency is clearly visible in a simplified mechanical model of the spring. Assume that the spring displacement due to an applied force is only due to bending of the long spring beams. The curved sections are neglected for now. Then the total displacement Δx of the spring under an applied force F would be $\Delta x = \frac{FNL^3}{EtW^3}$. With E the orientation dependent Youngs modulus of silicon. The corresponding spring constant k is then $k = \frac{F}{\Delta x} = \frac{EtW^3}{NL^3}$. This approximate formula is valid only in the case where $t > W$. By decreasing the spring constant k through decreasing the thickness t , the fracture strength of the complete spring is also linearly reduced [24]. As a consequence, the thickness is a linear trade-off between spring fragility and spring stiffness.

At this point, all dimensioning is covered and the optimal spring shape is therefore determined. However, maximum spring strain and spring constant are not yet fixed. The orientation on the wafer will affect this. This is a consequence of the anisotropic nature of silicon [25]. Figure 11, shows the result of a FEA simulation where both maximum spring strain and spring constant are simulated for identical springs with different orientations on the wafer. In order to optimize the spring constant and spring strain, one should place the longitudinal axis of the spring in a $\langle 100 \rangle$ -direction. A deviation thereof will result in a lower maximum strain and higher spring constant. With maximum deviations in the $\langle 100 \rangle$ -direction of approximately -25% and $+25\%$ respectively.

4. Experimental results

A SEM image of a spring, made according to the explained process is given in Figure 12. Force and displacement were measured simultaneously for individual springs with a Femtotools device. Results thereof are shown in Figure 13. A good agreement with both analytical calculus and FEA simulations is visible. This also proves the validity of the mechanical models used to optimize the spring design. Verification of the maximum spring strain however was not possible, due to limitations of the Femtotools equipment. Its maximum possible force is limited to 1 mN, while the expected force at maximum strain is one order of magnitude bigger. Proper measurements hereof should also take into account that minor defects in the silicon lattice can heavily affect the measured results [26]. These defects can be introduced during wafer fabrication, but also during

Figure 11: FEA results of (a) maximum achievable normalized spring strain and (b) normalized spring constant with respect to the orientation of the spring longitudinal axis.

Figure 12: SEM image of a silicon spring between two silicon islands fabricated with the proposed process.

Figure 13: Measured, Simulated and Calculated force displacement curves for the fabricated silicon spring.

various wafer processing steps. A thorough characterization is therefore a subject of future work. The proof that the processed silicon can be bent around two axes simultaneously is given in Figure 14. Here the silicon is placed on a marble with a radius of 8 mm. By wetting it with isopropyl alcohol, the capillary forces ensure that the silicon conforms to the curved surface. The corresponding two dimensional bending radius of 8 mm is 20 % smaller than current state of the art [19]. Figure 15 shows the same device placed on a fingertip. A solid elements model of the stretchable silicon is build for FEA. It is meshed with a tetrahedral mesh consisting of 6740 elements per

Figure 14: Stretchable Silicon network placed on a marble with a radius of 8mm. The inset shows the same silicon network before bending.

Figure 15: Silicon network placed on the tip of a finger to showcase the two dimensional bending capabilities.

spring. Displacements and rotations are applied to give the silicon the same shape as when placed on the marble. According to this model, the maximum volumetric strain in the islands during two dimensional bending up to a radius of 8 mm is a negligible 0.006 %. This is important since semiconductor electronics generally have different characteristics under different strains [27]. Leaving the islands essentially strain free, leads to uniform electronic behaviour. Independent of the shape the silicon is conformed to. On the other hand, the maximum local strain in the silicon of the springs rises to 0.117 %. Which is still far below the practical fracture upper limit of 2 %, generally assumed in literature [18].

Electrical interconnects running over the springs were measured with simple probes. Resistivity is determined for both unstretched and stretched conditions. These are compared with the expected theoretical resistivity. Based on a bulk resistivity of sputtered Cu of 1.35×10^{-7} Ohm m [28]. The theoretical interconnect resistivity between two islands is 570 Ohm. Here, the sputter process was optimized for minimal stress in the Cu. However, by increasing the deposition power and decreasing the processing pressure, a less resistive Cu layer can be deposited [29]. In the most ideal case, the resistivity can be lowered by one order of magnitude. The measured resistivity of 560 ± 40 Ohm in the unstretched case compares well with the theoretical resistivity. According to FEA, the resistivity decreases linearly by less than 0.02 % upon stretching up to 60 %. Measurements on samples with different strains from 0 % up to 60 % are in line with the simulation. However, the 0.02 % decrease could not be measured due to precision limitations. As a consequence, measured resistivities were independent of spring strain. This is good news for the circuit interconnect design. A constant resistivity can be designed with, independent of the final degree of bending or stretching of the silicon network.

The influence of Cu interconnects and SiO₂ isolation layers on top of the silicon spring was investigated by FEA. During the design process of the spring shape these layers were neglected. The idea behind this was that the layers are much thinner than the silicon. Also, the Young's moduli of the materials are lower than that of silicon. As such, their impact on the mechanical characteristics of the spring was assumed to be minimal. Simulation results show that this assumption was indeed justified. The spring constant is not affected at all by these extra layers. The maximum stress in the silicon rises only by 4 %, indicating that the maximum strain of the metalized spring is nearly the same as the non-metalized one. This is good news. It allows to design the springs without having to worry too much about the used electrical interconnecting stack. Force displacement measurements were carried out both on metalized and non-metalized springs. No difference was measurable between both types of springs. Therefore, Figure 13 is not only valid for bare silicon springs, but also holds for springs with metal interconnects on top.

5. Conclusion

We have demonstrated a process to transform standard rigid <100> silicon wafers into double curvature bendable silicon. This is achieved by structuring the wafer into a network of rigid islands interconnected by stretchable springs. The main enabling technology herein is DRIE. As is demonstrated, such a wafer can be placed on a sphere with a radius of only 8mm. Important design considerations with respect to spring structure, dimensioning and orientation have been investigated. On top of this, electrical interconnects were fabricated and characterized. Indicating the feasibility to interconnect actuators and electronics on the individual islands with each other. This wafer scale process can theoretically be carried out on foundry processed wafers. As such enabling a wide variety of complex and high performance stretchable electronics, with applications in the medical field and far beyond.

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