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Architecture Optimization for Energy-Efficient Resolution-Scalable 8-12-bit SAR ADCs

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Abstract Low power analog-to-digital converters (ADCs) in energy constrained devices, such as wireless sensor read-out modules, often target dynamic resolution scalability with application context to reduce the average power consumption. This work implements such an 8 to 12-bit resolution scalable ADC, using an oversampling and noise-shaping successive approximating register (SAR) architecture. This architecture is selected for its high power efficiency after a detailed comparison of various resolution enhancing techniques within the SAR framework. Specifically, in this paper, three resolution enhancing techniques are reviewed and compared on their energy usage namely: the majority voting, the oversampling, and the oversampling with noise shaping SAR ADC. Furthermore, the proposed resolution scalable ADC simplifies the design of the noise shaping filter by enabling the use of a first order switched-capacitor low-pass filter for shaping the comparator noise and the in-band quantization noise. The ADC design also alleviates the matching concerns by using only an 8-bit capacitive digital-to-analog converter (DAC) for a maximum 12-bit resolution, or 11-bit effective number of bits (ENOB). The architecture can be configured to allow an operation from 8-bit traditional SAR ADC up to an 11-bit ADC by enabling the oversampling and noise shaping loops within the SAR architecture. This ADC is designed to operate with up to 320kS/s and achieves a power scaling from 80nW to 1.5 μ W, resulting in an steeper energy-ENOB scaling trend compared to state-of-the art resolution scalable ADCs.

Keywords Resolution scalable · Analog-to-digital converter · SAR ADC · Noise shaping · Majority Voting · Oversampling

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1 Introduction

Low power ADCs in sensor front ends often target resolution scalability as a function of the quality requirements for the current sensing task, to minimize the system power consumption [1–3]. Typically, such ADCs operate in low-medium frequency range with resolutions ranging between 8 to 12-bit depending on the application. The charge redistribution SAR ADC provides very high energy efficiency, enables smooth resolution scalability, and is well suited for implementation in advanced CMOS technologies [4]. Yet, its operation is often limited to less than 10-bit due to the increased power consumption of the noise limited comparator [4] and the matching requirements of the DAC capacitor array [5]. Different resolution enhancing techniques such as majority voting [6, 7], oversampling [6], noise-shaping with oversampling [8] and DAC mismatch error shaping [5] have been proposed in literature to overcome the power bottleneck of a traditional SAR ADC at high resolutions. Most of these techniques use some form of oversampling to reduce the quantization noise floor by distributing the quantization noise over a wider bandwidth. Then, by low-pass filtering the ADC output over the signal bandwidth, these architectures enable an improvement in the ADC's signal-to-noise ratio (SNR). Such oversampled architectures allow further resolution enhancement by adding a noise shaping feedback loop, which shapes the comparator and the in-band quantization noise to higher frequencies, thus enhancing the in-band SNR [9]. Moreover, these techniques enable efficient resolution scalable ADCs, because the lowest resolution mode only uses a conventional, low-resolution SAR ADC.

This paper makes a detailed comparison of three resolution enhancing techniques for SAR ADC namely, a) majority voting, b) oversampling and c) oversampling with noise shaping from a power-efficiency point of view. Based on the comparison results, this work then introduces an 8 to 12-bit

resolution scalable ADC by combining the architecture of the oversampled, noise shaping converter with an 8-bit capacitive DAC based SAR ADC. Such an architecture was first used in [8] for a fixed resolution, and is here improved along the following two aspects. First, it enables a configurable ADC architecture that allows to scale resolution from 8-bit with a traditional SAR ADC, to up to 12-bit by selectively enabling the oversampling and the noise shaping loops in the SAR architecture. Secondly, it simplifies the noise shaping filter design down to a simple, first order switched capacitor based filter. The 90nm CMOS ADC design presented in this paper targets speech processing applications with a sampling rate of up to 320kS/s for a signal bandwidth of up to 10kHz.

The paper is organized as follows: Section II reviews three resolution enhancing techniques for the SAR ADC architecture and compares their performance based on their energy consumption and resolution scalability. Next, based on the comparison results, Section III details the mathematical model of oversampling and noise-shaping SAR ADC while Section IV details the transistor level design in 90nm CMOS process. Section V explains the particulars of the circuit simulation setup and provides the simulation results. Conclusions are presented in Section VI.

2 Review on resolution enhancing techniques for SAR ADC

Due to its high energy efficiency, the successive approximation analog-to-digital converter (SAR ADC) is the most commonly used data converter architecture in the 6 to 10-bit, low-energy region [4]. Very often the performance of the basic SAR architecture is however limited to an ENOB below 10-bit due to: a) high power consumption requirements to reduce the comparator noise, and b) the matching requirements of the DAC array. In the following subsections, we first discuss the impact of resolution on the power consumption of the individual blocks in a conventional SAR ADC and then use this to provide a review and comparison of three architectural methods that enhance the SAR resolution beyond 10-bit ENOB and also enable better power-vs-resolution performance.

2.1 Conventional SAR ADC

Capacitive DAC: The key element of the SAR ADC design is the feedback DAC which generates the analog voltage that is compared to the sampled input voltage. In low power operation, the charge redistributing capacitive DAC type is most often used due to its low static power consumption [1,

10]. The capacitive DAC energy consumption per converted sample is described by [11]:

$$E_{DAC} = \zeta \cdot \sum_{i=1}^n 2^{n+1-2i} \cdot (2^i - 1) \cdot C_u V_{ref}^2 \quad (1)$$

Where parameter n represents the resolution, V_{ref} the reference voltage, ζ an architectural parameter that depends on the DAC switching scheme and C_u the unit capacitance. The supply voltage V_{DD} is taken as 1.2V, which is the nominal voltage of a UMC 90nm CMOS process. As a consequence, the voltage V_{ref} of the DAC is taken as 0.8V which ensures a typical saturation voltage margin of 200mV on both the positive and negative supply rail. The architectural factor ζ is taken as 1, which represents a conventional switching DAC. A smaller unit capacitance C_u reduces the energy consumption, but its minimum size is limited by thermal noise, capacitor mismatch and technology constraints. In our further study, only thermal noise and technology constraints are taken into account, which limit the smallest capacitance to 1fF.

Dynamic latched comparator: The second component in the SAR ADC signal flow is the comparator, which takes the consecutive decisions to generate one digital output bit per conversion cycle. In low power SAR ADC designs, the dynamic latched comparator is most commonly used as opposed to the static comparator, for its high speed and power efficiency [1]. The comparator energy per n -bit sample conversion is approximately derived as [12]:

$$E_{comp} = 2n^2 \cdot \ln(2) \cdot C_{load} V_{eff} V_{DD} \quad (2)$$

Where V_{eff} is the overdrive voltage of the input differential pair, equal to 50mV in weak inversion designs [12]. The parameter C_{load} is the single ended capacitance at the comparator output node, which optimization is limited by the comparator input referred noise. An approximate formula for this input referred noise is given by [12]:

$$\sigma_{in,comp}^2 = \kappa \frac{2kT\gamma}{C_{load}} \quad (3)$$

Where κ is an architecture dependent parameter, γ the thermal noise factor equal to 2/3 and kT the product of the Boltzmann constant and absolute temperature, taken as 300K. The comparator is designed by enforcing the input noise RMS value to follow $\sigma_{in,comp} < 0.1 \cdot V_{LSB}$.

Logic: The third and last component of the conventional SAR ADC is the logic which controls the feedback DAC using the comparator decisions and which stores the digital output value. The most common way to construct an n -bit SAR logic is to use $n + 1$ D-flipflops for the timing control and n D-flipflops for the record register [13]. The energy

Fig. 1 Estimation on energy consumption of the conventional SAR ADC components, normalized to 1 at the 8-bit total energy consumption.

consumption per sample of the SAR ADC logic can then be expressed as:

$$E_{logic} = \alpha \cdot n(2n + 1) \cdot E_{DFF} \quad (4)$$

Where α is the switching activity factor and the energy E_{DFF} is the average switching energy of a D-flipflop. The logic energy is estimated using parameters $\alpha = 0.4$ and E_{DFF} as $8 \cdot C_{min} \cdot (V_{DD})^2$ assuming a D-flipflop build with 8 minimal sized gates and where C_{min} is taken $1fF$.

Using the equations (1 - 4) an estimation of the SAR ADC energy consumption as a function of the ADC resolution is presented in figure 1, where the energy is normalized to the total energy of the 8-bit resolution ADC. At low resolutions the power consumption of the logic dominates, where at high resolutions the power consumption of the comparator dominates. The transition around 9-10-bit where the power dominance shifts towards the comparator, is a general trend observed in SAR ADCs. This trend is caused by the power consumption and sizing of the comparator becoming too large to achieve the desired high accuracy [1]. The next subsections discuss three resolution enhancement techniques to overcome this power-bottleneck in the 8-12-bit resolution range, and also evaluate the impact of these enhancements on the energy consumption of the modified SAR ADC.

2.2 Majority voting SAR ADC

The first technique that enhances the resolution of the SAR ADC with low power operation is *Majority Voting* [6,7]. This technique focuses on reducing the comparator power consumption, which is often a bottleneck factor to achieve high ENOB [1]. In the following section, first the 1 bit enhancement is explained and subsequently elaborated towards a generic increase in resolution, denoted by Δn .

Fig. 2 System level diagram for the 1-bit enhancing, majority voting SAR ADC. Majority voting components are highlighted in black.

2.2.1 Operation principle

One bit enhancement: The system diagram for a 1-bit enhancing using majority voting in a 3-bit SAR ADC is shown in figure 2. Around the conventional n_0 -bit SAR ADC, indicated by the gray color, two extra blocks are added: i) the DAC size is increased by 1 bit for a final resolution of $n_0 + 1$; and ii) extra logic is added in parallel with the existing SAR logic, called the voting logic.

The 1-bit enhancing majority voting principle works as follows. First, the SAR ADC resets the DAC voltage V_{DAC} and samples the input voltage V_{IN} . Then, the SAR bit cycling operations resolve 1 output bit every cycle as in a conventional SAR. When the input to the comparator ($V_{REF}/2 - V_{DAC}$) becomes smaller than half of the designed V_{LSB} voltage of the comparator, the SAR ADC switches from normal bit cycling mode to majority voting mode. In this mode the comparator takes a number of consecutive votes, NV , on the same DAC input voltage. As the comparator input noise is Gaussian shaped, the majority vote out of these NV decisions yields a smaller effective input noise. In general, it is shown that the effective input noise RMS value becomes [7]:

$$\sigma_{in,eff} = \frac{\sigma_{in,comp}}{\sqrt{0.64NV + 0.36}} \quad (5)$$

When the effective input noise $\sigma_{in,eff}$ reaches half of the conventional input noise $\sigma_{in,comp}$, one extra bit is converted with the correct accuracy. Figure 3 visualizes this noise relation and the effect on the input referred Gaussian noise PDF.

General Δn -bit enhancement: In general this principle can be extended towards multiple bits of resolution enhancement, Δn . Therefore the DAC is extended towards $n_0 + \Delta n$ resolution and the voting logic is activated Δn times per sample conversion. This general principle is illustrated in figure 4, by the timing diagram of a 2-bit enhancing example. First, the regular SAR ADC bit cycling operations take place. Second, the comparator input becomes smaller than the designed V_{LSB} input. By taking the majority vote out of $NV_1 = 5$ comparator evaluations, an extra bit is gained. Third, another bit is gained when the comparator input becomes smaller than the first majority voting mode. A second

Fig. 3 Normalized effective input noise RMS of comparator $\sigma_{in,eff}$ in function of number of votes NV . Top-right: visualization on a 1-bit improvement of the input noise PDF.

Fig. 4 Example time diagram of a 2-bit enhanced majority voting SAR ADC: 1) The DAC voltage V_{DAC} gets precharged while V_{IN} is bottom plate sampled; 2) Regular SAR bit cycling (BC) operations resolve 1 bit every cycle; 3) Detection of a small comparator input, which enables the majority voting mode where the comparator takes NV_1 evaluations to resolve one extra bit; and 4) Detection of smaller comparator input where majority voting takes NV_2 comparator evaluations to obtain a second extra bit.

majority voting mode is then triggered where the comparator makes $NV_2 = 25$ evaluations on the same DAC input. These NV_2 evaluations reduce the effective comparator noise $\sigma_{in,eff}$ further, as indicated by figure 3. It is noted that the number of votes NV_i take place sequentially, and increase significantly per extra bit. The final output accuracy of a majority voting SAR ADC then becomes:

$$n_{ADC} = n_0 + \Delta n \quad (6)$$

$$= n_0 + \log_2 \left(\sqrt{0.64 \cdot \max_i(NV_i) + 0.36} \right) \quad (7)$$

Where n_0 is the comparator resolution and n_{ADC} the output resolution of the majority voting SAR. Finally, it should be noted that the small comparator input voltage can occur in any of the SAR bit cycles. As a result, a separate detection circuitry is needed for each bit improvement [6].

2.2.2 Comparison to conventional SAR ADC

The energy consumption of the different components of the majority voting SAR is modeled as follows. The DAC en-

ergy is equal to the conventional capacitive DAC at the desired final ADC output resolution, i.e. $n_0 + \Delta n$:

$$E_{DAC} = E_{DAC, n_0 + \Delta n} \quad (8)$$

During one sample conversion, the comparator makes $n_0 + \sum(NV_i - 1)$ evaluations. These evaluations however occur at a reduced comparator energy of E_{comp, n_0} , which represent the energy per evaluation of an n_0 -bit designed comparator. The comparator energy then becomes:

$$E_{comp} = \left[n_0 + \sum_{i=1}^{\Delta n} (NV_i - 1) \right] \cdot E_{comp, n_0} \quad (9)$$

The comparator energy is assumed to be dynamic only and hence the energy scales linearly with the number of evaluations. The logic energy is equal to that of a conventional $n_0 + \Delta n$ resolution SAR logic:

$$E_{logic} = E_{logic, n_0 + \Delta n} \quad (10)$$

The voting logic consists out of two $\lceil \log_2(\max(NV_i)) \rceil$ bit counters that both count $\sum NV_i$ times to obtain one sample:

$$E_{vot, logic} = \alpha \cdot 2 \left\lceil \log_2 \left(\max_i(NV_i) \right) \right\rceil \cdot \sum_{i=1}^{\Delta n} NV_i \cdot E_{DFF} \quad (11)$$

where α is the switching activity factor, taken as 0.4.

The formulas (8-11) are used to compare the energy budget for a conventional SAR versus the majority voting SAR architectures, displayed in figure 5. The x-label conventions in this figure indicate the used $\max(NV_i)$ value and the originating basic resolution n_0 . The majority voting architecture saves energy compared to the conventional SAR ADC, as a result of a significant decrease in comparator energy usage. The majority voting technique is promising to gain 1 extra bit. For a 10-bit resolution target, gaining 2 extra bit is however not very beneficial in energy usage due to the high voting logic energy consumption. At higher resolution (12-bit), the voting architecture performs significantly better than the conventional SAR due to the high power consumption in the comparator for the conventional SAR.

The remaining subsections introduce two other resolution enhancement architectures, followed by a comparison on the efficiency of resolution scalability of all three architectures.

2.3 Oversampled SAR ADC

The second technique that enhances the resolution of the SAR ADC is *Oversampling*. This technique trades bandwidth for accuracy, where low-resolution and thus energy efficient components are oversampled to achieve higher ENOB.

Fig. 5 Comparison on energy budget of the majority voting versus conventional SAR at final ADC output resolution n_{ADC} of 10 (left) and 12 (right) bit. Normalized energy to total energy consumption of a conventional 8-bit SAR ADC.

Fig. 6 System level diagram for the resolution scalable, oversampled SAR ADC. The oversampling blocks are highlighted in black: i) the externally generated oversampling clock; and ii) the decimation filter.

2.3.1 Operation principle

The system diagram for the oversampling SAR ADC is illustrated in figure 6. The conventional SAR ADC blocks, highlighted in gray, are designed for a base resolution of n_0 . Two additional blocks are necessary to enable resolution enhancement with oversampling. These are: i) the externally generated oversampling input clock; and ii) the decimation filter.

The oversampling architecture up-samples the n_0 resolution SAR ADC components with a sampling speed of $OSR \cdot f_{Nyq}$ (compared to the conventional SAR sampling speed f_{Nyq}), where OSR is the oversampling ratio. This operation spreads the quantization noise of the digital output values over a larger frequency spectrum, as illustrated in figure 7. When this oversampled spectrum is further low-pass filtered by an ideal decimation filter with decimation ratio OSR^{-1} , the in-band quantization noise is reduced, thus increasing the ENOB. The resulting enhanced resolution can be expressed as [9]:

$$n_{ADC} = n_0 + \frac{1}{2} \cdot \log_2(OSR) \quad (12)$$

Further it is noted from the schematic of fig. 6 that the comparator noise enters the system at the same node as the DAC quantization noise. As a consequence, the comparator noise also undergoes the oversampling and decimating operations and hence can be designed for a lower, n_0 resolution.

Fig. 7 Principle of the oversampling ADC: the quantization noise is spread over larger frequency band. The decimation operation chops off the out-of-band noise.

Fig. 8 Comparison on energy budget of the oversampled SAR versus conventional SAR at final ADC output resolution n_{ADC} of 10 (left) and 12 (right) bit. Normalized energy to total energy consumption of a conventional 8-bit SAR ADC.

2.3.2 Comparison to conventional SAR ADC

The energy consumption per n_{ADC} -bit output sample for the different blocks is calculated as follows. The conventional blocks (DAC, comparator and logic) all exhibit a dominant dynamic power consumption, which yields a linear increase in energy with the oversampling ratio:

$$E_{OSR} = OSR \cdot E_{conv, n_0} \quad (13)$$

The decimation filter is implemented with a hardware efficient Cascaded Integrator Comb filter (CIC-filter) consisting out of two n_{ADC} -bit registers and two n_{ADC} -bit adders, of which one register-adder couple is running at a clock speed of $OSR \cdot f_{Nyq}$ while the other at f_{Nyq} [14]. This gives an estimation on the energy consumption of the decimation filter:

$$E_{dec} = 2\alpha \cdot (1 + OSR) \cdot n_{ADC} \cdot E_{DFF} \quad (14)$$

Where α is the switching activity factor taken as 0.4 and the factor 2 originates from the assumption on the adder consumption to be equal to their corresponding register.

The formulas (13-14) are used to compare the energy budget of a conventional SAR versus the $OSR = 4$ and $OSR = 16$ oversampled SAR architectures, displayed in figure 8. The oversampling architecture clearly reduces the comparator part in the energy budget, at the expense of the DAC and logic to become dominant and to consume more than their conventional counterpart. This technique is found to be less energy efficient than the conventional SAR ADC.

Fig. 9 System level diagram for the resolution scalable, oversampled noise shaping SAR ADC. The oversampled noise shaping blocks are highlighted in black.

2.4 Oversampled noise shaping SAR ADC

The third technique that enhances the resolution of the SAR ADC reuses the oversampling principle, but adds a *Noise Shaping Loop*. This technique provides a better bandwidth-resolution trade-off than simple oversampling, thus allowing to use lower OSR values to achieve a similar ENOB compared to pure oversampling. This principle is often used in sigma-delta converters, which dominate the high resolution region in the ADC space [4].

2.4.1 Operation principle

The noise shaping technique can efficiently be implemented in the SAR ADC [8], as shown in the system diagram in figure 9. The crucial blocks are: (a) a regular SAR structure consisting of the DAC, comparator and logic; (b) a noise shaping loop; and (c) a decimation filter. The input voltage V_{IN} is sampled at $f_s = OSR \cdot f_{Nyq}$ on the capacitive DAC. Based on the comparator decision, the digital logic runs the classical binary search algorithm to find the nearest digital output code.

The oversampled noise shaping architecture gains in ENOB by the oversampling and shaping of the quantization noise to higher frequencies, as illustrated in figure 10. In contrast to pure oversampling a noise shaping loop is added. This noise shaping extracts the quantization residue and subtracts it from the next sample. Moreover, these residues are processed by a low pass filter H_{NS} thereby shaping the quantization noise onto higher frequencies. When the noise shaping filter is first-order low pass and processed by an ideal decimation filter, the resolution theoretically improves with 1.5-bit per octave of OSR [9]:

$$n_{ADC} = n_0 + \frac{3}{2} \cdot \log_2(OSR) \quad (15)$$

The improvement of ENOB-OSR is further taken as 1-bit per octave of OSR, which already accounts for analog imperfections such as charge sharing and comparator kick-back noise. This design choice moreover enables a simple and efficient digital design using oversampling values of power 2.

Fig. 10 Principle of the noise shaping oversampled ADC: the quantization noise is spread over a larger frequency band and high-frequency shaped. The decimation operation chops off the out-of-band noise.

2.4.2 Comparison to conventional SAR ADC

The energy consumption per n_{ADC} -bit output sample is estimated as follows. The regular SAR components exhibit a dominant dynamic energy consumption, which yields a linear increase of energy consumption with the oversampling ratio OSR:

$$E_{osr} = OSR \cdot E_{conv, n_0} \quad (16)$$

The filter order of the decimation filter needs to be larger than the order of the noise shaping loop, in order to successfully suppress the noise-shaped high-frequency signal components [9]. A filter order of 2 is sufficient, what results in a doubling of the energy consumption compared to the pure oversampling decimation filter of equation (14):

$$E_{dec} = 4\alpha \cdot (1 + OSR) \cdot n_{ADC} \cdot E_{DF} \quad (17)$$

The noise shaping filter H_{NS} is an analog block, implementing a switched capacitor integrator [8]. This block mainly consists of an operational transconductance amplifier (OTA) that stores the quantization residue on a parallel feedback capacitor, C_{FB} . The energy consumption per n_{ADC} -bit sample is derived in the following equations (18-20): The minimum necessary transconductance in the OTA can be expressed as:

$$g_m = 2\pi \cdot \frac{C_{FB}}{\beta} \cdot \left(OSR \cdot \frac{f_{Nyq}}{2} \right) \quad (18)$$

where $f_{Nyq}/2$ is the input signal bandwidth and β is the feedback-factor ($\approx 1/2$). This estimation assumes a C_{FB} that ensures $kT/C_{FB} < 1/5 \cdot (V_{LSB}^2/12)$ for a 12-bit ADC operating at reference voltage V_{ref} . Based on a g_m/I_D approach and assuming subthreshold biasing for efficiency, the bias current per branch of the differential pair, I_D , can be estimated as

$$I_D = \frac{g_m}{20} \quad (19)$$

Using the above equation, the estimated energy for the noise shaping block can then be expressed as

$$E_{hns} = \frac{2 \cdot I_D \cdot V_{DD}}{f_{Nyq}} \quad (20)$$

Fig. 11 Comparison on energy budget of the oversampled, noise shaping SAR versus conventional SAR at final ADC output resolution n_{ADC} of 10 (left) and 12 (right) bit. Normalized energy to total energy consumption of a conventional 8-bit SAR ADC.

The derived formulas (16-20) are used to compare the energy budget of a conventional SAR versus the *OSR* of 2, 4, 8 and 16 noise shaping architectures, as displayed in figure 11. When targeting 10-bit resolution the noise shaping SAR exhibits similar energy performance as the conventional SAR ADC. This because the oversampling of the logic and the overhead of the decimation and noise shaping filter cancel the gain in comparator energy usage. On higher 12-bit resolution however, the noise shaping technique improves in energy performance. More important, the designs of $OSR = 2, 4$ and 8 consume roughly the same energy, which is explained by trading-off logic to the noise shaping filter energy usage. Consequently, the 12-bit noise shaping SAR ADC can be made using a low resolution basic architecture, i.e. an energy efficient SAR ADC with n_0 of 8-bit.

2.5 Architecture comparison

Figure 12 compares four different ADC output resolutions n_{ADC} of 9, 10, 11 and 12-bit for the conventional SAR versus the majority voting, oversampling and oversampled noise shaping architectures. All resolution enhancing techniques use a basic ADC resolution n_0 equal to 8-bit. At low resolutions of 9 and 10-bit, the majority voting technique is the most energy efficient converter. The noise shaping technique performs worse than conventional due to the overhead in the decimation and noise shaping filter. The oversampling technique explodes in energy usage, and is further not shown in the figures of 10 to 12-bit. At higher resolutions of 11 and 12-bit, the noise shaping technique becomes more energy efficient than the other architectures. By these results, the noise shaping architecture enables an 8 to 12-bit resolution scaling range, with optimal energy efficiency at high resolution (11-12-bit) and at basic resolution (8-bit). At resolutions 9 to 10-bit, the noise shaping ADC incorporates an energy overhead, making this technique less efficient.

Fig. 12 Comparison on the resolution scaling range for the conventional SAR ADC versus the majority voting, oversampling and noise shaping technique. Four different final ADC resolutions n_{ADC} of 9, 10, 11 and 12 are shown. All resolution enhancing architectures use a basic SAR ADC of resolution n_0 of 8-bit. Normalized energy to total energy consumption of a conventional 8-bit SAR ADC.

3 Design of Resolution Scalable Oversampled Noise Shaping SAR ADC

Based on a power-vs-resolution trade-off comparison in the previous section, the noise shaping, oversampled SAR ADC was found to be most promising for an 8-12-bit resolution scalable SAR ADC. To work towards a transistor level design, this section first provides a detailed mathematical model and MATLAB based system level simulations for the resolution-scalable noise shaping SAR ADC.

The oversampled noise shaping SAR ADC uses the residual charge of the DAC, present at the end of the SAR conversion cycle. This charge Q is coupled back to the input of the comparator, while also the LSB decision is fed back to the DAC. In such an architecture it can be proven that [8]:

$$V_{DAC} = D_{OUT} - V_{IN} \triangleq V_Q \quad (21)$$

$$D_{OSR}(z) = V_{IN}(z) + \frac{1}{1 + H_{NS}(z)} \cdot V_Q(z) \quad (22)$$

where H_{NS} is the transfer function used for noise shaping and V_Q is the quantization residue.

To push the quantization noise to higher frequency, the noise shaping filter H_{NS} should be low pass. A simple, but efficient approach is to use a switched capacitor based first order low pass filter with the following transfer function:

$$H_{NS}(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (23)$$

This filter is chosen over the filter of [8], because it provides a more constant increment in ENOB, which is useful for resolution scalability, whereas the filter of [8] is optimized towards a fixed OSR of 4. Further, this filter also consumes less power because it allows to use smaller capacitors.

Fig. 13 MATLAB simulation results with a 7.01kHz, 2Vppd input signal, depicting resolution scalability with oversampling ratio. Left: the ideal regular 8-bit SAR. Center: 4x oversampling with first order noise shaping. Right: 8x oversampling with first order noise shaping. Ideal decimation is used in the MATLAB simulations.

The complete architecture in figure 9 is modeled in a MATLAB environment to evaluate the proposed noise shaping filter of equation (23). Figure 13-left shows the output magnitude spectrum of an 8-bit fully differential SAR ADC with a 7.01kHz sinusoidal input signal with an amplitude 2Vppd, sampled at 20.48kHz. When the noise shaping loop and ideal decimation filter are enabled, it can be seen that the resolution increases from a DAC limited value of 8-bit to 9.9-bit with an OSR of 4 (Fig. 13-center) and to 11.5-bit for an OSR of 8 (Fig. 13-right). These MATLAB simulations show an increase of 1.5-bit ENOB per octave of OSR, equal to the theoretic expected value of first order noise shaping filters [9].

4 Circuit Design of the Oversampled Noise Shaping SAR ADC

This section details the circuit design of the resolution scalable, oversampled noise shaping SAR in 90nm UMC CMOS process. All following circuits are presented in single ended graphs, which in reality are designed fully differential. Subsection 4.1 details the blocks of the regular SAR ADC, Subsection 4.2 explains the implementation of the oversampling blocks, while Subsection 4.3 extends the design to include the noise shaping loop.

4.1 Inner SAR ADC design

A regular SAR ADC has the DAC, the comparator and the control logic as crucial functional blocks. This ADC uses a fully differential 8-bit binary weighted capacitive DAC. The unit capacitance C_u for this DAC is chosen to be a 5fF metal-oxide-metal (MOM) capacitor. The input signal is bottom plate sampled on the capacitor array, while the top plate samples the common mode voltage V_{CM} . The thermal noise

Fig. 14 Left: Circuit details of the strong arm latch based comparator. Right: The inverters to assure equal loading on the comparator output pins, and the active high reset-set (RS) latch to assure reliable interfacing to the logic.

of the single ended DAC, estimated to be $56.9\mu\text{Vrms}$ via kT/C noise, is a factor of about 5x smaller than the quantization noise with 12-bit accuracy.

A strong arm latch is used as the comparator and is designed for only 8-bit performance, as a very important advantage of the oversampled and noise shaped SAR ADC is that the comparator noise is also shaped along with the quantization noise to out of band frequencies. The architecture of the comparator is shown in figure 14, along with its interface to the digital logic. The strong arm latch is chosen, because of its speed and power advantages over a static comparator [15]. Furthermore, in order to enable scalable energy efficiency in function of the configurable ADC resolution, all the blocks of the regular SAR ADC are completely dynamic. Hence, power consumption scales linearly with the sampling frequency of the ADC, and hence with the desired resolution.

The digital SAR logic consists of a ring oscillator which generates the timing and control signals, and a code register for the control of the DAC, as used in regular SAR ADCs [13].

4.2 Oversampling components design

Figure 15 depicts the signal path for the oversampling operation in a regular SAR ADC. The sampling switch uses a transmission gate architecture, and is sized to achieve linearity of 14.5b. The top plate of the DAC samples the common mode voltage V_{CM} using a bootstrapped switch to reduce the parasitic capacitance on the top plate, while meeting the necessary linearity specification. The oversampled SAR output D_{OSR} , is fed to the OSR-scalable CIC filter.

Hardware and power efficient second order CIC filters are used for the low pass filtering and decimation of the oversampled digital signal D_{OSR} . Also here, this filter type is chosen because of its power scalability with resolution,

Fig. 15 Schematic depicting the signal flow through the oversampling blocks: the input sampling switches, the common mode DAC switch and the OSR-scalable CIC filter that enables decimation of D_{OSR} to D_{OUT} . Red highlighting of the resolution-scalable features.

Fig. 16 Schematic illustrating the integration of the noise shaping loop (black) on the oversampling signal path (gray): the first order switched-capacitor (SC) integrator samples and integrates the DAC voltage at the end of each SAR conversion. The resolution scalable features are highlighted in red: i) the input sampling frequency; ii) the powering down of the SC filter at an OSR of 1; and iii) the OSR-scalable CIC2 filter.

which is affected by scaling of the sampling frequency. The main drawback of the CIC filter is the high attenuation in the passband around Nyquist frequency.

4.3 Noise shaping components design

Figure 16 depicts the signal path for the noise shaping loop along with the oversampling path. The DAC voltage is sampled on the noise shaping capacitor C_{NS} at the end of the SAR conversion cycle, and integrated by a first order switched capacitor integrator. The output of the DAC at the end of the SAR conversion cycle is always between V_{CM} and $V_{CM} - V_{LSB}$. This allows the use of a simple telescopic cascode OTA, as the signal swing at the input and output is relatively small. The capacitor value C_{NS} was chosen to be 50fF to reduce the noise contribution of the noise shaping loop. The noise shaping loop is disabled for the lowest resolution of 8-bit, as it allows to power down the OTA, to obtain minimal power consumption at all OSR values.

Fig. 17 The 8192 points based FFT spectrum of the oversampled digital output signal D_{OSR} for a 2Vppd, 1.01kHz input signal. The ADC sampling frequency is 81.92kHz, yielding an OSR of 4.

5 Simulation Results

This section details the setup and the transistor level simulation results for the oversampled and noise shaped SAR ADC, designed in 90nm UMC CMOS. All circuits use a supply voltage of 1.2V. All displayed numbers and spectra are obtained with the Spectre simulator on transient simulations of 100ms. Transient noise is included in these simulations with $f_{noise,max} = 100\text{MHz}$ and $f_{noise,min} = 10\text{Hz}$, where noise contribution from all the transistors in the analog signal path is included. Further, a transient simulation including a 1% relative mismatch on the DAC capacitor sizes resulted in only up to 0.1-bit degradation in the ENOB. Finally, coherent sampling with 8192 points was used to estimate the FFT spectrum.

The magnitude spectrum for a differential input signal of 1.01kHz and 2Vppd, and a sampling frequency of 81.92kHz for an OSR of 4, is shown in figure 17. Using an ideal low pass filter with a cut off frequency of $f_{Nyq}/2 = 10.24\text{kHz}$, yields a signal to noise and distortion ratio (SNDR) of 60.89dB and corresponding ENOB of 9.82-bit.

Figure 18 shows the variation of ENOB versus input frequency for an OSR of 4. At higher input frequency, the ideal LPF curve slightly improves in ENOB, due to the large attenuation of the undesired harmonics which fall outside the passband of the decimation filter. The CIC2 filter achieves good ENOB at low to medium input frequencies. However, at the designed input bandwidth of 10.24kHz, the large pass-band attenuation results in a degradation of about 1-bit in ENOB.

Figure 19 (left Y-axis) illustrates the scaling of ENOB w.r.t. OSR. At an OSR of 1, the noise shaping filter is disabled, resulting in an ENOB of 7.8-bit in the regular SAR mode. At low OSR-modes, the noise shaping increases ENOB by 1.5-bit per doubling of OSR. For higher OSR-modes, the design allows to increase the OSR up to 16, and with noise shaping enabled the resolution increases up to an ENOB of 11-bit. This degradation w.r.t. the ideal 12-bit performance

Fig. 18 ENOB versus input frequency for an OSR of 4. Decimation with an ideal (dotted) and CIC2 (solid) low pass filter with a cut off frequency of 10.24kHz.

Fig. 19 ENOB (solid, left Y-axis) and Power (dashed, right Y-axis) versus OSR for an input frequency of 1kHz.

Fig. 20 Power breakdown of the resolution scalable ADC for OSR of 4 (left) and OSR of 16 (right).

estimated is due to charge sharing between the DAC and OTA and due to comparator kickback noise. Further, figure 19 (right Y-axis) also depicts the power consumption of the resolution scalable ADC as a function of the OSR. The power is estimated with a transient simulation of 10ms at an input signal of amplitude 2Vppd and frequency 1kHz. It can be seen from Fig. 19 that, by tuning the OSR, the ADC enables a power versus ENOB trade-off.

The power budget of the main blocks is represented in figure 20 for an OSR of 4 and 16. It can be seen that the power consumption of the DAC and the noise shaping loop is dominant at an OSR of 4. However, at OSR of 16, the power consumption is mainly dominated by the DAC due to the increase in sampling rate. The CIC filter is not included in the power estimation. The overall ADC power consumption sums up to 548nW at OSR of 4 and increases to 1.5μW at an OSR of 16.

Fig. 21 Simulated energy usage of this work versus ENOB, compared to the fixed resolution VLSI and ISSCC '10-'16 ADC designs [4] and other resolution scalable SAR ADC designs [1–3].

Table 1 Comparison Table

	[16]	[1]	[17]	[8]	This Work
Architecture	SAR	SAR	$\Delta\Sigma$	NS-SAR	NS-SAR
Tech. [nm]	65	65	180	65	90
Vdd [V]	0.8	0.4 - 1	1.5	1.2	1.2
f_{Nyq} [MHz]	0.08	0.02	0.20	22	0.02
Power [μ W]	0.106	0.12 - 0.23	140	806	0.08 - 1.5
ENOB [bit]	9.1	4.8 - 8.8	13.7	10	7.8 - 11.1
FoM [fJ/c-s]	2.4	22 - 143	105	35.8	18 - 53

Figure 21 compares the simulation based energy usage of this work to the other medium resolution scalable SAR ADC designs of [1–3] and the non-resolution-scalable, ISSCC and VLSI '10-'16 ADC designs [4]. This work achieves an optimal energy efficiency both at low ENOB (7.8-bit) and at high ENOB (11-bit). Further, the energy-ENOB scaling trend is much steeper thus more suited for resolution scalable designs, as compared to the other resolution scalable ADCs.

Table 1 compares this design with the state of the art ADCs with low-medium sampling frequency and 10-bit resolution. The figure-of-merit (FoM) of the proposed ADC is comparable to the state of the art ADCs. However, Ref. [16] exhibits a significantly better FoM, mainly due to the use of a very small unit capacitance of 0.25fF. Such a small unit capacitance was beyond the scope of this work, but can be combined with ideas presented here for further improvement in FoM. The FoM for this ADC is however nearly constant and has an average value of 30fJ/conv-step due to a proportional increase in ENOB with an increase in power consumption.

6 Conclusion

This work reviews the power-vs-resolution trade-off of three architectures that enhance the SAR ADC's resolution beyond the traditional DAC mismatch and comparator noise limited performance. The noise shaping oversampled SAR ADC architecture is estimated to be most energy efficient in the 8-12-bit resolution range. Based on these derived results, this work presents the design of an 8-12-bit resolution scalable, oversampled and noise shaped SAR ADC with a simplified noise shaping filter. Such an ADC architecture benefits from the energy efficiency of the charge redistribution SAR, while oversampling and noise shaping enable up to 11-bit ENOB with an only 8-bit DAC. The proposed ADC is designed in 90nm UMC CMOS and targets acoustic applications with a sampling rate of 320kS/s for a signal bandwidth of 10kHz. The dynamic nature of the ADC enables to scale the power from 80.4nW to 1.49 μ W as the resolution is varied from 8 to 11-bit, to achieve a steeper energy-ENOB scaling trend compared to state-of-the art resolution scalable ADCs.

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References

1. M. Yip and A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10-Bit 0.4-to-1V Power Scalable SAR ADC for Sensor Applications," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1453–1464, june 2013.
2. S. Fateh, P. Schonle, L. Bettini, G. Rovere, L. Benini, and Q. Huang, "A Reconfigurable 5-to-14 bit SAR ADC for Battery-Powered Medical Instrumentation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2685–2694, november 2015.
3. N. Verma and A. Chandrakasan, "An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1196–1205, june 2007.
4. B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: <http://web.stanford.edu/~murmman/adcsurvey.html>, last checked on 2016-11-18.
5. Y. S. Shu, L. T. Kuo, and T. Y. Lo, "An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, 2016.
6. P. Harpe, E. Cantatore, and A. Van Roermund, "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction," *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 270–271, 2013.
7. M. Ahmadi and W. Namgoong, "Comparator Power Reduction in Low-Frequency SAR ADC Using Optimized Vote Allocation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 11, pp. 2384–2394, november 2015.
8. J.A. Fredenburg and A.M. Flynn, "A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, december 2012.
9. D. Johns and K. Martin, *Analog Integrated Circuit Design - Chapter 14 Oversampling Converters*. New York (N.Y.): Wiley, 1997, ISBN:0-471-14448-7.
10. P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. van Roermund, "A 3nW Signal-Acquisition IC Integrating an Amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC," *2015 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, vol. 58, pp. 382–383, march 2015.
11. C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, 2010.
12. T. Sundstrom, B. Murmann, and C. Svensson, "Power Dissipation Bounds for High-Speed Nyquist Analog-to-Digital Converters," *IEEE Transactions on Circuits and Systems*, vol. 56, no. 3, pp. 509–517, march 2009.
13. T. Anderson, "Optimum Control Logic for Successive Approximation Analog-to-Digital Converters," *Comput. Design*, vol. 11, no. 7, pp. 81–86, july 1972.
14. E. Hogenauer, "An Economical Class of Digital Filters for Decimation and Interpolation," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 29, no. 2, pp. 155–162, april 1981.
15. Razavi, Behzad, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, spring 2015.
16. M. Liu, P. Harpe, R. Van Dommele, and A. Van Roermund, "A 0.8V 10bit 80kS/s SAR ADC with Duty-Cycled Reference Generation," *IEEE International Solid-State Circuits Conference*, vol. 58, pp. 278–279, march 2015.
17. A. Perez, E. Bonizzoni, and F. Maloberti, "A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-amp Third-Order $\Delta\Sigma$ Modulator Consuming 140 μ W," *IEEE International Solid-State Circuits Conference*, pp. 478–480, february 2011.