Organic RFID transponder chip with data rate compatible with electronic product coding

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ABSTRACT

Data rates of plastic transponder chips have been limited to a few kHz, limited by the inherent low mobility of organic semiconductors. However, a target application for plastic RFID tags is Electronic Product Coding (EPC), which will require, at a base carrier frequency f_c = 13.56 MHz, a data rate of $f_c/512$ = 52.969 kb/s. In this work, we show that the compatibility of organic semiconductors with high-k gate dielectrics allows boosting the current drive of transistors in functional circuits to EPC compatible clock rates. We demonstrate an 8 bit RFID transponder chip with critical dimension of 2 μm having a data rate of 50 kb/s at V_{DD} = 18 V.

1. Introduction

In recent years, many research activities in organic electronics are focused on organic radio-frequency identification (RFID) tags because of the potential of this technology to be applied in low-cost, large volume manufacturing. To find wide acceptance, RFID tags need to be compatible with Electronic Product Coding (EPC), developed for high-volume logistics applications [1,2]. Some of those EPC specifications have already been met by plastic tags in recent years, namely the transmission of 64 bit and 96 bit codes (with supplemental bits for redundancy and destroy code) [3–5], as well as the use of HF (13.56 MHz) base carrier frequency compatible with regulations concerning human exposure to electromagnetic fields [4] and basic anti-collision protocols [4]. Nevertheless, state-of-the-art organic transponder chips have shown an order of magnitude lower data rate as compared to the requirement of the EPC specifications (26.48 kb/s for the forward link and 52.969 kb/s for the return link [2]). In this work, we demonstrate organic RFID transponder chips fulfilling the latter EPC specification.

2. Technology

The critical factor to address the circuit speed is the current drive of the transistors, determined by the carrier mobility, the specific capacitance of the gate dielectric, and the inverse of the channel length. Vapor-deposited pentacene [6] has mobility, in our bottom-contact devices, of 0.5 cm²/Vs. In this work, 30 nm pentacene has been evaporated in an ultra-high vacuum chamber at 0.25 Å/s, whereby the substrate was kept at 68 °C. The isolation of the transistors is achieved by an integrated shadow mask [7], shown in Fig. 1, that results in a reliable isolation of the semiconductor area and off-currents below 10 pA. As gate dielectric, we use sputtered Al_2O_3, with a specific

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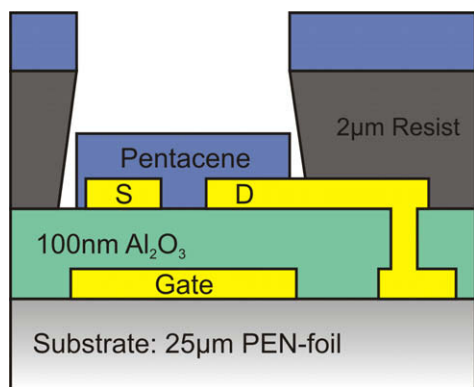
Fig. 1. Cross-section of the organic thin-film transistor process on foil having Al_2O_3, treated with a self-assembled monolayer of trichloro(phenethyl)silane, as gate dielectric.
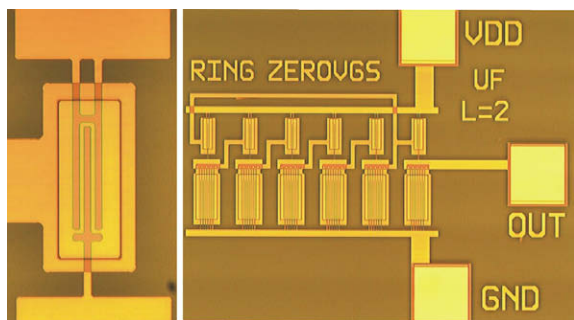
**Fig. 2.** Micrograph image of (left) a single transistor with channel length $L = 2$ μm and source/drain finger size of 5 μm and (right) a 5-stage ring oscillator with channel length $L = 2$ μm.

capacitance of 70 nF/cm^2, treated by a self-assembled monolayer of trichloro(phenethyl)silane. That, in turn, allows for some downscaling the transistor channel length, in our case to 2 μm, while maintaining a reasonable output resistance in saturation of Ro = 9.75 MΩ at 0 V gate-source voltage. A cross-section of this process flow is depicted in Fig. 1. Fig. 2 shows a micrograph image of a 5-stage ring oscillator realized in this technology.

This organic thin-film circuit technology allows to design with lower overlap capacitance and to downscale the transistor channel length, within the boundaries achievable by existing high-throughput tools (e.g. steppers used in backplane manufacturing). In this work, we varied the channel lengths (L) of the circuits between 20 μm and 2 μm. We also limited the gate-source and gate-drain overlap capacitances by decreasing the width of the finger-shaped source and drain contacts (that overlap the gate) from 5 μm to 2 μm. Fig. 2 shows a micrograph image of one transistor. All devices and circuits are processed on 25 μm thick polyethylene naphthalate (PEN) foil, which was, during processing, laminated on a 150 mm carrier substrate, and delaminated after completion of the process.

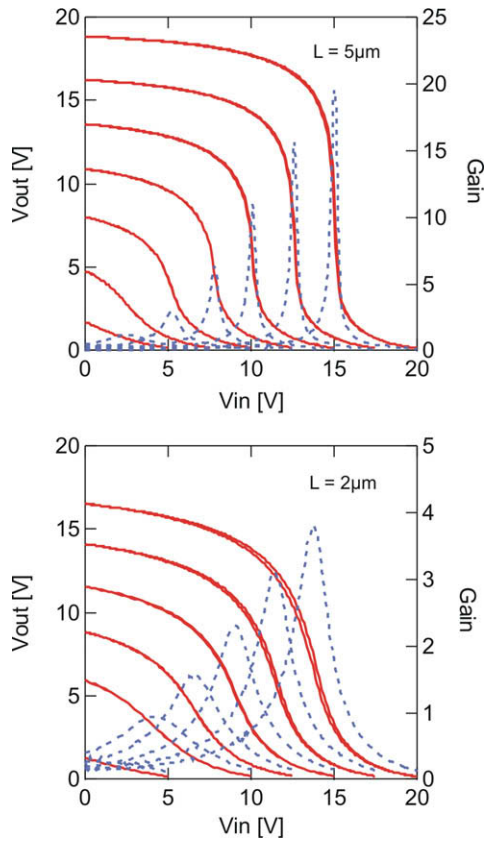## 3. Results and discussion

Typical transfer and output curves of transistors fabricated in this technology, having $L = 5$ μm and 2 μm, are depicted in Fig. 3. The transistors are normally-on and the charge carrier (hole) mobility exceeds 0.5 cm^2/Vs for both 2 and 5 μm channel length devices. The output resistance in saturation at gate-source voltage of 0 V is 206.6 ± 8.1 MΩ for $L = 5$ μm and 9.75 ± 0.22 MΩ for $L = 2$ μm. Fig. 4 shows a typical transfer curve of a zerovgs-load
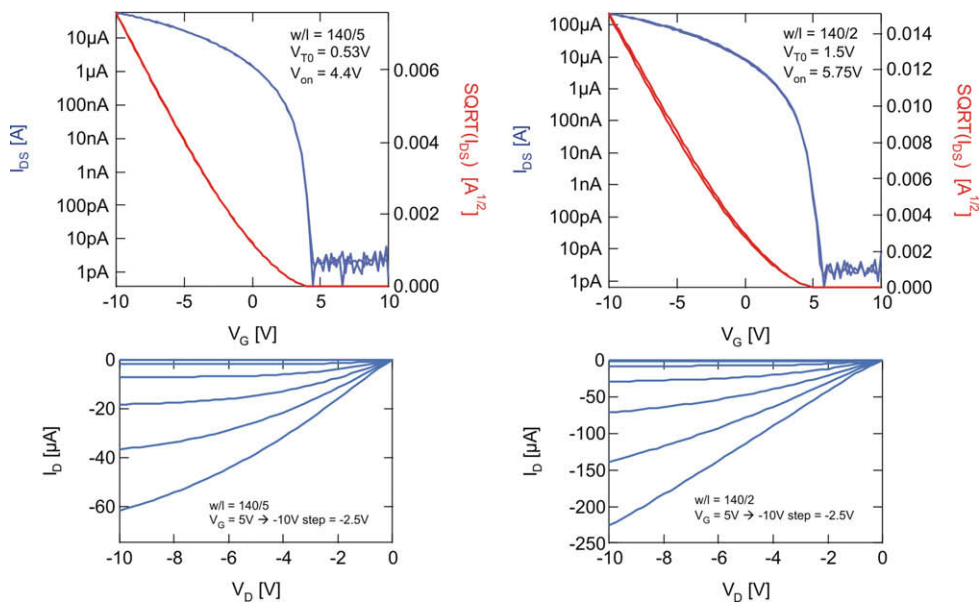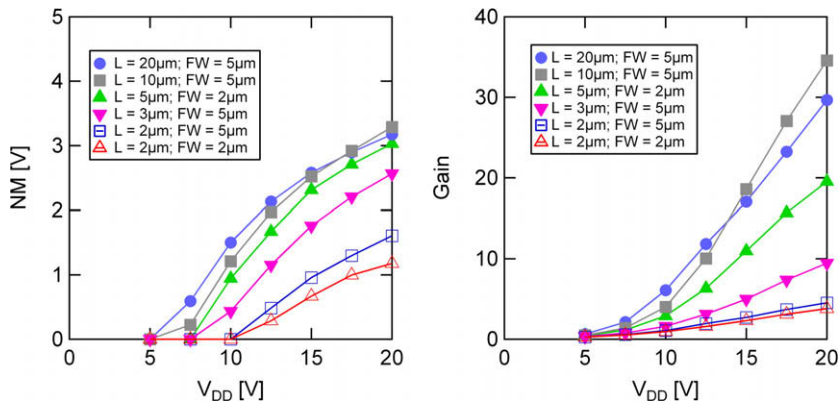

Fig. 3. Typical measured (top) transfer and (bottom) output curves of transistors with (left) $W/L = 140/5$ and (right) $W/L = 140/2$. The mobility exceeds 0.5 cm^2/Vs, off-current is below 10 pA.

inverter [3] with channel lengths of 5 µm and 2 µm, having reduced gate-drain and gate-source overlap while varying the supply voltage between 5 and 20 V. The ratio between

drive and load transistor is 1:10. Both inverters show high gains and noise margins.

In Fig. 5, the extracted main parameters of an inverter (noise margin and gain) are plotted as a function of supply voltage for different inverters with varying channel length and overlap capacitance. The gain of these inverters varies from 3.8 to 34.5 for increasing channel length at a supply voltage of 20 V. This is mainly due to a lower output resistance with increasing channel lengths. The noise margin figure indicates that long channel lengths yield more robust inverters with larger noise margins at different supply voltages. As a consequence, the inverters with long channel lengths are more robust at supply voltages below 10 V, at the expense of lower speed. This effect is shown in Fig. 6, where we plot the inverter stage delay as a function of
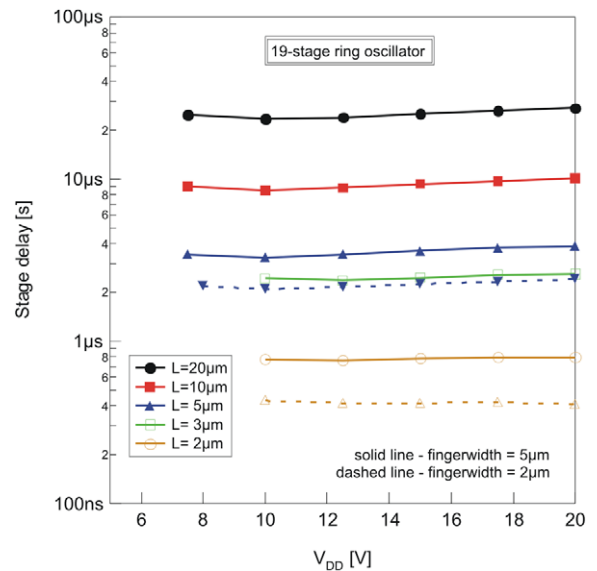

Fig. 4. Series of measured transfer curves of an inverter when varying the supply voltage between 5 and 20 V for transistors having a drive:load transistor ratio of 1:10 (zerovgs-load inverter configuration), source/drain finger sizes of 2 µm and a channel length of (top) 5 µm and (bottom) 2 µm. The solid lines represent the measured transfer curves, whereas the dashed lines represent the calculated gain.

Fig. 6. Overview of stage delays versus supply voltage, measured on 19-stage ring oscillators with varying channel lengths, between 20 µm and 2 µm (color and symbol codes) and source/drain finger sizes of 5 µm (solid lines) and 2 µm (dashed lines).
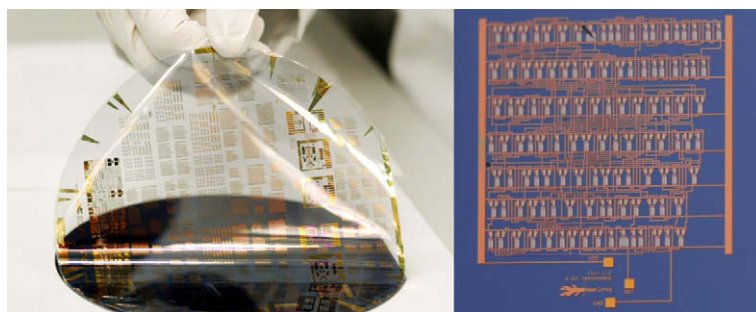

Fig. 5. Noise margin (left) and gain (right) as a function of increasing supply voltage, extracted out of the measured transfer curves of inverters having different channel lengths (20–2 µm) and different overlap capacitance (finger width FW = 5–2 µm).

Fig. 7. Photograph of the 150 mm foil being delaminated from the carrier wafer (left) and a detailed die picture of the 8 bit RFID transponder chip on foil (right). The die size is 24.73 mm^2. The design comprises 294 transistors.

supply voltage, as extracted from 19-stage ring oscillators, for transistors with channel lengths varying from 20 μm to 2 μm and with gate-overlap of the transistor-fingers ranging from 5 μm to 2 μm. Stage delays below 1 μs, and as low as 400 ns, are shown at V_{DD} as low as 10 V. The effect of decreasing the overlap capacitance is also shown in Fig. 6 for the circuits having a channel length of 2 μm and 5 μm: shrinking the overlap from 5 μm to 2 μm improves the stage delay by a factor of 1.5–2.

We proceeded with the design and realization of 8 bit RFID transponder chips, having a channel length of 2 μm and either 5 μm or 2 μm finger widths. Fig. 7 shows the photographs of the 150 mm wafer and a zoom of the die. The corresponding schematic is depicted in the inset of Fig. 8. This figure also depicts the output signal of both types of transponders having a channel length of 2 μm. The obtained data rate is 8.69 kb/s for the channel length of 5 μm and finger width of 2 μm. A data rate of 21.68 kb/s has been obtained for a channel length of 2 μm and finger width of 5 μm. In agreement with the two-fold faster inverter stage delay for the 2 μm fingers, the data rate of this transponder is also twice as high as that of the

design with 5 μm fingers. The obtained data rate of the 8 bit transponder with channel length and fingers of 2 μm is a record 50 kb/s, which is a 25-fold improvement over the latest published result [4].

4. Conclusions and outlook

In summary, this work shows that organic RFID transponder chips with EPC-compatible data rates can be realized with organic semiconductors, mainly thanks to the combination of such semiconductors with high-k dielectrics without penalty in the charge carrier mobility. The high-k dielectrics allow high accumulation charge densities, hence drive current, and open options for shorter channel lengths, down to 2 μm, without loss of saturation in the transistor output characteristics. Specific figures for the speed that we achieved are gate delays in 19-stage ring oscillators down to 400 ns at V_{DD} = 10 V, and bit rates for 8 bit RFID transponders of 50 kb/s at V_{DD} = 18 V.

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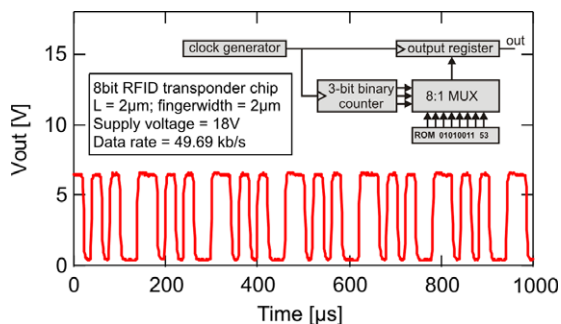
Fig. 8. Measured signal of the 8 bit RFID transponder chip having transistors with channel length of 2 μm. The width of the source-drain fingers is also 2 μm. The supply voltage for the 8 bit transponder chip was 18 V, yielding a data rate of 49.69 kb/s. The inset shows the schematic overview of the digital logic portion of the 8 bit transponder chip.