Charge Transport in Organic Transistors Accounting for a Wide Distribution of Carrier Energies—Part II: TFT Modeling

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Abstract—A physically based analytical model of the drain current of an organic thin-film transistor is proposed. It is compared with the measurements collected from transistors made with different gate insulators, organic semiconductors, and fabrication processes. The extracted model parameters provide quantitative information on the charge transport in the active layer of the transistor. The analysis suggests that the tail states are an intrinsic property of the organic semiconductor, whereas the deep states arise from the interaction between the semiconductor and the gate insulator. The relative importance of tail and deep localized states is related to the operating regions of the transistor. The resulting mathematical expressions are simple and suitable for computer-aided design implementation.

Index Terms—Computer-aided design (CAD) applications, density of states (DOS), organic thin-film transistor (OTFT).

I. INTRODUCTION

ORGANIC electronics have been identified as a viable candidate for low-cost, disposable, large-area, and flexible electronics. The transistors are the main building blocks for any electronic circuit. Therefore, understanding and modeling the physical phenomena occurring in organic thin-film transistors (OTFTs) is essential to further improve the device performance and to rationally design organic circuits.

Over the years, many models to study and/or describe the charge transport in OTFTs have been proposed in the literature [1]–[7]. All of them take into account, directly or indirectly, the effect of the density of states (DOS) on the drain current. More in detail, in the pioneering work of Horowitz and Delannoy [1],

the model was based on a single trap level located near the majority-carrier transport band. Subsequent works [2], [3] accounted for the effect of charge trapping by empirical gate-voltage-dependent mobility. Such dependence was physically explained by Vissenberg and Matters [8] assuming an exponential DOS and solving the variable-range hopping (VRH) transport by means of the percolation theory. The derived expressions of the conductivity and the mobility have been the starting point to develop several OTFT models recently proposed [4]–[7].

On the other hand, the assumption of an exponential DOS seems to be in contradiction with several specific studies [9]–[14], which extracted the DOS from thin-film transistors (TFTs) based on different organic semiconductors. These investigations demonstrate that the DOS of single-crystal, amorphous, doped, or undoped organic semiconductors can be well approximated by a Gaussian function, an exponential function, or by a combination of these functions. More specifically, the tail states can be approximated by a Gaussian or an exponential function, whereas the localized states at deep energies are well described by an exponential function.

In this paper, the theory proposed in Part I [15] is used to derive an analytical model for OTFTs with a double exponential DOS. The model is compared with a large number of experimental data collected from transistors made using different organic semiconductors, gate insulators, and fabrication processes. This analysis reveals the origin of the deep trap states and thus reconciles the different experimental results. Furthermore, the model enables a detailed discussion of the relative importance of deep and tail states on the measured characteristics, and the extracted parameters yield physical information about the charge carrier transport. A quantitative criterion is given in order to understand, directly from the experimental data, the usefulness of the proposed theory and model. The OTFT model is the natural extension of [4]–[7].

This paper is organized as follows: In Section II, transistor fabrication is described. In Section III, the analytical model of the drain current of an OTFT is derived. In Section IV, it is compared with the experimental characteristics measured from different transistors, and the physical parameters are discussed. In Section V, conclusions are drawn.

II. DEVICE FABRICATION

The transistors are fabricated on 25- μm -thick polyethylene naphthalate (PEN) foil laminated on a removable Si support

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Fig. 1. (a) PEN foil on a rigid silicon wafer. (b) Delaminated foil obtained after the fabrication process. (c) Pentacene molecule. (d) Precursor pentacene molecule. (e) Transistor stack.

wafer of 150-mm diameter (see Fig. 1). Gate electrodes and first-level interconnect lines are made by patterning the gold using standard photolithographic techniques.

Pentacene TFTs: A 100-nm-thick aluminum oxide (Al_2O_3) is sputtered as a gate dielectric. Source-drain electrodes are gold covered by pentafluorobenzene thiol, which improves hole injection into the p-type semiconductor. The semiconductor is a layer of evaporated pentacene [see Fig. 1(c)], with an average thickness of 30 nm. The transistors were characterized in nitrogen atmosphere using an Agilent 4156C parameter analyzer. The fabrication and measurements have been carried out at IMEC.

Precursor pentacene TFTs: The gate dielectric is a 350-nm-thick photoimageable polymer [polyvinyl phenol (PVP)], which is spin coated and subsequently exposed to ultraviolet light to define contact holes. Source-drain electrodes and second-level interconnect lines are defined in the second gold layer. On top of this stack, a 50-nm-thick precursor pentacene [see Fig. 1(d)] film was spin coated. Synthesis of this tetrachlorobenzene precursor and conversion procedure to pentacene are described in [16]. The transistors were fabricated and tested in air, without the use of flow boxes, and using as-purchased materials for the photolithography steps. The fabrication and measurements have been carried out at Polymer Vision.

III. OTFT MODEL

Here, the theory proposed in Part I [15] is used to derive the drain current expression of an OTFT. For convenience, we remember that, in the case of a double exponential DOS, the conductivity and the mobility are given by the following equations:

$$\sigma = \sigma_0 \left[\frac{\pi N_t T_t^3}{(2\alpha)^3 B_c T^3} \right]^{\frac{T_t}{T}} \exp \left(\frac{\Delta E_F}{k_B T} \right) \quad (1)$$

$$\mu = \left[\frac{1}{\mu_d} + \frac{1}{\mu_t} \right]^{-1} \quad (2)$$

where $\mu_d = \sigma/(qn_d)$, $\mu_t = \sigma/(qn_t)$ and n_d , n_t are the carrier concentrations related to deep and tail states, respectively. N_t is the total density of tail states, and T_t is the DOS width, which takes into account the energetic disorder of the tail states. α is the charge spatial localization parameter, $B_c = 2.8$, k_B is the Boltzmann's constant, T is the temperature, and ΔE_F is the energy difference between the Fermi level and the lowest unoccupied molecular orbital (LUMO) one.

In the following, the equations for the drain current are developed for n-channel transistors, and they can be easily rewritten for p-type ones.

The integral expression of the drain current, which is valid in all the regions of operation, can be determined as [6]

$$I_{DS} = \frac{W}{L} \int_{V_S}^{V_D} \int_{\varphi_s}^{\varphi_s} \frac{\sigma(\varphi, V_{ch})}{F_x(\varphi, V_{ch})} d\varphi dV_{ch} \quad (3)$$

where W is the channel width; L is the transistor channel length; V_S and V_D are the source and drain voltages, respectively; V_{ch} is the channel potential (i. e. the electron quasi-Fermi level); φ is the electrostatic potential; and φ_s is the electrostatic potential at the gate insulator/organic semiconductor interface. $\sigma(\varphi, V_{ch})$ is calculated according to (1), where $\Delta E_F = q(\varphi - V_{ch}) + \Delta E_{Fi}$, $\Delta E_{Fi} = E_{Fi} - E_{LUMO}$, and $E_{Fi} = E_{gap}/2$. Under the gradual channel approximation, the electric field F_x along the direction orthogonal to the insulator/semiconductor surface can be calculated with the 1-D Poisson equation, resulting in

$$F_x(\varphi, V_{ch}) = \sqrt{\frac{2q}{\epsilon_s} \int_{V_{ch}}^{\varphi} n(\varphi', V_{ch}) d\varphi'} \quad (4)$$

where $\epsilon_s = \epsilon_0 k_s$, ϵ_0 is the vacuum permittivity, and k_s is the relative permittivity of the semiconductor. In a double exponential DOS, the carrier concentration can be written as $n = n_d + n_t$, where n_d and n_t are calculated with [15, eq. (22)] specialized with parameter sets $\{N_d, T_d\}$ and $\{N_t, T_t\}$, respectively. Substituting the expression of the carrier concentration into (4) and integrating, the drain current can be written as

$$I_{DS} \simeq \frac{W}{L} \sigma_0 \left[\frac{\pi N_t \left(\frac{T_t}{T} \right)^3}{(2\alpha)^3 B_c} \right]^{\frac{T_t}{T}} \int_{V_S}^{V_D} dV_{ch} \int_{V_{ch}}^{\varphi_s} d\varphi \times \frac{\exp \left[\frac{q(\varphi - V_{ch}) + \Delta E_{Fi}}{k_B T} \right]}{\sqrt{\Theta_d \exp \left[\frac{q(\varphi - V_{ch})}{k_B T_d} \right] + \Theta_t \exp \left[\frac{q(\varphi - V_{ch})}{k_B T_t} \right]}} \quad (5)$$

where

$$\Theta_o = N_o \frac{2\pi k_B T}{\epsilon_s \sin \left(\pi \frac{T}{T_o} \right)} \exp \left(\frac{\Delta E_{Fi}}{k_B T_o} \right) \quad (6)$$

and we remember that $o \in \{t, d\}$. In order to solve (5), surface potential φ_s has to be calculated.

Applying Gauss' law to the insulator/semiconductor interface, the electric field results in a function of the surface potential and the gate voltage: $F_x(\varphi_s) = (C_i/\epsilon_s)(V_G - V_{FB} - \varphi_s)$, where C_i is the gate-insulator capacitance per unit area, and

V_G and V_{FB} are the gate and flatband voltages, respectively. By equating the latter expression with (4), φ_s is given by the numerical solution of the following equation:

$$\sqrt{\frac{2q}{\epsilon_s} \int_{V_{ch}}^{\varphi_s} n(\varphi', V_{ch}) d\varphi'} = \frac{C_i}{\epsilon_s} (V_G - V_{FB} - \varphi_s). \quad (7)$$

An analytical solution of (5) cannot be found, as the denominator of the integral is the sum of two exponential functions. This mathematical situation has been also encountered in the past for amorphous silicon TFTs [17]–[19]. We would like to highlight that the physics background we assumed in deriving (5) is completely different from that of amorphous silicon, but there are mathematical similarities between the equations. These are summarized here.

- 1) The VRH conductivity derived in (1) exponentially depends on factor $E_F/(k_B T)$. This is the same formulation obtained for a semiconductor where the charge carrier transport takes place in a parabolic band and $\sigma_{band} = q\mu_{band}n_{band}$, band mobility μ_{band} is constant, and $n_{band} = n_i \exp[E_F/(k_B T)]$.
- 2) A double exponential density of traps is assumed.

Following the same approach proposed in [19], the drain current [see (5)] can be rewritten as

$$I_{DS} \simeq \left(\frac{1}{I_{deep}} + \frac{1}{I_{tail}} \right)^{-1} = \left(\frac{1}{I_D^{Eq.(5)}(\Theta_t = 0)} + \frac{1}{I_D^{Eq.(5)}(\Theta_d = 0)} \right)^{-1}. \quad (8)$$

It is interesting to note that the composition rule of the deep and tail currents in (8) is analogous to the one derived for the mobility in (2). This is not surprising and can be interpreted as follows: When the Fermi energy level is located at low energy, hence at low carrier concentration, the mobility is limited by the deep states, and therefore, the drain current is given by the deep-state current. On the contrary, at large concentration, the mobility is limited by the tail states, and the transistor current is defined by the tail-state current. However, we highlight that, from a mathematical point of view, it is not possible to formally derive (8) starting from (2). It is worth noting that (8) is a very good approximation of (5) when the correlation between deep and tail states is low, which means $T_t \neq T_d$. The accuracy of the approximation increases by increasing the difference between the two characteristic temperatures. Under this hypothesis, the deep and tail states are separately considered, and the overall current can be calculated from the knowledge of the deep and tail currents. This is the key step in order to obtain an analytical expression of the drain current. When a single exponential DOS is considered, the deep and tail currents can be calculated following the same approach proposed in [6]. Thus

$$I_{deep} = \frac{W}{L} \frac{\Xi_0 \Lambda_d}{C_i^{2T_d/T}} \left[(Q'_{aS})^{\frac{2T_d}{T}} - (Q'_{aD})^{\frac{2T_d}{T}} \right] \quad (9)$$

$$I_{tail} = \frac{W}{L} \frac{\Xi_0 \Lambda_t}{C_i^{2T_t/T}} \left[(Q'_{aS})^{\frac{2T_t}{T}} - (Q'_{aD})^{\frac{2T_t}{T}} \right] \quad (10)$$

where

$$\Xi_0 = \sigma_0 \frac{k_B T \epsilon_s}{q C_i} \quad (11)$$

$$\Lambda_d = \frac{T}{2T_d - T} \left[\frac{C_i^2 \sin\left(\pi \frac{T}{T_d}\right)}{\pi N_d 2k_B T \epsilon_s} \right]^{\frac{T_d}{T}} \left[\frac{\pi N_t \left(\frac{T_t}{T}\right)^3}{(2\alpha)^3 B_c} \right]^{\frac{T_t}{T}} \quad (12)$$

$$\Lambda_t = \frac{T}{2T_t - T} \left[\frac{C_i^2 \left(\frac{T_t}{T}\right)^4 \sin\left(\pi \frac{T}{T_t}\right)}{(2\alpha)^3 B_c 2k_B T_t \epsilon_s} \right]^{\frac{T_t}{T}} \quad (13)$$

and Q'_{aS} and Q'_{aD} are the accumulated charges per unit area at the source and drain sides of the transistor, respectively.

Finally, substituting into (8)–(10), the overall drain current valid in all the transistor operating regions reads

$$I_{DS} = \frac{W}{L} \Xi_0 \left[\frac{\Lambda_d \Lambda_t \Phi_d \Phi_t}{\Lambda_d \Phi_d + \Lambda_t \Phi_t} \right] \Phi_d = \|V_{GS} - V_{FB}\|^{\frac{2T_d}{T}} - \|V_{GS} - V_{FB} - V_{DS}\|^{\frac{2T_d}{T}} \Phi_t = \|V_{GS} - V_{FB}\|^{\frac{2T_t}{T}} - \|V_{GS} - V_{FB} - V_{DS}\|^{\frac{2T_t}{T}} \quad (14)$$

and operator $\|x\|$ gives x if x is greater than zero, and zero otherwise.

IV. RESULTS AND DISCUSSION

The modeling results are compared with the experimental data collected from different devices and in a wide range of bias conditions. The derived physical parameters are discussed, and the usefulness of the proposed model is analyzed.

As a first step, we verify that the model based on a single exponential DOS [6] is not suitable to describe our experimental data over the whole biasing range. In order to extract model parameters T_o , i.e., the DOS characteristic temperature, and flatband voltage V_{FB} from the measured transfer characteristics, we used the following integral method proposed in [20]:

$$F(V_{SG}) = \frac{\int_0^{V_{SG}} I_{DS}(V'_{SG}) dV'_{SG}}{I_{DS}(V_{SG})} \quad (15)$$

where $F(V_{SG})$ is defined according to (15), and it is directly applied on the measured transfer characteristics. This method was successfully applied to amorphous silicon and organic TFTs under the assumption that the mobility follows power law dependence on the gate voltage (this condition is fulfilled when an exponential DOS is assumed). An analytical expression of (15) can be obtained by separately considering the linear and saturation regions of the transistor. In the linear region, the drain current has to be approximated with a first-order Taylor expansion, and substituting the mathematical expression into (15) results in

$$F_{Lin}(V_{SG}) \simeq \frac{T}{2T_o} (V_{SG} - V_{FB}). \quad (16)$$

In the saturation region, the current can be directly substituted into (15) without approximations and gives

$$F_{Sat}(V_{SG}) = \frac{T}{2T_o + T} (V_{SG} - V_{FB}). \quad (17)$$

Fig. 2. (Main panel) Transfer characteristics at $V_{SD} = 10$ V. The blue line with symbols shows the measured data, whereas the dashed red and green lines are the fits with a single exponential DOS model [6]. (Inset) The blue full line is the functional $F(V_{SG})$ calculated according to (15), whereas the dashed red and green lines are obtained fitting (16) and (17) at large and small V_{SG} , respectively.

Fig. 3. (Main panel) Transfer characteristics at $V_{SD} = 1$ V. The blue line with symbols shows the measured data, whereas the dashed green and red lines are the fits with a single exponential DOS model [6]. (Inset) The blue full line is the functional $F(V_{SG})$ calculated according to (15), whereas the dashed red and green lines are obtained fitting (16) at small and large V_{SG} , respectively.

By applying function (15) to the measured transfer characteristics of a transistor operating in the linear or saturation region, the numerical quantity $F(V_{SG})$ is obtained, and it can be fitted with (16) or (17). This procedure yields physical parameters T_o and V_{FB} .

The results of this method are plotted in the inset in Figs. 2 and 3. The blue line is the quantity $F(V_{SG})$ obtained from experimental data: it cannot be fitted by a straight line [see (16) and (17)] in the whole range of gate potentials. Furthermore, the shape of $F(V_{SG})$ also suggests that it could be approximated by two straight lines: one for high values of V_{SG} (dashed red line) and the other for low V_{SG} (dashed green line).

By fitting the single exponential model on these two intervals, the corresponding drain currents are compared with the measurements in the main panel in Figs. 2 and 3. Both transistors show the same results. At small values of V_{SG} ,

TABLE I
TECHNOLOGICAL, GEOMETRICAL, AND PHYSICAL PARAMETERS OF THE TRANSISTORS. W : TRANSISTOR WIDTH; L : TRANSISTOR CHANNEL LENGTH; k_{osc} : PENTACENE DIELECTRIC CONSTANT (VALUE TAKEN FROM [8]); C_i : GATE-INSULATOR CAPACITANCE PER UNIT AREA; $\mu_{FE} = (L/(WC_iV_{SD})) \times (\partial I_{SD}/\partial V_{SG})$: LINEAR FIELD-EFFECT MOBILITY CALCULATED AT $V_{SG} - V_{FB} = 20$ V; α^{-1} : LOCALIZATION RADIUS (VALUE TAKEN FROM [8]); T : DEVICE TEMPERATURE; σ_0 : CONDUCTIVITY PREFACTOR; N_t : TOTAL NUMBER OF TAIL STATES (TYPICAL VALUE, TAKEN FROM [23]); N_d : TOTAL NUMBER OF DEEP STATES; T_t : TAIL-STATE CHARACTERISTIC TEMPERATURE; T_d : DEEP-STATE CHARACTERISTIC TEMPERATURE; V_{FB} : FLATBAND VOLTAGE

	OTFT 1 (T1)	OTFT 2 (T2)
Organic Semiconductor	Pentacene	Precursor Pentacene
OSC deposition	Evaporation	Spincoating
W [μm]	1000	500
L [μm]	10	5
k_{osc}	3	3
Gate insulator	Al_2O_3	PVP
C_i [nF/cm^2]	70	9.5
μ_{FE} [cm^2/Vs]	0.045	0.154
α^{-1} [$\text{\AA}$]	2.2	2.2
T [K]	298	298
σ_0 [S/cm]	1×10^5	4.65×10^5
N_t [cm^{-3}]	1×10^{21}	1×10^{21}
N_d [cm^{-3}]	4.5×10^{20}	3.6×10^{19}
T_t [K]	360	360
T_d [K]	850	907
V_{FB} [V]	4.3	17.7

corresponding to low energies in the DOS, the transistor works in weak accumulation (subthreshold region), and the deep-state exponential DOS accurately reproduces the experimental behavior. By increasing V_{SG} , the Fermi level shifts to higher energies, and in strong accumulation, the current is overestimated by the deep-state current. On the other hand, in this operating region, the current calculated by considering only the tail states accurately reproduces the measurements.

This analysis clearly shows that the actual DOS of our devices is well described with a double exponential function, and hence, the theory presented in Part I [15] can be used to model the transistors. The fitting procedure gives a total of six parameters, namely, $\{\sigma_{0d}, T_{0d}, V_{FBd}\}$ and $\{\sigma_{0t}, T_{0t}, V_{FBt}\}$. The first set is obtained from the fit at low V_{SG} , and it is used to calculate the deep-state current, whereas the second parameters set is for the tail-state current. It is worth noting that V_{FBt} has to be considered as an equivalent flatband voltage, which takes into account the global effect of the charge localized in the deep states.

These results can be unified in a physically consistent formulation due to the proposed theory. Since the transistor conductivity only depends on the tail-state distribution [see (1)], in strong accumulation, the current is only defined by the tail exponential and results in $\sigma_0 = \sigma_{0t}$ and $T_t = T_{0t}$. When the transistor works in weak accumulation, the deep-state distribution dominates the current, and from this operating region, we have $V_{FB} = V_{FBd}$, $T_d = T_{0d}$, and $N_d \propto (N_t)^{T_t/T_d} / (\sigma_{0d})^{T/T_d}$. Since the model only depends on ratio N_t/N_d , we chose the same value of total number of tail states for the two semiconductors: $N_t = 10^{21} \text{ cm}^{-3}$ [23]. Values of N_t between 10^{20} and 10^{22} cm^{-3} are usually assumed for organic semiconductors [21]–[23]. The numerical values of parameters obtained for the different OTFTs are reported in Table I. It is important to

Fig. 4. (Blue symbols and lines) Measured and (red lines) modeled transfer characteristics of an Al_2O_3 -pentacene TFT for several source-drain voltages. ($\circ$) $V_{SD} = 1$ V. ($\triangle$) $V_{SD} = 10$ V. ($\square$) $V_{SD} = 20$ V. The geometrical and physical parameters of the transistor model [see (14)] are reported in Table I.

Fig. 5. (Main panel) Output characteristics and (inset) output conductance values of an Al_2O_3 -pentacene TFT. The blue symbols and lines are the experimental data, whereas the red lines are obtained with the analytical model of (14).

note that the hypothesis behind the theory are fulfilled both in transistors T1 (pentacene) and T2 (precursor pentacene) since $\chi \equiv T_d/T_t$ results in $\chi_{T1} = 2.36$ and $\chi_{T2} = 2.52$, and $\eta \equiv N_d/N_t$ results in $\eta_{T1} = 0.45$ and $\eta_{T2} = 0.036$. The values of η and χ obtained from both transistors fully justify approximation $E_b \simeq 0$, and hence, the conductivity only depends on the tail states (see [15, Sec. II and Fig. 2]).

The comparisons between the measurements and the analytical model [see (14)] are shown in Figs. 4–6 for Al_2O_3 -pentacene and PVP-precursor pentacene TFTs. There is a very good agreement between the experimental data and the model for both devices in the whole range of biasing conditions. In the case of a pentacene TFT (see Fig. 4), the model slightly overestimates the current at large gate voltages and small V_{SD} . From the shape of the output conductance drawn in the inset in Fig. 5, we can see that it is due to contact effects. Their con-

Fig. 6. (Blue symbols and lines) Measured and (red lines) modeled transfer characteristics of a PVP-precursor pentacene TFT. The geometrical and physical parameters of the transistor are reported in Table I.

tributions are not included in the presented model and will be treated in future work. Although in the case we are considering the contact resistances are a minor effect, they may lead to a wrong estimation of the tail-state parameters. In such situation, the extraction procedure [see (15) and (17)] has to be applied on the transfer characteristic measured at higher drain voltages. The detailed discussion on the parameter extraction procedures is beyond the scope of this paper. Further considerations can be found in [24] for a single exponential DOS, and they can be extended to the case of a double exponential function as discussed above.

Finally, in the light of the theory and the analytical model, physical information on the materials used to fabricate the transistors can be derived. 1) From the comparison of σ_0 results that the channel conductivity of precursor pentacene deposited on a PVP insulator is about four times the conductivity of pentacene on Al_2O_3 , and this is confirmed by the estimated field-effect mobility μ_{FE} reported in Table I. 2) The total number of deep states in precursor pentacene is one order of magnitude less than the value of N_d obtained for pentacene, and the DOS width is slightly broader, i.e., $T_{dT2} > T_{dT1}$. 3) The two semiconductors have the same tail-state temperature.

These results can be interpreted as follows. Tanase *et al.* [21] showed that the tail-state distribution extracted from organic light-emitting diodes can be unified with the DOS extracted from OTFTs made with the same organic materials. On the other hand, Ke *et al.* [25] showed that the distribution of interface traps and deep states strongly depends on the gate-insulator properties. Moreover, the experimental study provided by Veres *et al.* [26] indicates that the gate insulator changes the DOS of the organic semiconductor.

These findings suggest that the tail states are an intrinsic property of the organic semiconductor, whereas the deep states characterize the interaction between the semiconductor and the gate insulator. Therefore, by comparing the extracted parameters, we should conclude that precursor pentacene has been fully converted in pentacene, the two fabrication processes give semiconductors with the same intrinsic disorder ($T_{tT1} = T_{tT2}$),

Fig. 7. (Main panel) Transfer characteristics at $V_{SD} = 20$ V. The blue line with symbols shows the experimental data taken from [27], whereas the dashed red and green lines are the fits with a single exponential DOS model [6]. (Inset) The blue full line is the functional $F(V_{SG})$ calculated according to (15), whereas the dashed green and red lines are obtained fitting (17) at small and large V_{SG} , respectively.

and the interface PVP-pentacene has less traps with respect to the Al_2O_3 /pentacene one ($N_{d_{T2}} \ll N_{d_{T1}}$). This indicates that pentacene is well formed on the PVP dielectric. This analysis shows that the disorder of the organic semiconductor is enhanced by the insulator with large permittivities, and it is in agreement with the study presented in [26].

In order to investigate more in detail the nature of the tail and deep trap states, we model other four OTFTs [27], which are made with the same organic active layer (evaporated pentacene) but have different gate-insulator materials: PVP, PVP copolymer, SiO_2 treated with OTS, and SiO_2 .

Following the same procedure described before, for each OTFT ($T3 - T6$), the functional $F(V_{SG})$ is calculated by applying (15) to the transfer characteristic, and then, it is fitted by means of (17). The results are displayed in the inset in Figs. 7 and 8 for transistors made with PVP-pentacene ($T3$) and $\text{SiO}_2 + \text{OTS}$ -pentacene ($T5$), respectively. As shown in the inset in Fig. 7, in the case of $T3$, the quantity $F(V_{SG})$ obtained from the experimental data cannot be fitted by a straight line in the whole range of V_{SG} . According to the previous analysis, the DOS can be accurately approximated with a double exponential function, and the proposed model [see (14)] is needed to describe the OTFT in all the regions of operation. On the other hand, the functional calculated for $T5$ (inset in Fig. 8) can be fitted by means of only one straight line, and hence, a single exponential DOS is accurate enough to model the OTFT with the $\text{SiO}_2 + \text{OTS}$ dielectric. This result is in agreement with other works [8], [28], which successfully modeled the mobility of OTFTs by means of a single exponential DOS.

Transistors PVP copolymer-pentacene ($T4$) and SiO_2 -pentacene ($T6$) behave as $T3$ and $T5$, respectively. The fitted physical parameters of transistors $T3 - T6$ are reported in Table II, and the comparisons between the measurements and the model are displayed in the four panels in Fig. 9. It is worth to note that the DOS parameters obtained for $T3$ (PVP) and $T4$

Fig. 8. (Main panel) Transfer characteristics at $V_{SD} = 20$ V. The blue line with symbols shows the experimental data taken from [27], whereas the dashed red line is fitted with a single exponential DOS model [6]. (Inset) The blue full line is the functional $F(V_{SG})$ calculated according to (15), whereas the dashed red line is fitted using (17).

(PVP cop.) are in very good agreement with the ones calculated for $T2$ (PVP).

These results greatly support that the tail states are an intrinsic property of the organic semiconductor, whereas the deep states arise from the interaction between the semiconductor and the gate insulator. When the gate insulator introduces additional deep-energy traps in the semiconductor, the resulting DOS can be approximated by a double exponential function, and the proposed model can be used to accurately describe the drain current of the OTFTs.

Finally, it is worth to note that the functional $F(V_{SG})$ gives information about the shape of the DOS; hence, it is a useful tool to understand when the double exponential model is needed, and it can be used to accomplish an *a priori* choice. In fact, after the calculation of $F(V_{SG})$ directly from a single transfer characteristic, the OTFT model based on a single exponential DOS [6] or on a double exponential DOS [see (14)] can be appropriately chosen.

V. CONCLUSION

An analytical model for the drain current of OTFTs is derived. This extends the work in [6] to the case of a double exponential DOS. The model has been validated with experimental data collected from transistors made with different semiconductors, fabrication processes, and gate insulators.

The measurements have been interpreted by means of the proposed theory and model. The tail states are an intrinsic property of the organic semiconductor, whereas the deep states are induced by the gate insulator. When the interaction between the gate insulator and the organic semiconductor is weak, the DOS is composed by only tail states that can be approximated with a single exponential function. This is in agreement with other works [4]–[6], [8], [28]. On the other hand, when the gate insulator introduces additional traps in the semiconductor, the overall DOS can be approximated with a double exponential

TABLE II
TECHNOLOGICAL, GEOMETRICAL, AND PHYSICAL PARAMETERS OF THE TRANSISTORS. W : TRANSISTOR WIDTH;
 L : TRANSISTOR CHANNEL LENGTH; k_{osc} : PENTACENE DIELECTRIC CONSTANT (VALUE TAKEN FROM [8]);
 C_i : GATE-INSULATOR CAPACITANCE PER UNIT AREA (VALUES TAKEN FROM [27]); α^{-1} : LOCALIZATION
RADIUS (VALUE TAKEN FROM [8]); T : DEVICE TEMPERATURE; σ_0 : CONDUCTIVITY PREFACTOR;
 N_t : TOTAL NUMBER OF TAIL STATES (TYPICAL VALUE, TAKEN FROM [23]); N_d : TOTAL NUMBER
OF DEEP STATES; T_t : TAIL-STATE CHARACTERISTIC TEMPERATURE; T_d : DEEP-STATE
CHARACTERISTIC TEMPERATURE; V_{FB} : FLATBAND VOLTAGE

	OTFT 3 (T3)	OTFT 4 (T4)	OTFT 5 (T5)	OTFT 6 (T6)
Organic SemiC.	Pentacene	Pentacene	Pentacene	Pentacene
OSC deposition	Evaporation	Evaporation	Evaporation	Evaporation
W [μm]	170	170	170	170
L [μm]	130	130	130	130
k_{osc}	3	3	3	3
Gate insulator	PVP	PVP cop.	SiO_2 +OTS	SiO_2
C_i [nF/cm^2]	12.26	9.32	34.53	34.53
α^{-1} [$\text{\AA}$]	2.2	2.2	2.2	2.2
T [K]	295	295	295	295
σ_0 [S/cm]	9.3×10^6	18.6×10^6	6×10^6	3.2×10^6
N_t [cm^{-3}]	1×10^{21}	1×10^{21}	1×10^{21}	1×10^{21}
N_d [cm^{-3}]	3.6×10^{19}	3.6×10^{19}	-	-
T_t [K]	360	360	426.6	494
T_d [K]	820	855	-	-
V_{FB} [V]	3	2.5	4.35	11.2

Fig. 9. (Blue dashed lines with symbols) Measured and (red full lines) modeled transfer characteristics of pentacene TFTs with different gate insulator materials. Experimental data are taken from [27]. The geometrical and physical parameters of the transistors are reported in Table II. $V_{SD} = 20$ V.

function, and this is in agreement with many studies presented in the literature [9]–[13].

In the case of a double exponential DOS, when the OTFTs work in weak accumulation (subthreshold region), the current is dominated by the charge carrier transport in the deep states of the DOS, whereas when the transistors are biased in the linear region, the channel is strongly accumulated, and the current is defined by the tail states.

The proposed analytical OTFT model is of general applicability and can be further extended in order to account for the channel modulation and contact effects. This physically based model can be thus considered as the basic building block of a more general framework useful to investigate the physics of organic semiconductors and for circuit simulation.

REFERENCES

- [1] G. Horowitz and P. Delannoy, "An analytical model for organic-based thin-film transistors," *J. Appl. Phys.*, vol. 70, no. 1, pp. 469–475, Jul. 1991.
- [2] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "Modeling of organic thin film transistors of different designs," *J. Appl. Phys.*, vol. 88, no. 11, pp. 6594–6597, Dec. 2000.
- [3] M. Estrada, A. Cerdeira, J. Puigdollers, L. Reséndiz, J. Pallares, L. F. Marsal, C. Voz, and B. Iñiguez, "Accurate modeling and parameter extraction method for organic TFTs," *Solid State Electron.*, vol. 49, no. 6, pp. 1009–1016, Jun. 2005.
- [4] E. Calvetti, L. Colalongo, and Zs. M. Kovacs-Vajna, "Organic thin film transistors: A DC/dynamic model for circuit simulation," *Solid State Electron.*, vol. 49, no. 4, pp. 567–577, Apr. 2005.
- [5] M. Fadlallah, W. Benzarti, G. Billiot, W. Eccleston, and D. Barclay, "Modeling and characterization of organic thin film transistors for circuit design," *J. Appl. Phys.*, vol. 99, no. 10, p. 104504, May 2006.
- [6] F. Torricelli, Z. M. Kovács-Vajna, and L. Colalongo, "A charge-based OTFT model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 20–30, Jan. 2009.
- [7] O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part I—Compact DC modeling," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2952–2961, Dec. 2009.
- [8] M. C. J. M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Phys. Rev. B, Condens. Matter Mater. Phys.*, vol. 57, no. 20, pp. 12964–12967, May 1998.
- [9] O. Tal, Y. Rosenwaks, Y. Preezant, N. Tessler, C. K. Chan, and A. Kahn, "Direct determination of the hole density of states in undoped and doped amorphous organic films with high lateral resolution," *Phys. Rev. Lett.*, vol. 95, no. 25, pp. 256405/1–256405/4, Dec. 2005.
- [10] D. V. Lang, X. Chi, T. Siegrist, A. M. Sergent, and A. P. Ramirez, "Amorphous like density of gap states in single-crystal pentacene," *Phys. Rev. Lett.*, vol. 93, no. 8, pp. 086802/1–086802/4, Aug. 2004.
- [11] J. Puigdollers, A. Marsal, S. Cheylan, C. Voz, and R. Alcubilla, "Density-of-states in pentacene from the electrical characteristics of thin-film transistors," *Organic Electron.*, vol. 11, no. 8, pp. 1333–1337, Aug. 2010.
- [12] J. Puigdollers, M. Della Pirriera, A. Marsal, A. Orpella, S. Cheylan, C. Voz, and R. Alcubilla, "N-type PTCDI-C₁₃H₂₇ thin-film transistors deposited at different substrate temperature," *Thin Solid Films*, vol. 517, no. 23, pp. 6271–6274, Oct. 2009.
- [13] F. De Angelis, L. Mariucci, S. Cipolloni, and G. Fortunato, "Analysis of electrical characteristics of high performance pentacene thin-film transistors with PMMA buffer layer," *J. Non-Cryst. Solids*, vol. 352, no. 9–20, pp. 1765–1768, Jun. 2006.
- [14] N. Hulea, H. B. Brom, A. J. Houtepen, D. Vanmaekelbergh, J. J. Kelly, and E. A. Meulenkaamp, "Wide energy-window view on the density of states and hole mobility in poly(p-phenylene vinylene)," *Phys. Rev. Lett.*, vol. 93, no. 16, pp. 166601/1–166601/3, Oct. 2004.

- [15] F. Torricelli, "Charge transport in organic transistors accounting for a wide distribution of carrier energies—Part I: Theory," *IEEE Trans. Electron Devices*, to be published.
- [16] P. T. Herwig and K. Müllen, "A soluble pentacene precursor: Synthesis, solid-state conversion into pentacene and application in a field-effect transistor," *Adv. Mater.*, vol. 11, no. 6, pp. 480–483, Apr. 1999.
- [17] K. Khakzari and E. H. Lueder, "Modeling of amorphous-silicon thin-film transistors for circuit simulations with SPICE," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1428–1434, Jun. 1992.
- [18] S. Chen and J. B. Kuo, "An analytical a-Si:H TFT DC/capacitance model using an effective temperature approach for deriving a switching time model for an inverter circuit considering deep and tail states," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1169–1178, Jul. 1994.
- [19] L. Colalongo, "A new analytical model for amorphous-silicon thin-film transistor including tail and deep states," *Solid State Electron*, vol. 45, no. 9, pp. 1525–1530, Sep. 2001.
- [20] A. Cerdeira, M. Estrada, R. García, A. Ortiz-Conde, and F. J. García Sánchez, "New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions," *Solid State Electron*, vol. 45, no. 7, pp. 1077–1080, Jul. 2001.
- [21] C. Tanase, E. J. Meijer, P. W. M. Blom, and D. M. de Leeuw, "Unification of the hole transport in polymeric field-effect transistors and light-emitting diodes," *Phys. Rev. Lett.*, vol. 91, no. 21, pp. 216 601–216 604, Nov. 2003.
- [22] F. Torricelli, Z. M. Kovács-Vajna, and L. Colalongo, "The role of the density of states on the hole mobility of disordered organic semiconductors," *Organic Electron.*, vol. 10, no. 5, pp. 1037–1040, Aug. 2009.
- [23] S. Scheinert and G. Paasch, "Interdependence of contact properties and field- and density-dependent mobility in organic field-effect transistors," *J. Appl. Phys.*, vol. 105, no. 1, pp. 014 509/1–014 509/9, Jan. 2009.
- [24] M. J. Deen, O. Marinov, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part II—Parameter extraction," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2962–2968, Dec. 2009.
- [25] L. Ke, S. B. Dolmanan, C. Vijila, S. J. Chua, Y. H. Han, and T. Mei, "Investigation of the device degradation mechanism in pentacene-based thin-film transistors using low-frequency-noise spectroscopy," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 385–390, Feb. 2010.
- [26] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, and S. M. Khafaf, "Low- k insulators as the choice of dielectric in organic field-effect transistors," *Adv. Funct. Mater.*, vol. 13, no. 3, pp. 199–204, Mar. 2003.
- [27] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "High-mobility polymer gate dielectric pentacene thin film transistors," *J. Appl. Phys.*, vol. 92, no. 9, pp. 5259–5263, Nov. 2002.
- [28] M. Estrada, A. Cerdeira, I. Meijja, M. Avila, R. Picos, L. F. Marsal, J. Palares, and B. Iñiguez, "Modeling the behavior of charge carrier mobility with temperature in thin-film polymeric transistors," *Microelectron. Eng.*, vol. 87, no. 12, pp. 2565–2570, Dec. 2010.

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