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Author contact	elly.depelecijn@esat.kuleuven.be , michiel.steyaert@esat.kuleuven.be + 32 (0)16 326586

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A Fully Integrated Switched-Capacitor Based AC-DC Converter for a 120V_{RMS} Mains Interface

Elly De Pelecijn and Michiel Steyaert
KU Leuven ESAT-MICAS

Kasteelpark Arenberg 10, 3001 Heverlee, Belgium
Email: elly.depelecijn@esat.kuleuven.be

Abstract—A fully integrated AC-DC power converter interfacing the 120 V_{RMS} mains and fabricated in 0.35 μm -CMOS is presented. The converter uses a variable voltage division approach in order to step down the high input voltage while increasing the power density. The design includes customized AC-switches and a high-voltage capacitor and achieves an output power of 15.16 μW at an efficiency of 80.7 % on 9.8 mm².

I. INTRODUCTION

Electronic applications powered through the AC-mains, are often accompanied by a large power converter. While the wide availability of the AC-mains holds a strong advantage for this power source, the efficiency drop of the converters at low power levels (μW - to mW-range) holds a strong limitation. As a result, applications in standby or low power applications, like sensors, suffer large energy losses if powered through the mains [1]. A fully integrated converter optimized for the μW - and mW-range can solve this problem. In the mean time, it is a small and low cost solution such that the converter can fit next to the existing converter and power the standby mode.

CMOS technologies tolerate voltages of a few volt while the mains voltage is much larger. Consequently, bridging the voltage gap between the high AC-mains (120 V_{RMS}-230 V_{RMS}) and the low DC output in a monolithic way is challenging. Traditionally, the high voltage compatibility is realized through bulky transformers [2]. Alternatively, [3] uses an ESFI-SOS technology to avoid using low quality integrated inductors at low frequencies. However, this technique is very expensive.

Like [4] and [5], this work separates the high AC-input from the on-chip active components by using a high voltage capacitor in standard CMOS. A switching capacitor mimics the effect of a variable voltage division, instead of a fixed division as in [4], such that the power density increases strongly. Compared to [5], the efficiency is boosted since the presence of a load or LDO regulation stage is not required.

Section II elaborates the theoretical idea of the power converter, followed by a circuit description of a converter facing 120 V_{RMS} at 60 Hz in section III. Finally, the measurement results of the fully integrated power converter are shown.

II. SYSTEM DESCRIPTION

A. Variable Voltage Division

In order to limit the on chip voltages, [4] capacitively divides the input AC-voltage into a voltage with a lower amplitude that is fed into a full-bridge rectifier. Due to the

Fig. 1. Illustration of V_X , created by a time dependent voltage division. Power is/is not transferred to the output during the green/red intervals.

diodes in the rectifier, power is only transferred to the output when the diodes are conducting. This happens twice per period of the input (60 Hz), when the input divided voltage reaches its peak value and is higher than the output voltage V_{DC} . The converter is left idling otherwise, thereby firmly limiting the power density of the converter and demanding a large decoupling capacitor to restrict the voltage ripple.

This work is based on a variable voltage division of the AC-input. When multiple division factors $\alpha_1 \dots \alpha_4$ are available, the sine waves $V_1(t) \dots V_4(t)$ with amplitudes $A_1 \dots A_4$, as shown in Fig. 1, can be generated:

$$V_i(t) = \alpha_i \cdot V_{AC}(t) = A_i \cdot \sin(\omega t), \text{ with } \alpha_i > \alpha_{i+1} \quad (1)$$

The blue V_X -waveform of Fig. 1 is created by combining the different $V_i(t)$. Supposing the on-chip voltage is limited by V_{MAX} , V_X can follow $V_1(t)$ until V_{MAX} is reached and then switches to $V_2(t)$, $V_3(t)$ and $V_4(t)$ gradually. As a result, V_X can be seen as a waveform based on the input V_{AC} and divided by a time dependent voltage division factor $\alpha(t)$:

$$V_X(t) = \alpha(t) \cdot V_{AC}(t) \quad (2)$$

When this V_X voltage is fed into a full bridge rectifier, it conducts more than 2 times every period of the input voltage. As shown in Fig. 1 by the green intervals, V_X is several times higher than the output V_{DC} due to the time dependent voltage division factor. Every time $V_X > V_{DC}$, the rectifier conducts

Fig. 2. Model of converter with variable capacitive division.

and transfers power to the output. As a result, the converter's power density increases significantly compared to [4].

B. Switched Capacitor Voltage Division

The time dependent voltage division could be implemented with a resistor bank and would result in the behavior described previously. However, a power converter based on resistors would result in poor efficiency [6]. As a consequence, the proposed chip uses capacitors to divide the AC voltage into a lower voltage. Fig. 2 shows the main part of the converter. The AC-input is $(V_{AC,P} - V_{AC,N})$. The divided voltage $V_{XN} = (V_X - V_{AC,N})$ behaves as in equations (3) and (4) when capacitor C_3 is switched off and on respectively. $V_{OFS2}(t)$ and $V_{OFS2,3}(t)$ are the offset voltages of the waveforms. The rectifier is assumed non-conducting in these equations.

$$\text{Off} : V_{C2}(t) = V_{OFS2}(t) + \frac{C_1}{C_1 + C_2} \cdot V_{AC}(t) \quad (3)$$

$$\text{On} : V_{C2,3}(t) = V_{OFS2,3}(t) + \frac{C_1}{C_1 + C_2 + C_3} \cdot V_{AC}(t) \quad (4)$$

A different behavior from V_X in Fig. 1 can be distinguished for V_{XN} in Fig. 3. The reason for this is double sided.

The *memory effect* creates a first difference: when $V_{C2,3}$ reaches V_{MIN} , capacitor C_3 is disconnected from C_2 and it preserves the voltage of before the switching event. No charge transfer is induced, meaning that disconnecting C_3 changes the voltage division factor (3) but does not create extra conduction moments (peaks) in [A,B], as was the case in previous section. On the other hand, the offset $V_{OFS2}(t)$ of V_{C2} changes. Still, decoupling C_3 early is desirable because it increases the slope of V_{XN} (3) so that interval [B,C], in which conduction is possible, becomes larger.

Secondly, *charge redistribution* should be considered. Connecting 2 capacitors with a different voltage induces a charge transfer that results in a DC-shift of the voltages on the capacitors. Therefore, when $|V_{XN}|$ reaches the maximum value V_{MAX} and capacitor C_3 becomes connected, a large voltage dip takes place due to charge redistribution:

$$|V_{DIP}| = \frac{C_3 \cdot V_{MAX} - C_3 \cdot |V_{OLD}|}{C_1 + C_2 + C_3} \quad (5)$$

Here, V_{OLD} is the voltage on C_3 before switching. By disconnecting C_3 , it is possible to let V_{C2} rise to V_{MAX} again and let another charge redistribution take place. As such,

Fig. 3. Waveforms of converter with switching capacitive division in 1 period. Green/red: conductive/non-conductive diode bridge. Blue: switching of C_3 .

the offset of V_{XN} is shifted step-wise to 0 until point A or C is reached. Consequently, by creating multiple charge redistribution moments, 1 capacitor is sufficient to implement a similar effect like the time dependent voltage division factor in [B,C]. This results in a strong area and complexity advantage.

$$V_{MAX} = \frac{C_1}{C_1 + C_2 + C_3} \cdot V_{AC,MAX} \quad (6)$$

V_{MAX} limits the maximum output voltage of the converter and links the capacitor values to the AC-input (6). Like V_{MIN} , the ratio between C_2 and C_3 is also crucial for the performance of the power converter, as explained subsequently.

C. System Analysis

In order to determine the different parameters of the design: C_1 , C_2 , C_3 , V_{MIN} and V_{MAX} , it is important to evaluate the output power P_{OUT} , power losses P_{LOSS} , efficiency η and area of the power converter. Following formulas, which are averaged over period T of the AC-input, are used to define the converter's performance under the assumption of a constant output voltage V_{DC} (large C_{OUT}).

$$I_{ON}(t) = \frac{C_1 \cdot C_{OUT}}{C_1 + C_{2,3} + C_{OUT}} \frac{dV_{AC}(t)}{dt} \approx C_1 \frac{dV_{AC}(t)}{dt} \quad (7)$$

$$P_{OUT} = \frac{1}{T} \cdot \int_0^T V_{DC} \cdot I_{ON}(t) dt \quad (8)$$

$$= \frac{V_{DC}}{T} \sum_{i=1}^N \int_{t_{on,i}} I_{ON}(t) dt \quad (9)$$

$$P_{LOSS} = \frac{1}{T} \sum_{j=1}^{N-2} \frac{C_3(C_1 + C_2)(V_{MAX} - |V_{OLD,j}|)^2}{2(C_1 + C_2 + C_3)} \quad (10)$$

Here, $C_{2,3}$ is C_2 or $C_2 + C_3$ when C_3 is disconnected, respectively connected. N stands for the number of conduction moments in 1 period, while $I_{ON}(t)$ is the current conducted to the output when the diode bridge is on during $t_{on,i}$. As the converter aims for the μW -range and operates at low frequencies, charge redistribution losses during switching give the most significant loss-contribution (10). This is comparable

to the ‘slow switching limit’ in switched capacitor DC-DC converters [7], so that conduction losses are neglected. Based on (7)-(10), following trade-offs between high output power and high efficiency should be considered: First of all, C_1 is desired large to increase the output power (7)-(9). This high voltage capacitor, however, creates a strong area requirement, consequently limiting the power density. Secondly, picking $V_{\min}$ close to $V_{\max}$ decreases the voltage ripple since the non-conductive interval [A,B] is shorter. Finally, the ratio between C_2 and C_3 is important. Once C_1 and $V_{\max}$ are chosen, the sum $C_3 + C_2$ is fixed by (6). Taking C_3 larger than C_2 results in large voltage dips. This causes an increment in the number of conduction moments N and leads to an increase in output power $P_{\text{OUT,AVG}}$. However, the larger the dips and the more the converter switches, the higher the losses become (10), causing the efficiency to drop.

Based on previous trade-offs, the converter is designed for a $V_{\max}$ of 14 V. This results in a peak output voltage of 12.8 V due to the voltage drop across the rectifier. The chosen capacitor values are $C_1 = 50$ pF, $C_2 = 185$ pF and $C_3 = 370$ pF.

III. CIRCUIT IMPLEMENTATION

A. Monolithic Capacitors

Capacitor C_1 bridges the voltage gap between the high AC-input and the DC-output and should sustain next voltage:

$$V_{C1} = V_{AC,P} - V_X \leq \max(V_{AC}) - V_{DC} \quad (11)$$

Taking some margin, this capacitor should thus be able to hold 200 V without breakdown. A custom design is required because the standard capacitors in the 0.35 μm technology cannot tolerate such a high voltage. Calculating with a breakdown voltage of 1 MV/cm [8], the terminals of C_1 should be separated by 2 μm . Sharp corners are not desired due to the point effect.

Based on [4], [5] and taking into account all metal density rules, the capacitor’s design is optimized to the highest capacitance density possible. The result is a capacitor with density of 24.6 pF/mm², for which the cross section of 1 cell is shown in Fig. 4 (a). The $V_{AC,P}$ -terminal is situated in the top metal and surrounds rectangular rounded islands connected to V_X . Through vias these V_X islands are connected to its terminal in a lower metal. The sizes and spacing of the islands are chosen

Fig. 4. Cross section of high voltage capacitor implementation (a) and transistor level implementation of the AC-switches (b).

to optimize the fringing capacitive coupling in the top metal even as the capacitive coupling between different metals.

Capacitors C_2 and C_3 are implemented as standard bar-capacitors. The output filter capacitance C_{OUT} is a combination of MOM and MOS capacitors.

B. Switching in AC-environment

Due to the AC input voltage, the voltage at node V_X can be higher or lower than the voltage at $V_{AC,N}$. When using a single MOS-transistor for S_{12} and S_{34} (Fig. 2), this would cause drain-bulk diodes to become forward biased such that current flows in the bulk and latch-up could take place. Fig. 4 (b) shows the implementation of one AC-switch. The left branch DMOS transistor is switched on when $V_2 > V_1$ while the right branch DMOS is used for $V_1 > V_2$. The diodes force the current in the correct direction. The function of the capacitors is to limit the drain-source voltages of the transistors when the voltage across the switches change direction.

C. Switch Driving Logic

Hysteresis comparators, clocked with an external 20 kHz-pulse, control switches S_{12} and S_{34} and decide when capacitor C_3 should be connected to C_2 . When $|V_{XN}|$ reaches $V_{\max}$, the comparator registers the voltage on C_2 is too high and C_3 should be connected. When $|V_{XN}|$ falls below $V_{\min}$, the comparator decides C_3 can switch off. To increase flexibility, the hysteresis width is set with an external voltage. Decoding logic determines the correct switch driving signals based on the output of the comparators.

The DMOS transistors used in the switches can tolerate $V_{\max}$ between source and drain. The gate-source voltage, however, should be limited to a few volt. This way, the generated control signals that swing between 0 and 3 V are not sufficient to drive the switches. Level shifters, shown as the S1-driver in Fig. 5, push these signals between the correct voltage levels, so that the transistors in Fig. 4 (b) are driven correctly. A full system overview of the power converter is given in Fig. 5.

Fig. 5. Full system overview.

Fig. 6. Chip micrograph.

IV. MEASUREMENTS

The AC-DC converter of Fig. 5 is fabricated in a $0.35\ \mu\text{m}$ technology and is measured for an input voltage of $120\ \text{V}_{\text{RMS}}$, $60\ \text{Hz}$. The micrograph of Fig. 6 shows the fully integrated converter with active area of $9.8\ \text{mm}^2$. The different capacitors can be distinguished. The performance of the converter chip is measured for a variable load current. The resulting efficiency curve is shown in Fig. 7(a) and reveals an operation region from 0 up to $15.16\ \mu\text{W}$. At maximum output power, the converter also achieves its peak efficiency of 80.7% . Figure 7(b) shows the measured voltages at nodes V_X , $V_{\text{AC},N}$ and V_{DC} for a load current of $0.6\ \mu\text{A}$ and output power of $6.85\ \mu\text{W}$. Table I compares this work to the state-of-the-art integrated power converters for AC-mains purposes. All values are measured for an input of $120\ \text{V}_{\text{RMS}}$, $60\ \text{Hz}$. Amongst the highlighted capacitive monolithic converters, this work achieves the highest power density and efficiency at peak output power and has an equal performance based on the Voltage based Scaled Output Capacitance, $\text{VSOC} = V_{\text{RIPPLE}} \cdot C_{\text{OUT}} / V_{\text{AVG}}$. This parameter reflects that for an equal amount of output capacitance, these converters have a

Fig. 7. (a) Converter efficiency vs. output power and (b) measured voltage waveforms for $I_{\text{LOAD}} = 0.6\ \mu\text{A}$ and $P_{\text{OUT}} = 6.85\ \mu\text{W}$.

comparable output ripple performance. The AC-DC converter in [6] achieves the highest power density but at very low efficiency. It should be noted that [6] uses an external $10\ \mu\text{F}$ SMD capacitor. In order to be able to compare the converters, the last row of Table I is added. C_{MAIN} is the sum of all capacitors, including externals, in the main part of each converter. Particularly, if each converter has an equal amount of capacitance at its disposal, this work as well as [4] and [5] will produce a larger amount of output power than [6]. Thanks to the presented technique, even at a higher efficiency.

TABLE I
COMPARISON TO STATE-OF-THE-ART MONOLITHIC AC-DC CONVERTERS.

	This work	[4]	[5]	[6]*
Technology [μm]	0.35	0.13	0.35	0.35
Active area [mm^2]	9.8	3.5	6	7.7
P_{MAX} [μW]	15.16	1.5	6.4	$3 \cdot 10^3$
$P_{\text{MAX}}/\text{area}$ [$\mu\text{W}/\text{mm}^2$]	1.55	0.43	1.06	390
η @ P_{MAX} [%]	80.7	59	70-75	2-3
$V_{\text{AVG}} (V_{\text{REG}})$ [V]	9.5	4	3.3	3.3
VSOC [nF]	0.45	0.2	0.45	*
$P_{\text{MAX}}/C_{\text{MAIN}}$ [W/F]	5819	440	637	300

* not fully integrated, contains $10\ \mu\text{F}$ -SMD capacitor

V. CONCLUSION

This work showed the results of a monolithic AC-DC converter capable of interfacing a high voltage of $120\ \text{V}_{\text{RMS}}$ at $60\ \text{Hz}$. Due to a variable capacitive division, power is available multiple times during the period of the input while only one capacitor faces the high AC-voltage. As a result, the converter achieves a better peak performance compared to the state-of-the-art. For the output power of $15.16\ \mu\text{W}$, an efficiency of 80.7% is achieved. This without any external component.

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