A 174 pW–488.3 nW 1 S/s–100 kS/s All-Dynamic Resistive Temperature Sensor With Speed/Resolution/Resistance Adaptability

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***Abstract*—A versatile resistive temperature sensor for Internet-of-Things is presented, based on an all-dynamic architecture. This allows efficient scaling of power with conversion rate, enables optional oversampling for an adaptable resolution, and provides efficient adaptability to different resistor values. A new double-sided measurement mode is proposed to compensate for offset, 1/f noise and nonidealities at system level. The sensor achieves a minimum power consumption of 174 pW at 1 S/s measurement rate, which scales up to 488.3 nW at 100 kS/s. It offers a nominal rms resolution of 0.61 °C and a resolution FoM as low as 1.82 pJ·°C^2.**

***Index Terms*—Duty-cycling, dynamic, Internet-of-Things (IoT), resistive bridge, SAR ADC, temperature sensor.**

I. Introduction

The recent growing interest in Internet-of-Things (IoT) applications requires a new generation of ultralow power on-demand sensing circuits. Due to the scarce energy available, circuit specifications shift from high performance requirements to ultralow power constraints. Specifically considering temperature sensors, that are widespread in IoT applications, a moderate resolution of 0.1 °C to 1 °C is usually acceptable, but the power consumption should be down to nW level. In addition, a short measurement time and ultralow sleeping power are critical to enable efficient duty-cycling of the overall IoT node. Resistor-based temperature sensors have a high efficiency [1] but mostly target high resolution, resulting in μW-level power consumption [2]. Moreover, these sigma delta modulator-based approaches require oversampling and active dc-biased circuits. This is not favorable for IoT, as conversion times are long and it is difficult to duty-cycle the dc bias quickly and efficiently. An SAR-based alternative [3] also required static biasing at μW-level. Recent low-power sensors [4], [5] have long conversion times and do not support duty-cycling, while still consuming $>$ 70 nW. The design in [6] consumes only 113 pW but is limited in temperature range ($-$20 to 40 °C) and operating speed (fixed to 0.2 S/s).

To address the above issues, an all-dynamic architecture is proposed, which allows quick and efficient duty cycling as needed for IoT. Moreover, this approach enables flexibility in operating speed and resolution (by means of optional oversampling) with inherent scaling of power. Finally, the proposed solution makes the optimization of the energy consumption possible for different values of the sensor resistance by simply adapting the timing of the interface circuitry. This enables the same interface to efficiently digitize multiple resistive sensors, even if they have different resistivity.

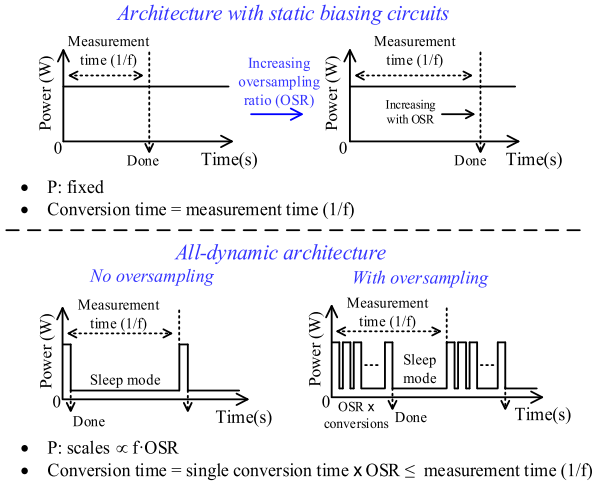

Fig. 1. Architecture with static biasing circuits versus all-dynamic architecture.

A comparison between a dc-biased architecture and the proposed all dynamic architecture is shown in Fig. 1. The architecture with static biasing circuits consumes a constant amount of power over time. Even though the resolution can be improved by a longer conversion time or a higher oversampling ratio (OSR), the absolute power (P) remains the same while the effective measurement frequency (f) goes down. Thanks to the nature of dynamic circuits, the all-dynamic architecture automatically goes to sleep mode after the conversion is completed. Therefore, speed and resolution can be set independently while the power automatically scales proportionally to f·OSR, making the sensor more versatile and suitable for low-power duty-cycled IoT nodes.

This letter shows a prototype of a versatile resistive temperature sensor with a range of 0 °C–100 °C for environmental monitoring with wireless sensor nodes. The sensor interface includes a Wheatstone bridge and an asynchronous SAR ADC. The resistive bridge is duty-cycled to avoid static power consumption [7], [8]. Beyond [7], [8], a "double sided measurement" is introduced, which improves resolution, removes ADC offset, reduces flicker noise and compensates systematic errors. The conversion time is only 10 μs and a minimum power consumption of 174 pW (at 1S/s) can be achieved while offering a nominal rms resolution of 0.61 °C and a resolution FoM down to 1.82 pJ·°C^2. If needed, the measurement rate can be increased from 1S/s up to 100 kS/s and the resolution can be improved from 0.61 °C to 0.068 °C by means of oversampling with an appropriate scaling of power.

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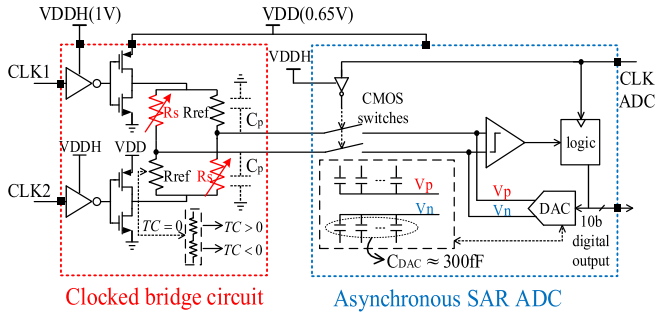

Fig. 2. Architecture of the all-dynamic resistive bridge sensor interface.

This letter is organized as follows: the proposed all-dynamic temperature sensor is described in Section II, the measurement results are presented in Section III, and the conclusions are given in Section IV.

II. Proposed All-Dynamic Temperature Sensor

A. Architecture

Fig. 2 shows the architecture of the resistive sensor interface, which includes a clocked Wheatstone bridge and an asynchronous SAR ADC. The temperature sensing resistors R_s use a nonsilicide n-diffusion resistor (0.17%/°C). A nonsilicide p-poly resistor (−0.035%/°C) and a nonsilicide n-poly resistor (0.013%/°C) in series implement the temperature independent reference resistors R_{ref}, enabling the use of R_{ref} as the reference for other types of sensors in the future. Each side of the bridge is connected to complementary switches, thus it can be connected to VDD or GND depending on the polarity of CLK1 and CLK2. A 10b asynchronous SAR ADC is used to sample and digitize the bridge output voltage. C_{DAC} is only 300fF to save both ADC and bridge power. The bridge and ADC share the same supply VDD (0.65 V) to enable a ratiometric measurement. A high voltage supply VDDH (1 V) is used to reduce the leakage of the bridge switches and to improve the ADC switch linearity. The differential output of the bridge is ±0.5 mV/°C (simulated), where CLK1 and CLK2 determine the polarity. R_{ref} is equal to the value of R_s at around 50 °C. The choice of the resistance value and its tradeoffs are elaborated in the next section.

B. Duty-Cycled Resistive Bridge and Resistance Value Choice

An asynchronous switched-capacitor SAR ADC is well-suited for IoT applications as it can digitize with a single clock edge and offers a short conversion time. Its power scales with speed as the ADC uses only dynamic circuits. To avoid static power from the resistive bridge, the bridge is duty-cycled using CLK1 and CLK2. As shown in Fig. 3, the bridge output voltage is directly sampled on the DAC capacitors of the ADC. The settling time constant τ is proportional to $R_{\text{ref}}(\approx R_s)$ multiplied by the sum of C_{DAC} and C_p, where C_p is the parasitic capacitance of the bridge, as shown in

$$\tau = 0.5 \cdot R_{\text{ref}} \cdot \left(C_p + C_{\text{DAC}}\right). \tag{1}$$

To save power, the bridge is switched off after its output voltage is settled (in about 5τ) and sampled, after which the ADC performs digitization. Therefore, the energy consumed by the bridge for one sample can be calculated as

$$E_{\text{bridge}} = \left(\text{VDD}^2/R_{\text{ref}}\right) \cdot 5\tau + 2 \cdot C_p \cdot (\text{VDD}/2)^2 \tag{2}$$

where the first term is the energy consumed by the resistors in the bridge, and the second term is the energy consumed to charge C_p. C_{DAC} does not need to be recharged, as the SAR ADC can maintain the previously sampled charge on its capacitor [9]. The charge kept on

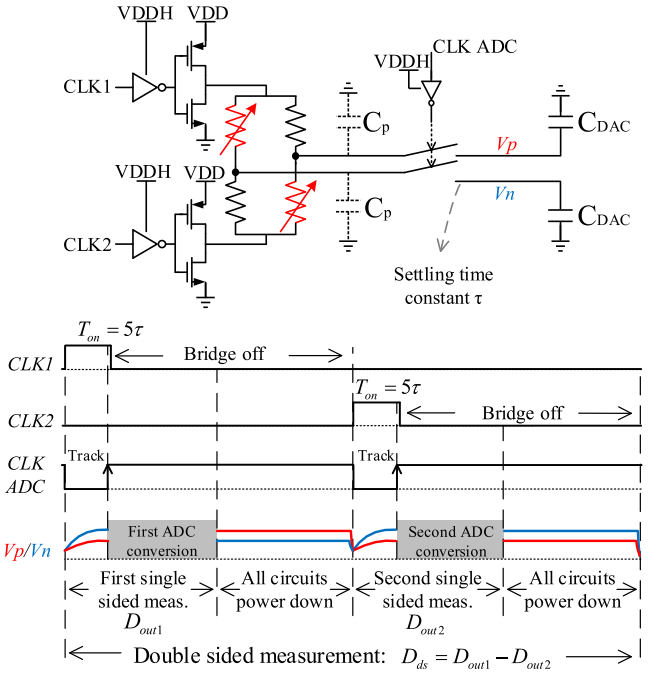

Fig. 3. Principle of duty-cycled bridge and waveforms for single sided and double sided measurements.

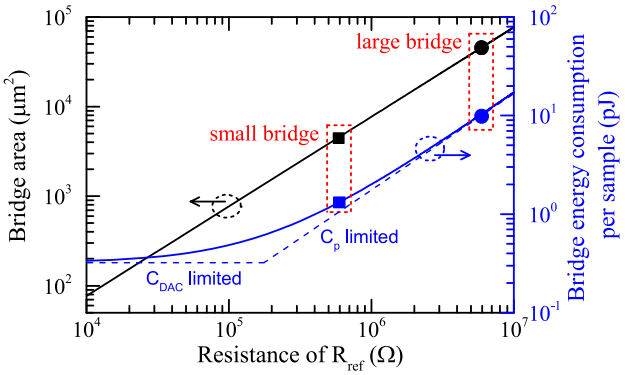

Fig. 4. Impact of the bridge resistance on bridge energy and area.

C_{DAC} is redistributed with C_p at the beginning of the next sampling period. Equation (2) can be rewritten as (3) using (1)

$$E_{\text{bridge}} = \text{VDD}^2 \cdot \left(2.5 \cdot C_{\text{DAC}} + 3 \cdot C_p\right). \tag{3}$$

This shows that, with the help of duty-cycling, the energy consumed by the bridge for one sample only depends on the DAC capacitance and the bridge parasitics C_p, but not on the bridge resistance R_{ref}. However, C_p is indirectly related to R_{ref} as a larger resistance takes a larger chip area which implies higher C_p. Therefore, in contrast to the traditional approach where a large resistance is required for low power consumption, better power efficiency can be achieved with a smaller resistance for the duty- cycled bridge, as the parasitic C_p can be reduced. Fig. 4 shows the energy per sample consumed by the bridge and the bridge area for different resistance values. Smaller resistors give a lower energy consumption as well as a smaller area. However, very small resistors suffer from increased mismatch, they require switches with a very low on-resistance, and need very short clock pulses. Therefore, as a compromise, a "small bridge" with 600 kΩ R_{ref} is chosen in this letter. A "large bridge" with 10x larger resistors is also implemented on chip to verify the theory described above. Multiplexers select which of the two bridges is active.

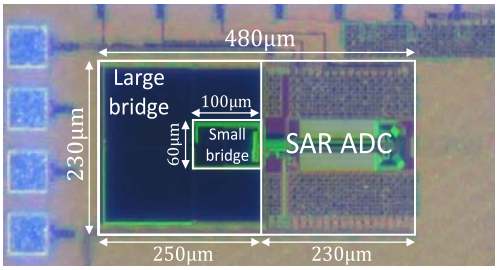

Fig. 5. Die photo.

C. Single Sided and Double Sided Measurement

The waveforms in Fig. 3 explain the operation over time. First, CLK1 is high for a time 5τ to enable the bridge, which generates a differential output voltage $V_p - V_n$. After that, CLK ADC samples the voltage and starts digitizing it, while CLK1 already goes low to switch off the bridge. The measurement result D_{out1} is produced after the conversion delay and by then all circuits are powered down. While this "single sided" measurement gives a complete temperature reading, better performance can be achieved by the "double sided" measurement which is introduced in this letter. In this case, CLK2 is enabled in a second step, enabling the bridge again but now with reversed supplies causing a reversed output voltage and a reversed second measurement D_{out2}. By subtracting D_{out2} from D_{out1}, a double sided measurement D_{ds}, which provides 3 dB higher SNR is obtained. Similar to traditional techniques such as correlated double sampling and chopping, the double sided measurement can remove ADC offset and reduce flicker noise. Moreover, it can compensate systematic nonidealities during the entire conversion, as it is implemented over the entire system. The total conversion time for a single sided measurement with the small bridge is 5 μs, including 1.5 μs bridge settling time, resulting in a maximum speed of 200 and 100 kS/s for the single and double sided measurement, respectively. The large bridge has 10x larger resistors and consequently a 10x larger C_p. This leads to a longer settling time, and consequently a maximum speed of 6.6 and 3.3 kS/s. Even though the double sided measurement has a better performance, the single sided measurement still has its advantages, as it enables shorter conversion time and does not need any digital subtraction at the ADC output.

D. Asynchronous SAR ADC

An asynchronous SAR ADC [9] is used such that a single clock edge enables the entire ADC operation. The ADC uses a segmented DAC with 3 unary and 7 binary bits to improve DNL and save power. Unit capacitors of 250 aF are employed to minimize C_{DAC} while achieving sufficiently low kT/C noise. Moreover, the DAC is not reset but returns to the previously sampled voltage after each conversion, so there is no need to spend energy charging C_{DAC} for each cycle as temperature varies slowly. Differently from [7], high-V_{th} transistors with increased length are used for the ADC logic to minimize leakage. Moreover, the sampling switch is implemented with a CMOS gate rather than using dynamic clock boosting to enable operation at very low speed.

III. Measurement Results

The entire interface was fabricated in 65 nm CMOS and occupies an area of 0.11 mm^2 (including both bridges) or 0.06 mm^2 (excluding the large bridge), as shown in Fig. 5. The bridge settling time is fixed to 1.5 μs/150 μs for small/large bridge, respectively, over all test chips and temperatures. Both bridges produce a similar output

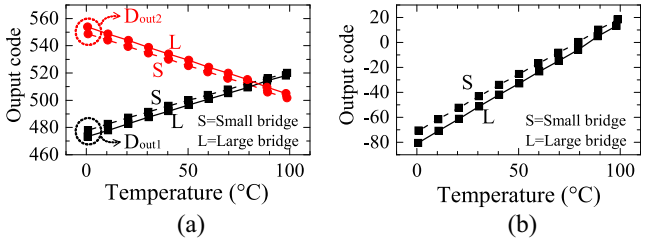

Fig. 6. Measured output code versus temperature. (a) Single and (b) double sided.

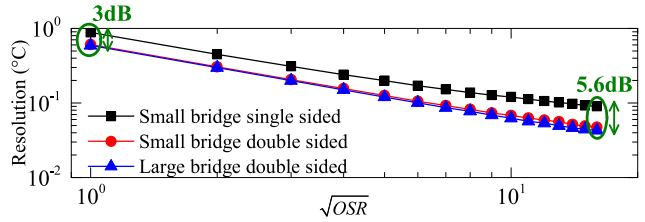

Fig. 7. Measured RMS resolution versus square root of OSR.

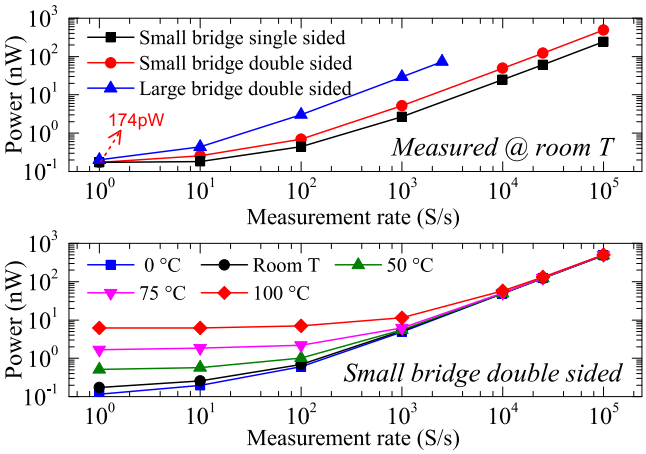

Fig. 8. Measured power consumption versus measurement frequency.

code except for some offset, as shown in Fig. 6. The measured rms resolution obtained with different OSRs is shown in Fig. 7. When there is no oversampling, 0.88/0.61 °C rms resolution is achieved for a single/double sided measurement with the small bridge for a conversion time of 5/10 μs, respectively. The small and large bridge have a similar rms noise because the resistor noise is sampled on C_{DAC} resulting in the same kT/C contribution, which is about 13% of the total noise power. The other noise contributions are 44% from ADC quantization noise and 43% from ADC comparator noise according to simulations. With the help of oversampling and averaging, the resolution can be improved effectively. The flicker noise becomes significant in the single sided mode at a high OSR, and hence limits the noise reduction. The double sided measurement suffers less from this problem, as it can reduce the 1/f noise. As a consequence, 5.6 dB noise difference is observed at a high OSR, as indicated in Fig. 7. Thanks to the all-dynamic design, the power scales proportionally to the measurement speed over more than 3 orders of magnitude (Fig. 8, top). The leakage power is 174 pW when measured at room temperature (around 25 °C), and it starts dominating the total power consumption when the speed is below 10 S/s. As expected, the large bridge consumes about 5 times more power compared to the small bridge due to the larger parasitic C_p. As leakage depends on temperature, the power consumption goes up for higher temperatures at

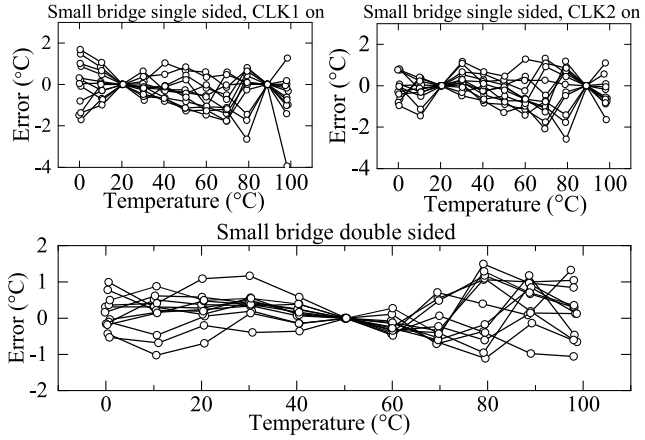

Fig. 9. Temperature inaccuracy for 12 samples, measured at 25 kS/s.

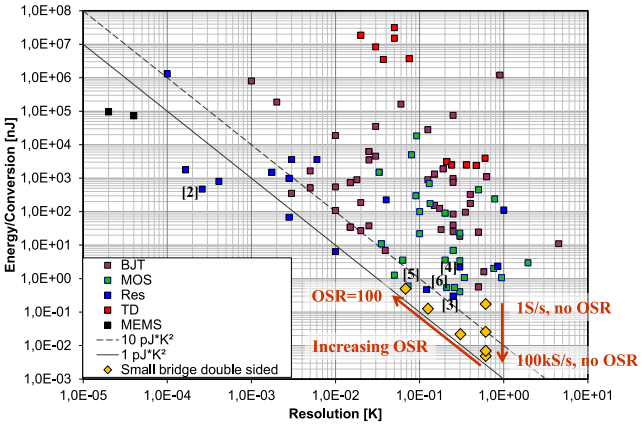

Fig. 10. Resolution FoM benchmark of this letter for various speeds and OSRs [1].

TABLE I
MEASURED PERFORMANCE SUMMARY AND COMPARISON

	[3]	[4]	[5]	[6]	This work			
Type	Res	MOS	MOS	MOS	Res			
Technology	180nm	180nm	180nm	65nm	65nm			
ADC	SAR	FDC	FDC	TDC	SAR			
Area(mm^2)	0.18	0.09	0.008865	0.15	0.06 (small bridge + ADC) 0.11 (two bridges + ADC)			
T range (°C)	0~100	0~100	-20~100	-20~40	0~100			
Inaccuracy (°C) calibration method	-0.5/0.5 1-point	-1.4/1.5 2-point	-0.22/0.19[a] 2-point	-1.93/1.93 2nd order fit	Small bridge single sided -3.9/1.7 2-point	double sided -1.1/1.5 1-point		
Resolution (°C)	0.25[b]	0.3	0.073	0.21	0.88	0.61		0.068[c]
Conversion time (s)	12.5µ	30.5m	8m	4.8	5µ	10µ	10µ	1m
Meas. rate (S/s)[d]	80k	32.8	125	0.208	100k	1	100k	100
Power (W)	36µ	71n	75n	113p[e]	242.9n	174p[f]	488.3n	49.6n
E/conv. (J)	450p	2.16n	600p	542p	2.43p	174p	4.88p	496p
FoM (pJ·°C^2) E/conv.×(Res.)^2	28.13	194.82	3.2	23.92	1.88	64.75	1.82	2.29

[a] ±3σ value, min/max value for the rest [b] Resolution in LSB [c] OSR=100
[d] 1/(conversion time + sleep time) [e] Measured at 20°C [f] Measured at room T (~25°C)

low speed operation (Fig. 8, bottom). According to post-layout simulations, the active power breakdown in the small bridge mode is approximately 51% for the bridge, 48% for the ADC, and 1% for the 1-V clock drivers. For the leakage power, 80% is from the ADC and the remaining is from the clock drivers.

Twelve IC samples from one batch were characterized in a temperature chamber from 0 to 100 °C with a 10 °C step. A 1/3DIN Pt100 sensor is placed close to the chip as a reference. Temperature inaccuracy can be caused by the resistor's nonlinear temperature behavior, the nonlinearity of the bridge, and ADC nonlinearity. In this case, the distortion caused by DAC mismatch is dominant. Besides, due to mismatch of the ADC sampling switches, the sampled DAC voltages V_p and V_n will suffer from a different temperature-dependent signal droop because of leakage. This mismatch increases the gain in one of the single sided modes, but decreases the gain symmetrically in the opposite single sided mode. As a result, 2-point calibration is needed for single sided measurements, while 1-point calibration is sufficient for double sided measurements. On top of that, the signal droop during the conversion also causes ADC distortion, which leads to an inaccuracy of $-3.9/+1.7$ °C and $-2.6/+1.3$ °C for the two single sided measurements (Fig. 9, top). The double sided mode partially compensates the ADC distortion and hence improves the inaccuracy to $-1.1/+1.5$ °C after only a 1-point calibration at 50 °C (Fig. 9, bottom).

IV. CONCLUSION

Table I shows a performance summary and comparison to prior-art [3]–[6]. This letter (small bridge double sided measurement mode) achieves a nominal resolution of 0.61 °C with a conversion time of only 10 μs. It achieves the lowest reported energy/conversion (4.88 pJ at 100 kS/s) and a very low absolute power of 174 pW at 1 S/s. Fig. 10 shows the resolution FoM benchmark of this letter. A very low resolution FoM of 1.82 pJ·°C^2 (at 100 kS/s) is achieved, which is the state-of-the-art among sub-μW temperature sensors. The energy/conversion (4.88 pJ) is almost two orders of magnitude lower than state of the art [3] (450 pJ). Moreover, this is the only low-power design with adaptable power (more than three orders of magnitude) versus speed, resolution, and sensor resistance, and it provides a short conversion time, making it a versatile interface that is suitable for duty-cycled nW-level IoT nodes.

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