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Design and test of analog circuits towards sub-ppm level

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Abstract

Electronics are increasingly being embedded in a growing number of applications in our daily life. This demands strong reliability and robustness of those electronic systems. The IC manufacturing process not being perfect, however, inevitably results in some fabricated parts having defects. Test methods must detect such faulty ICs before shipment. While the fault coverage of testing for digital integrated circuits in industry today already reaches the sub-ppm level, this is not yet the case for analog integrated circuits or the analog part in mixed-signal ICs. This invited talk will review some techniques that are being explored in industrial practice to aim for sub-ppm-level coverage for the analog and mixed-signal circuits as well. This will be illustrated with some practical examples from automotive IC designs.

Summary

The large increase of the number of silicon chips inside modern applications such as cars has created an increasing interest to avoid electronic malfunctions in the field. The current state of the art for complex mixed-signal ICs is of the order of 1 ppm test escapes (see figure 1). Although the number of transistors in the digital core usually outnumbers the number of analog transistors by an order of magnitude, the observed digital test escapes are typically below 100 ppb. The dominant remaining portion of customer returns in industry can therefore be traced back to silicon defects in the analog circuitry that are not caught by the test program today [1].

Fig. 1. Evolution of test escapes in a typical automotive IC [1].

Although the digital core is a dense and large part of a typical mixed-signal IC, a very good quality can be achieved because of the use of a structured test approach with scan insertion and a combination of stuck-at, bridging, I_{ddq} and transitional ATPG patterns. For the analog blocks, industry does not yet fully adopt automated structured approaches, but often still uses functional testing, resulting in lower fault coverage and more test escapes. It has been shown that typical specification testing of analog blocks offers no guarantee to meet the quality requirements, below the ppm level [2,3].

This invited talk highlights the use of structured methods to improve the analog fault coverage and to reduce the number of analog test escapes. The typical structured approach adopts an approach in the lines of the Simulate-Before-Test methodology (see figure 2): the impact of each potential defect in the circuit is simulated based on fault models representing those physical defects; any discrimination between the measured response(s) to the given test stimuli by both the faulty circuit and the fault-free circuit allows to detect the defect during testing. This simulation-based structural approach is however complicated by the lack of an adequate set of fault models, and by the unavoidable presence of process variations.

Fig. 2. Flow of simulation-based structural analog test methodology.

The choice of the proper input test stimuli, the proper selection of the output signals to measure and how, any

targeted (re)configuration of the circuit during testing by means of extra test circuitry (e.g. switches), or the further postprocessing of the measured waveforms, etc. are all design for testability techniques that allow to improve the fault coverage.

As an illustration of a possible structured approach, let us consider a power-on reset circuit with 15 transistors in a high-voltage technology. According to the 6-fault model used, the circuit has 94 possible faults, out of which less than 50% are detectable with typical specification testing. Using targeted test stimuli and applying defect-specific masking on the measured waveforms, the fault coverage can increase significantly [1,4]. For example, figure 3 clearly shows the increase in fault coverage when applying a sinewave excitation (S1, S2 or S3) on the supply voltage and using no/simple/optimized masking on the measured time-domain power-supply current waveform [4]. Similar results have been obtained for other stimuli and measured signals, increasing the fault coverage far above the typical specification testing for this circuit.

Fig. 3. Increase of fault coverage for different maskings applied to the measured waveforms of the power-on reset circuit, for three different test stimuli S1, S2 and S3.

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