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21.1 Mixed-Signal Programmable Non-Linear Interface for Resource-Efficient Multi-Sensor Analytics

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Tremendous progress has been made in reducing ADC power-consumption, yet, in many portable always-awake and multi-sensor systems, the power consumption is dominated by digital backend processing [1] for feature-computation and classification. Recent Analog-to-Information based innovations (see Fig. 21.1.1) have attempted to alleviate this bottleneck by reducing the amount of data streaming into the digital domain: (a) by extracting sensory features in the analog domain [2] and digitizing these instead of the raw-data; and (b) by compressing the data through an analog non-linearity in order to reduce the required digitization word-length [3-5]. Yet, both approaches suffer from limited applicability and design reuse problems, due to (a) their need for highly application-specific building blocks which are not portable across different sensor-signals in multi-sensor platforms; and (b) their need for complex, performance-sensitive analog building blocks which are not portable across silicon technologies. Overcoming the above shortcomings, this work reports a highly programmable non-linear interface that synergistically combines a digitally-computed, application-tunable non-linearity with a 10b binary DAC in an iterative mixed-signal loop (see Fig. 21.1.1 bottom) to enable a compressive analog to non-linear digital transfer-curve. Such configurable non-linear transfer-curve has wide applicability in multi-sensor analytics for feature-extraction, signal-emphasis/-de-emphasis, signal-correction, etc. A 90nm CMOS proof-of-concept illustrates this versatility with 2 very different application mappings, demonstrating (a) Compressive classification: 2× improvement in rms-error for heart-beat classification from muscle noise corrupted ECG signals, along with 50% backend data reduction; and (b) Analog impairment correction : up-to 20dB distortion correction for analog impairments in the sensory chain.

The wide versatility of the mixed-signal interface is enabled by a highly-flexible analog to non-linear-digital transfer-curve (see Fig. 21.1.2). This non-linear transfer-curve enhances the resolution in the input signal's region-of-interest while allowing for a lower resolution outside this region. Such configurable non-uniform representation creates an emphasis on the information content and enables output data-compression. This non-linearity is realized through 3 programmable parameters, (illustrated in Fig. 21.1.2) which control the shape of the non-linearity: (a) ϵ control the finest resolution present in the transfer-curve; (b) α dictates the position of this maximum resolution region; and (c) n_h defines the width of this region. The latter is directly linked to the digital output word-length and hence the data compression ratio. In order to realize this flexible non-linearity efficiently and without large memory (look-up tables) or area overheads, a new iterative mixed-signal digitization scheme is derived, which non-linearly maps an analog input (v_m) to its digital output ($b[1:n_d]$) as:

$$v_{in} = A + B \prod_{i=1}^{n_{it}} W(i)^{b(i)} \quad (1)$$

The parameters A , B and W are precomputed from ϵ , α , n_h using the formulas shown on Fig. 21.1.3. Based on values of ϵ , α and n_h , Eq. (1) enables a wide range of transfer-curves such as logarithmic, exponential, tangent-hyperbolic/its-inverse, etc. (see measurements in Fig. 21.1.4). As an example, for $\alpha \rightarrow 0$ and $\epsilon \ll 1$, Eq. (1) can be simplified to a logarithmic transfer-curve (similar to μ / A -Law) given as:

$$\ln(v_{in}) / \ln(\epsilon) \approx k(1 - \sum_{i=1}^{n_{it}} 2^{-i} b(i)) \quad (2)$$

The iterative search to derive the digital outputs ($b[1:n_d]$) is efficiently implemented through a mixed-signal loop, as illustrated in Fig. 21.1.3, consisting of a standard 10b capacitive binary DAC ($C_{unit} = 10fF$), a dynamic comparator and configurable digital logic. The latter controls the binary DAC with a programmable non-linear mapping scheme as follows: In every iteration i , the digital logic operates in closed loop with the analog to provide the binary threshold for bit $b(i)$ realizing the desired non-linearity (see Fig. 21.1.3). The first iteration compares the sampled analog input (v_m) with the parameter α to select the appropriate set of A , B , W as shown in the table in Fig. 21.1.3. In each remaining iteration, i , bit $b(i)$ is first set to '1' and the DAC control signals $c[9:0]$ are digitally updated as follows:

$$c_i[9:0] = A + B \prod_{j=1}^{i-1} W(j)^{b(j)} W(i)^{b(i)} \quad (3)$$

The subsequent comparator decision then sets or resets $b(i)$. This iterative approximation enables the DAC output to approach the sampled v_m starting from α , with n_h steps and a non-linear step-size controlled by ϵ .

The 90nm CMOS fully dynamic non-linear interface can operate up-to 33kS/s from a 1.2V supply with an input signal swing of 1.8Vppd. Measured transfer-characteristics in Fig. 21.1.4 shows the system's versatility through a logarithmic ($\alpha = 0$, Fig. 21.1.4 top-left) and exponential ($\alpha = 1$, Fig. 21.1.4 top-right) non-linearity for a several settings of n_h and ϵ . The parameter n_h can be set from 5 to 9 (see Fig. 21.1.4 top-left) and enables a trade-off between the data-compression ratio and the width of the high-resolution region, while the parameter ϵ influences the steepness of the curve (see Fig. 21.1.4 top-right), and hence the maximum resolution of the transfer-curve. Different digital non-linearities can also be combined on both sides of the transfer-function ($v_m < / > \alpha$), to enable a hyperbolic tangent (see Fig. 21.1.4 bottom-left) and its inverse (see Fig. 21.1.4 bottom-right) transfer-function, which allows one to focus the high resolution in an application-required region-of-signal-interest through tuning α . The total mixed-signal system power-consumption for the different operation modes and multiple sampling frequencies is highlighted in Fig. 21.1.4. Fig. 21.1.5 illustrates the quantization error for the non-linear transfer-curves of Fig. 21.1.4. The quantization error has a DAC limited 10b minimum at $v_m = \alpha$ and gradually increases away from α to enable a non-linear compressive transfer-characteristic. While only a few combinations of ϵ , α and n_h are shown in Figs. 21.1.4 and 21.1.5, these parameters can be independently tuned to benefit a wide range of applications.

Two applications are mapped to illustrate the system's versatility across sensor interfaces and tasks:

(a) Signal classification using non-linearly compressed data is illustrated through heart-beat detection from muscle noise corrupted ECG signals (Fig. 21.1.6 top). The setup uses MIT-BIH Noise Stress Test database [6], which contains noisy ECG signals with SNR from 24dB to -6dB. Measured results show that the non-linear mixed-signal mapping with $\alpha = 0.8$, $\epsilon = 0.05$ and $n_h = 5$ emphasizes the peaks while suppressing the muscle noise. Compared to a classical linear sensor interface, this reduces the rms error in heart-beat detection by 2× while also reducing the required digital word-length by 50% which decreases the dominant backend digital power by ~50%.

(b) Analog impairment correction of sensory signals is illustrated through front-end amplifier distortion correction (Fig. 21.1.6 bottom). Here, the non-linear interface is used in the inverse-tangent-hyperbolic mode with $\epsilon = 1.1$ and $n_h = 8$ to compensate the tangent-hyperbolic non-linearity of efficient open-loop amplification. Measured results show that the mixed-signal non-linear interface corrects the amplifier distortion from as high as 5% THD (SNDR 25dB) to 0.5% THD (SNDR 46dB) thus eliminating the need for power expensive backend digital calibration/correction.

Figure 21.1.7 highlights the different sections on the die micrograph and compares the reported mixed-signal interface to the state-of-the-art designs. The proposed design uses an iteratively computed digital non-linearity in a mixed-signal loop and hence is the first one to allow complete programmability to match its transfer-characteristics with the varying requirements of multi-sensor applications. This enables a true analog-to-information conversion, while reducing the digital word-length up to 50% at comparable power efficiency with the existing non-flexible implementations. While this work reports two application mappings, the highly configurable non-linear interface is widely applicable to many sensory analytics systems, such as gait/posture-detection from accelerometers, stress/fatigue detection in machine monitoring, etc.

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	Tech.	Non-Linearity	Transfer. Char.	Max. Data Compression	Output Width / Max. Resolution	Power @ Fs Static / Dynamic
This Work	90 nm CMOS	Digital - Programmable Standard Cells	Widely Configurable	50%	Prog. 5 to 10 9.5b	6.3 μ W @ 33 kS/s Dynamic
[3]	0.18 μ m CMOS	Analog. Non-Binary Cap. Array	Fixed - Exponential	25%	Fixed - 8 10.5b	40 μ W @ 25 kS/s Partially - Dynamic
[4]	0.18 μ m CMOS	Analog. Non-Linearly Spaced Vref.	Fixed - Logarithmic	30%	Fixed - 8 13b	2500 μ W @ 22000 kS/s Static
[5]	1.5 μ m BiCMOS	Analog. Diode Non-Linearity	Fixed - Logarithmic	NA	Fixed - 8 8	3 μ W @ 0.3 kS/s Static

Figure 21.1.7: Comparison to state-of-the-art designs and (bottom) Die micrograph highlighting different sections on chip.