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Digital-domain Chopping Technique for High-Resolution PLL-based Sensor Interfaces

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Abstract

Due to their high compatibility with scaled CMOS and emerging technologies, highly-digital time-based architectures, such as PLL-based architectures, have become an attractive alternative to amplitude-based circuits for sensor interfaces, in terms of high time resolution and the potential for low power and area scalability. Although quantization and thermal noise in PLL-based architectures can be addressed by applying noise shaping and oversampling, offset and 1/f noise limit the resolution at high oversampling ratios. Therefore, dynamic offset cancellation techniques such as chopping and autozeroing, as used in traditional amplitude-based circuits, must be adapted to such time-based implementations as well. This paper presents a digital-domain chopping technique suited for offset and 1/f-noise cancellation in applications where medium-to-high-resolution sensor interfaces are needed. System-level simulations demonstrate the benefits of this technique at high oversampling ratios. The resolution improvement is confirmed by measurements, showing the rate of 10dB of SNR gain per decade of oversampling as expected from theory.

Keywords: Sensor interface, Time-based, PLL, Chopping, Highly-digital, 1/f noise, Delta-sigma, CMOS

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1. Introduction

As CMOS technologies with shrinking supply voltage scale to more advanced nodes, the design of robust high-performance analog integrated circuits becomes more challenging. Furthermore, new emerging applications such as the internet of things require smart sensor nodes containing embedded electronics to acquire and exchange data in a networked fashion. This motivates the research of novel circuit topologies compatible with the increasing requirements in terms of low power and area compactness.

Sensor interface circuits are a fundamental building block to condition the sensor signal and convert it to the digital domain. Lately, time-based architectures have become an interesting option for sensor interface integrated circuits due to their compatibility with the technology scaling. In contrast to traditional amplitude-based sensor interfaces, such as the $\Delta\Sigma$ -based [1], [2], [3] and the SAR-based [4], [5], [6] architectures, time-based architectures operate in the time domain. This allows to bypass the noise margin and the dynamic range issues due to the supply voltage scaling [7]. The time-based sensor interfacing concept has been demonstrated in the past using discrete components to build simple and low-cost full sensor systems [8], [9]. More recent works have focused on CMOS implementation of integrated time-based sensor frontends. In [10], an energy-efficient period-modulation-based capacitive-sensor interface allows to extend the input range to manage parasitic capacitances up to 5 times larger than the sensor capacitor. Another example of time-based sensor interface is presented in [11], where a PWM signal representing the sensor value is generated, making it easier to interface to a microcontroller with a synchronized clock. In both examples, the interfaces make use of analog building blocks such as current amplifiers and high-transconductance OTAs. These analog building blocks use several transistors stacked between the supply voltage and the ground, making these architectures less feasible at scaled technologies [12].

This work focuses on PLL-based sensor interface architectures which allow a compact and simple highly-digital time-based implementation. Other bene-

fits inherent to digital circuits have been recently reported, such as robustness towards supply-voltage and temperature variations [13] and the compatibility with emerging technologies [14].

Since the PLL-based sensor interface in [15] resembles a $\Delta\Sigma$ loop (see Fig. 1(b)), oversampling and first-order noise shaping allow to trade off resolution for bandwidth. This has made possible to achieve resolutions of 9 bits and more [13]. Simulations however show that the $1/f$ noise from the oscillators and the bias circuits degrades the resolution performance of the PLL-based sensor interfaces at low bandwidths. This effect limits the maximum resolution that can be achieved by this type of architecture, even for high oversampling ratios. This problem is addressed in this paper.

Different from the traditional implementation of dynamic compensation techniques as used for amplitude-based architectures [16], this paper presents a novel chopping technique for time-domain signals in the PLL-based architectures. This technique offers the advantage of canceling both the DC offset and the $1/f$ noise in PLL-based sensor interfaces, in contrast with techniques presented earlier, which mitigate only the static offset [17]. In addition, this work introduces a modified version of the architecture presented in [15]. The two main advantages of this improved architecture are: 1) the cancellation of the effect of nonlinearity of the oscillators, and 2) the fixed sample rate at the output of the system, as will be discussed.

The paper is organized as follows. Section 2 gives an overview of the PLL-sensor interface operating principle and its most relevant sources of offset and noise. In section 3 the chopping technique is described and the design of the PLL-based sensor interface with chopping circuitry is discussed. The simulation and experimental results are presented in section 4. Finally, section 5 concludes the paper.

2. PLL-based sensor interfaces

2.1. Working principle

60 The PLL-based sensor interface working principle has extensively been described in [15], [13], [18] and will be summarized only briefly here. In Fig. 1(b), the modified PLL-based sensor interface addressed in this work is shown. The discussion is centered around the design of capacitive sensor interfaces, but similar principles can be used for resistive and other sensors [13]. In order to process
65 the physical sensor information in the time domain, the PLL-based sensor interface initially converts the capacitive sensor information to a time-domain signal. This is done by having the capacitive sensor control the period/frequency of a capacitance-controlled oscillator (CCO), CCO_{SENS} . The capacitive sensor is connected in a grounded configuration (i.e. one terminal connected to ground)
70 [19]. In principle, this does not prevent the presented architecture to interface capacitive sensors commonly used in a floating configuration (i.e. none of the terminals is grounded). The grounding of one terminal might even be required by some applications such as low-cost capacitive level measurement of a conductive liquid [20].

75 Once the sensor information is in the time domain, the conversion to the digital domain is done by using a digital phase-locked loop (PLL) with a reference oscillator CCO_{REF} and a phase detector. The latter provides a digital output encoded in a number of binary bits. The feedback loop is closed by digitally controlling the sensor oscillator CCO_{SENS} using a capacitive DAC steered by
80 the phase detector output. The total interfacing process can be understood using the analogy of frequency modulation and demodulation: first, the sensor information is modulated to the frequency domain using CCO_{SENS} , and then the information is recovered in the digital domain after being demodulated by the digital PLL.

85 2.2. Proposed PLL-based architecture with enhanced linearity

The proposed architecture is depicted in Fig. 1(b), while the original architecture reported in [15], [13] is shown in Fig. 1(a). For simplicity, the chopping circuit is not included here. In the original architecture, the locking between the frequencies of CCO_{REF} and CCO_{SENS} makes the operating point of the interface explore a wide range of the characteristic of the CCOs. In practical implementations, the CCOs can be highly nonlinear, reducing the linearity of the whole system. To avoid this, the proposed architecture integrates the sensor C_S in the feedback loop. In this case, the frequency of CCO_{SENS} only fluctuates around the operating point by the minimum quantization element in the phase detector. This frequency variation explores only a small range of the nonlinear CCO characteristic, and thus the output characteristic is linearized. Another advantage of this approach is the fixed output data sample rate due to the constant frequency of CCO_{REF} , saving the re-sampling operation otherwise needed for the digital conversion.

100 In contrast to the second-order PLL-based sensor interface architecture presented in [13], the proposed architecture uses a multi-bit phase detector in the feedback loop. This option allows to have an inherently stable system without degrading the SQNR. The main drawbacks of this approach are the increased complexity and the extra nonlinearity introduced by mismatch between the multiple components/elements of the multi-bit phase detector. Nevertheless, the linearity requirements are relaxed by the noise shaping of the mismatch error in the loop.

The schematic of the multi-bit phase detector implementation in Fig. 2 helps to understand the operation of the system in the time domain. The digital conversion of the signal phase in the CCOs is done using two flash time to digital converters (TDCs), TDC_{REF} and TDC_{SENS} in Fig. 2. The time-domain signals in the phase detector nodes for the case where CCO_{SENS} leads CCO_{REF} are shown in Fig. 3(a). In this case, the signal coming from CCO_{SENS} propagates through the delay elements of TDC_{SENS} into the nodes D_8 to D_{15} . When

115 CCO_{REF} clocks the latches in this example, the three nodes where the signal
 has already propagated set the nodes b_8 to b_{10} at the output of the latches to
 1, and the rest to 0. For TDC_{REF} , since the signal coming from CCO_{REF} has
 not propagated yet, the nodes b_7 to b_0 are set to 1. These signals are inverted
 in polarity and order to express the negative phase with respect to the refer-
 120 ence. This makes the digital output of the phase detector equal to 11. The
 digital output value is fed back through the loop, connecting 11 elements of the
 capacitive DAC to the sensor node. In this way, the frequency of CCO_{SENS} is
 increased to minimize the phase with respect to the reference CCO_{REF} . In Fig.
 3(b), the case where CCO_{SENS} lags CCO_{REF} is shown. In this case, the signal
 125 coming from CCO_{REF} propagates through the delay elements of TDC_{REF} into
 the nodes D_0 to D_7 . Now CCO_{SENS} acts as the latch clock. In this example,
 the nodes b_7 to b_5 at the output of the latches are set to 0 (due to the polarity
 inversion), and the rest to 1. For TDC_{SENS} the nodes b_8 to b_{15} are latched to
 0 since the signal coming from CCO_{SENS} has not propagated yet, yielding an
 130 output equal to 5. Only 5 elements of the capacitive DAC are turned on in this
 case, decreasing the frequency of CCO_{SENS} to reduce the phase. In the locked
 state for a constant sensor value, the digital output toggles between only two
 different values. The time average of this signal represents the sensor value.

2.3. Theoretical and simulated SNR

135 An analytical model has been developed to evaluate the achievable resolution
 performance of the PLL-based sensor interface. The model considers the inher-
 ent structure of the system and the main non-idealities of the building blocks
 involved in the data conversion. Since the main sources of noise in this particular
 structure come from both the quantization operation and the oscillator phase
 140 noise, the SNR is used to evaluate the resolution performance of this system.

The digital output of the PLL-based sensor interface is oversampled to fur-
 ther increase the resolution, taking advantage of the resemblance between this
 architecture and $\Delta\Sigma$ converters [18]. In addition, this converter inherently ben-
 efits from first-order quantization noise shaping. This is due to the integration

145 of the frequency error in the the oscillators and the subsequent quantization in the phase detector. The noise shaping reduces the needed oversampling ratio (OSR), defined as:

$$OSR = \frac{f_s}{2f_{BW}} \quad (1)$$

where f_s is the sampling frequency of the system and f_{BW} is the bandwidth of the input signal of interest, outside which the noise is shaped and digitally
150 filtered. The quantization noise can be expressed as [18]:

$$N_{Q,rms}^2 = \frac{\Delta^2 \pi^2}{12} \frac{1}{3 OSR^3} \quad (2)$$

where Δ is the quantization step. Additionally, the noise contributed by each oscillator can be characterized by the input-referred phase noise spectrum as a function of the frequency f through the following formula:

$$|N_{IRPN}^2(f)| = \frac{|\theta_n^2(f)| f^2}{K_{CCO}^2} \quad (3)$$

where $|N_{IRPN}^2(f)|$ is the power spectral density of the noise signal n_{IRPN} at
155 the input of the CCO, $|\theta_n^2(f)|$ is the phase noise spectrum at the output of the CCO and K_{CCO} is the conversion gain of the CCOs. At a certain offset frequency Δf from the operating frequency, the noise power can be calculated using the phase noise figure $L(\Delta f)$ as follows:

$$|N_{IRPN}^2(\Delta f)| = \frac{L(\Delta f) \Delta f^2}{K_{CCO}^2} \quad (4)$$

Assuming a typically flat input-referred phase noise (i.e. white noise) in a
160 bandwidth f_{BW} , and given that the phase noise is specified as single-side band noise, the rms-power of the noise signal n_{IRPN} can be equated as:

$$n_{IRPN}^2 = 2N_{IRPN}^2(\Delta f) f_{BW} = 2 \frac{L(\Delta f) \Delta f^2}{K_{CCO}^2} f_{BW} \quad (5)$$

The total noise contributed by the two oscillators with identical K_{CCO} can be expressed now in terms of the oversampling ratio defined in equation (1), where the sampling frequency f_s is replaced by the oscillator frequency f_0 :

$$N_{P,rms}^2 = 2n_{IRPN}^2 = 2 \frac{L(\Delta f) \Delta f^2}{K_{CCO}^2} \frac{f_0}{OSR} \quad (6)$$

165 The main factor that limits the SNR of the PLL-based sensor interface in real implementations is the oscillator phase noise [18]. Thus, the total output noise can be approximated by the phase noise coming from the oscillators. Under this assumption, the SNR of the PLL-based sensor interface can be calculated as:

$$SNR[dB] = 10\log\left(\frac{S_{in,rms}}{N_{P,rms}^2}\right) = 10\log\left(\frac{S_{in,rms}^2}{2} \frac{K_{CCO}^2}{L(\Delta f) \Delta f^2 f_0}\right) + 10\log(OSR) \quad (7)$$

where $S_{in,rms}$ is the maximum sensor amplitude. It can be seen that for a fixed
 170 operating frequency f_s , a fixed offset frequency Δf and a constant CCO gain K_{CCO} , the SNR decreases with 10dB per decade of extra phase noise figure $L(\Delta f)$ and increases with 10dB per decade of extra OSR.

The PLL-based sensor interface system has also been modeled using Matlab, and the SNR has been plotted in Fig. 4 for different phase noise and OSR values.
 175 The model ignores the effect of 1/f phase noise. An example using a 4-bit phase detector and two identical CCOs with free-running frequency $f_0 = 10MHz$ and gain $K_{CCO} = 1MHz$ is simulated. The phase noise is calculated at a frequency offset of $\Delta f = 100kHz$. The right side of the plot in Fig. 4 represents the dominant phase noise region, which is approximated by equation (7). The figure
 180 shows that the SNR directly depends on the phase noise in this region. Thus, a low-phase-noise oscillator topology is needed in this architecture.

It can be concluded from Fig. 4 that, in absence of 1/f phase noise, the system can achieve over 14 bits ENOB of resolution. Thus, high-resolution conversion using the PLL-based sensor interface is possible for realistic phase
 185 noise figure values (below $-100dBc/Hz$) and sufficient oversampling ($OSR \geq 50000$). However, it has been observed that the 1/f noise from the oscillators is modulated by the feedback loop to the output of the sensor interface as low-frequency phase noise [18]. This limits the theoretical performance described above at low bandwidths (high OSR). Due to the nonlinear nature of the phase
 190 detector, this process is however difficult to describe analytically, and will be simulated in the subsequent sections.

3. Digital-domain chopping technique

Traditionally, chopping has been used as an open-loop dynamic offset cancellation technique that reduces the effect of low-frequency amplifier imperfections [21]. The technique uses modulation to shift the signal to higher frequencies where there is no effect of DC offset and $1/f$ noise. Then, it demodulates the signal back to the baseband after having passed through the building blocks that introduce the DC and low-frequency disturbance signals. These operations allow to upconvert the unwanted part of the signal, that is filtered in subsequent stages to recover the original signal with reduced DC and low-frequency disturbance. The frequency components that appear at the chopping frequency and its odd harmonics limit the bandwidth of the system. Thus, this technique is suited for low-frequency applications such as sensor interfaces. A drawback of the chopping technique is the residual offset due to non-ideal switches, mainly caused by charge injection, which produces spikes in practical implementations. Different techniques have been proposed which allow to achieve offset levels around 100 nV [22].

It is possible to make an analogy between the effect of $1/f$ noise in time-based and in amplitude-based systems. In the time-based case, the important $1/f$ perturbation is contained in the phase of the oscillator. Thus, some error is introduced when the phase is compared. The measurement of the phase error can easily be reversed by interchanging the position of the oscillators at the input of the phase detector. This means that chopping can also here help to cancel the undesired $1/f$ noise otherwise present at the output, as will now be explained in detail.

3.1. Working principle

Chopping is implemented by introducing upmodulation and downmodulation as shown in Fig. 6. The working principle is explained using the example depicted in Fig. 5. Since $1/f$ noise can be considered as a slowly-varying DC offset, the example considers the particular case of a DC offset between the oscillators.

Fig. 5(a) shows an example of the digital output of the system for a constant capacitive sensor value under the presence of DC offset. The time-domain signal toggles between two values (6 and 7 in this example). The DC offset introduces an error $E_{DCoffset}$ between the average value of the time-domain output signal and the expected value. Fig. 5(b) shows the digital time-domain output signal for the case in which the digital-domain chopping technique is activated. The modulation of the signal of interest is done by interchanging the reference node and the sensor-DAC node at a frequency f_{chop} . The same frequency f_{chop} is used to demodulate the signal at the output of the oscillators. This allows to recover the original signal and to transpose the $1/f$ noise and the DC offset outside the band of interest. As seen in Fig. 5(b), the chopping half period generates a time-domain output toggling between two values (8 and 9 in the example). When averaged in a complete chopping cycle, the error introduced by the DC offset and by the low-frequency noise from the oscillators during the non-chopped half period is compensated for.

A large advantage of the proposed chopping technique is that, due to the inherent digitization, spurious signals at the chopping frequency and its odd harmonics can accurately be filtered out in the digital domain. Furthermore, the chopping spikes can easily be removed in the digital domain, avoiding the residual offset reduction techniques needed in amplitude-based systems.

The selection of the chopping frequency f_{chop} needs to consider the non-idealities introduced by the technique. On the one hand, f_{chop} has to be high enough to avoid that the $1/f$ frequency components fold into the bandwidth of interest. On the other hand, the chopping spikes introduced in each chopping cycle constitute a small source of data loss, that accumulated over several cycles can become significant. Thus, the chopping frequency needs to be low enough to avoid a degradation of the benefits of oversampling.

3.2. Design implementation

As a proof of concept, the technique has been implemented together with a capacitive sensor interface in a test chip. The detailed block diagram of the

implemented circuit is shown in Fig. 6. As explained before, the capacitive sensor and the capacitive DAC that provide the feedback loop are both connected to one of the stages of CCO_{SENS} . The capacitive sensor is emulated using an on-chip capacitive bank that can digitally be set up externally, to provide a controllable testing process. The total sensor capacitance can vary in a range from 250 fF to 8 pF in steps of 250 fF. The DAC consists of an array of 16 capacitive elements digitally controlled by the output of the interface. A reference capacitance sets the free-running frequency of CCO_{REF} . This frequency always needs to be lower than the frequency of CCO_{SENS} , because the feedback loop can only add capacitance and thus lower the frequency of CCO_{SENS} . To ensure that the PLL is locked for every sensor value, the total capacitance in the reference side is composed by the capacitance of a shorted replica of the DAC and an open replica of the sensor bank. This replicates the parasitic capacitances on both CCOs. These blocks were carefully laid out and then positioned to minimize the effect of mismatch.

In addition to the parasitic components previously mentioned, an implementation using an off-chip sensor needs to consider the total offset capacitance at the sensor node. This offset capacitance consists of the sum of the external parasitic capacitance (e.g. on the non-grounded plate of the sensor, the chip bond pad and package, the PCB, etc.) and the base capacitance of the sensor. To emulate the offset capacitance, a 2 pF capacitance has been placed in the sensor node, and copied symmetrically in the reference oscillator to adjust the tuning range of the PLL. In practical implementations, the proposed sensor interface needs to take into account the offset capacitance to provide accurate measurements. This is done through an initial calibration step when the sensor and the interface are connected. The effect of high offset capacitance values, e.g. the parasitic components in long interconnecting cables, can be avoided adapting smart techniques such as the one presented in [19].

The oscillators are implemented using the coupled sawtooth oscillator (CSO) topology [23] with 5 stages. This topology, shown in Fig. 7, is chosen due to its low phase noise performance, at the cost of a relatively higher power con-

sumption [24]. The phase noise in this topology is composed by $1/f^2$ and $1/f^3$ noise coming from input-referred white and $1/f$ noise, respectively. The main source of noise is the perturbation in the bias current generated by the PMOS current source, sized to minimize this effect. The voltage V_{bias} is generated through independent voltage references for each CCO. Its devices have also been sized in accordance to the low phase noise requirement. The stage nodes of both oscillators have been loaded with dummy capacitances C_{dummy} . In order to have balanced signal amplitudes in each node of the CCOs, the value has been set to 2 pF, the same value used to emulate the offset capacitance of the sensor. Additionally, this modified version of the CSO circuit can produce a bias-independent frequency. This is done by using the voltage generated by the bias current passing through resistances R_{ref} in each stage as the comparison reference required to charge and discharge the dummy capacitances C_{dummy} .

The signal is extracted from the third stage from each CCO to provide enough time for the loop to propagate the changes. It is connected through a buffer to a 4-bit phase detector, already presented in Fig. 2. The time-domain output consists of 16 thermometer-coded bit lines used to control the 16 elements of the capacitive DAC. An encoder provides a 4-bit binary output bus.

The up-modulating chopping circuit is implemented using transmission-gate analog switches. The switch transistors are sized optimally to minimize the voltage drop they introduce without adding excessive parasitic capacitance. The down-modulating chopping circuit is placed after the 4-bit phase detector, and not immediately after the oscillators, as shown in Fig. 6. In this way, the signals can be exchanged in the digital domain by simply choosing the positive or the negative outputs of the D-flipflops in the phase detector.

4. Simulation and measurement results

4.1. Simulation results

The system has been simulated at transistor level in Spectre using a standard 0.18 μm CMOS technology PDK. The parameters that represent the nonideali-

ties of the different building blocks have been extracted. The CCOs are designed to have a reference frequency equal to 10 MHz, which provides a good trade off between bandwidth (OSR) and both low noise and low power consumption. The maximum nonlinearity error of the simulated CCO characteristic is 14.8%
315 of the full frequency span. The simulated phase noise at 100 kHz offset is -109.4 dBc/Hz. However, the measured phase noise deviates from the simulated value, as explained in the next section. Thus, the measured phase noise value is used for the simulations.

The extracted CCO parameters are entered into the state-variable-based
320 Matlab model described in [13] to simulate the spectrum of the output. The signal-to-noise ratio in dB units SNR_{dB} can be calculated as the difference between the signal S_{dB} and the noise N_{dB} , both in dB units. For a maximum normalized input signal ($S_{dB} = 0dB$), SNR_{dB} is equal to N_{dB} . The noise level of the system N_{dB} for each frequency can be determined as the power spectral
325 density (PSD) of the output signal for a DC input value. Thus, the signal-to-noise ratio for a specified bandwidth (OSR) can be obtained by integrating the PSD in the frequency band of interest. It must be noted however that this method to calculate the SNR does not consider the non-linearity of the system, since it is derived from a DC input value. The simulated spectrum of the non-
330 chopped system output and the integrated value for each frequency point are depicted in Fig. 8(a). An SNR of only 63.8 dB or 10.3 ENOB is achieved (Fig. 8(a)) due to the presence of $1/f$ noise. The spectrum of the system output with chopping activated is shown in Fig. 8 (b). The digital-domain chopping circuit operates at a frequency $f_{chop} = 25$ kHz. This value represents a good
335 compromise to achieve enough system bandwidth despite the folding frequency components and a neglectable amount of data loss due to the chopping spikes removal. Using the same OSR, the $1/f$ noise is attenuated in the operation bandwidth and the SNR achieved is 83.1 dB or 13.5 ENOB. These system-level simulations demonstrate the feasibility of the presented digital-domain chopping
340 technique. The simulated SNR of the PLL-based sensor interface architecture increases with 3.2 ENOB at an OSR of 50000.

4.2. Measurement results

The PLL-based sensor interface has been prototyped using a standard $0.18\ \mu\text{m}$ CMOS technology. The chip layout and microphotograph are shown in Fig. 9.

345 The circuit has a total active area of $700\ \mu\text{m} \times 1400\ \mu\text{m}$.

Using the internal capacitive bank as a sensor load, the single oscillator characteristic has been extracted for both CCOs by turning off the feedback loop of the system. In Fig. 10(a), the measured and simulated characteristic of the CCOs are shown. The discrepancy is due to parasitic effects not included
350 in the simulations. Additionally, it can be observed that there is an offset in the measured characteristic of both CCOs due to mismatch between the CCO components. The maximum nonlinearity error of the measured characteristic of CCO_{REF} and CCO_{SENS} is 15.3% and 12.1% of the full frequency span, respectively. These values are comparable to the simulated value. In the case of
355 the phase noise, the measured value when the feedback was connected deviated considerable to the value measured in open loop. It could be verified that the toggling of the output introduced extra noise in the oscillators, with a measured value of -95 dBc/Hz. This explains the lower resolution of the system with respect to the predicted values obtained through simulations.

360 The average digital output has been measured and compared to the simulated value for each internal capacitive bank value in Fig. 10(b). The offset error observed is due to the offset between the frequency characteristics of the CCOs. The simulated maximum nonlinearity error achieved is 0.37% of the output span, while the measured maximum nonlinearity error is 0.33% of the
365 output span (without chopping). The simulated case ignores the nonlinearity in the capacitive DAC. Nevertheless, the matching with the measured case proves that this is not a dominant effect for the nonlinearity performance. The inherent linearization of the improved architecture drastically reduces the nonlinearity introduced by the CCOs.

370 Finally, the output data have been extracted for 3 seconds at a constant input value to calculate the Fast Fourier Transform down to sub-hertz bandwidths.

The spectrum of the measured data without chopping is depicted in Fig. 11(a). The results show that the prototype yields an SNR of 66.6 dB or 10.8 ENOB for an OSR of 50000, not far from the simulated value. The spectrum of the
 375 system output when chopping is activated shows an attenuation of $1/f$ noise in the band of interest, as shown in Fig. 11b. The chopping signal is provided as an off-chip chopping square signal with a frequency $f_{chop} = 25$ kHz. For an OSR of 50000, the system now shows an SNR of 79.9 dB or 13.0 ENOB.

These measurements confirm the benefits of this chopping method in terms
 380 of resolution increase, providing 2.2 extra ENOB for an OSR of 50000. The smaller improvement compared to the simulations can be explained by the fact that the continuous toggling of the output signals interferes in the operation of the core circuit. In particular, measurements show that this effect is also present in the phase detector, introducing extra phase noise which is not considered in
 385 the simulated case.

The complete sensor interface consumes a maximum of 1.56 mW from a 1.8-V supply. To allow flexibility during the testing process, the chopping clock signal is provided externally using a microprocessor. A more optimal implementation is to derive the chopping clock directly from the reference clock generated by
 390 CCO_{SENS} using, for example, a digital counter.

In Fig. 12, the SNR of the converted digital output is plotted versus the bandwidth of the system for both the non-chopped and the chopped cases. In the non-chopped case (blue line), one can see that the SNR stops increasing at a rate of 10dB per decade of bandwidth decrease for bandwidths below 1 kHz.
 395 The chopped case (red line) shows how the chopping technique mitigates the effect of the $1/f$ noise. This allows the system to achieve the expected increase rate of the SNR with decreasing bandwidth or increasing OSR (see equation (7)). In the limit case measured, for a bandwidth of 10 Hz, the system can achieve an SNR of 87.8 dB or 14.3 ENOB.

400 5. Conclusions

This paper has presented a digital-domain chopping technique suited for PLL-based time-domain sensor interfaces. Oversampling and first-order noise shaping are used in combination with the chopping technique to increase the resolution of the sensor interface at low bandwidths, where otherwise $1/f$ noise would level
405 off the 10dB-per-decade slope derived theoretically. Full system simulations validate the benefits in $1/f$ noise cancellation due to this chopping technique. The circuit has been prototyped in $0.18\ \mu\text{m}$ CMOS technology. The technique shows a measured improvement with 2.2 ENOB at 100 Hz bandwidth ($\text{OSR} = 50000$) compared to the non-chopped case. This results in a final SNR of
410 79.9 dB or 13.0 ENOB. For lower bandwidths down to 10 Hz the interface may obtain a resolution up to 14.3 ENOB. This makes the circuit architecture suitable for applications where the combination of area scalability, low power and medium-to-high resolution is required.

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Figure 1: (a) Architecture of the original PLL-based architecture [15], [13] for capacitive sensors with a multi-bit phase detector, and (b) the proposed architecture with enhanced linearity.

Figure 2: The phase detector is based on two flash TDCs used to detect either the lagging or the leading phase of the sensor oscillator with respect to the reference oscillator.

(a)

(b)

Figure 3: The operation of the phase detector is illustrated through two examples: (a) for the case where CCO_{SENS} leads CCO_{REF} and (b) for the case where CCO_{SENS} lags CCO_{REF} . The binary output for each case is included in each corresponding table in the figure.

Figure 4: The plot shows a sweep of the sensor interface system SNR (for the multi-bit phase detector implementation, using 4 bits) over different phase noise values, for different oversampling ratio values. A dominant phase noise region where practical implementations are situated can be clearly identified, as derived from the theoretical analysis.

Figure 5: (a) The digital output for the case when DC offset exists between the oscillators generates an average output value that deviates from the expected result. (b) The value of the chopped digital output is restored to the expected value when averaged through one complete chopping cycle.

Figure 6: The full PLL-based sensor interface implemented in the test chip includes two coupled sawtooth CCOs buffered into a multi-bit flash TDC phase detector, the output of which is used to control the state of the switches in the capacitive DAC. The DAC is connected in parallel to the sensor, and implemented as a capacitor array for controlability, into a node of the sensor CCO to generate the feedback structure.

Figure 7: Schematic of the implemented 5-stage coupled-sawtooth oscillator.

Figure 8: (a) The spectrum of the output simulated using the Matlab state-variable-based model for non-chopped operation with 100 Hz bandwidth reveals how the $1/f$ noise limits the SNR that can be achieved, even for high OSR values. (b) The simulated spectrum of the output in the chopped sensor interface case with 100 Hz bandwidth and $f_{chop} = 25$ kHz shows an increase of 3.2 bits of resolution.

Figure 9: (a) Layout plot and (b) microphotograph of the implemented test chip, showing the area of the oscillators, capacitive DAC and phase detector. The circuit has a total active area of $700 \mu m \times 1400 \mu m$.

Figure 10: (a) Measured versus simulated characteristic of the CCOs and (b) measured versus simulated characteristic of the full system. The proposed architecture compensates the sensor-to-frequency conversion nonlinearity, achieving a measured maximum nonlinearity error of 0.33% of the full output span.

Figure 11: (a) For the non-chopped case, the spectrum of the measured output with 100 Hz bandwidth reveals how the $1/f$ noise limits the SNR at low frequency/high OSR values. (b) The spectrum of the measured output in the chopped case with 100 Hz bandwidth and $f_{chop} = 25$ kHz shows an increase of 2.2 bits of resolution.

Figure 12: The measured SNR versus bandwidth plot reveals how the characteristic saturates with increasing OSR in the non-chopped case (blue line). In the case when chopping is active (red line), the characteristic shows the expected 10dB-per-decade rate.