Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies

Georges Gielen, *Fellow, IEEE,* Jelle Van Rethy, Jorge Marin, Max M. Shulaker, Gage Hills
H.-S Philip Wong, *Fellow, IEEE,* and Subhasish Mitra, *Fellow, IEEE*

***Abstract*—The evolution of electronics towards compact and highly energy-efficient systems requires joint efforts in developing both innovative system architectures and novel devices. Recent developments show that time-based sensor interfaces yield highly-digital architectures, which are compatible with advanced silicon CMOS at highly-scaled technology nodes. Advancements in CMOS time-based sensor interfaces show that new circuit techniques can help to increase performance and robustness. Furthermore, these architectures have successfully been implemented in carbon nanotube technology, a promising technology to further reduce the energy consumption in electronics. In addition, CNTs are excellent candidates to be functionalized as sensors, and can potentially improve the energy efficiency of sensors and sensor interfaces for future autonomy-demanding applications. This paper presents an overview of time-based sensor interfaces implemented in CMOS and CNT technologies, allowing for scalable and robust designs. Several CMOS and VLSI-compatible CNFET-based sensor interface circuits have been fabricated and validated through measurements, demonstrating the feasibility of these solutions.**

***Index Terms*—Carbon nanotube (CNT), carbon nanotube FET (CNFET), CMOS, scaling, VLSI, interface circuit, BBPLL, time-based.**

I. Introduction

IN an evolving world where the physical reality is becoming invisibly interwoven with electronics to provide a better quality of life in aspects such as health monitoring, energy savings, product quality control, catastrophe surveillance, environmental pollution measurements and many others, sensor systems are becoming increasingly important. In such scenario, networked sensor systems need to interface the analog physical world and the digital cyber world with a very limited power budget, making energy efficiency a central target for optimization. Other expected properties of these systems are compact size and low cost, while maintaining a good resolution and robustness. One approach to improve the energy efficiency of electronic circuits is to use innovative circuit architectures and techniques. An example of energy-efficient architectures is the bang-bang phase-locked loop (BBPLL)-based sensor interface presented in [1]. The time-based architecture makes highly-digital implementations feasible, which results in low-voltage, low-power and technology-scalable designs, yielding compact and cheap systems with a high energy efficiency. A complementary approach is to leverage emerging nanotechnologies which promise an increased energy efficiency beyond current silicon-based electronics. In this regard, carbon nanotube (CNT) technology is among possible others an excellent candidate for energy reduction in electronics. Carbon nanotube field-effect transistors (CNFETs)-based digital circuits (see Fig. 1) are projected to achieve an order of magnitude improvement in energy-delay product compared to silicon CMOS at highly-scaled technology nodes [2]. This is beneficial in digitally-dominated electronic circuits, such as the highly-digital BBPLL-based architecture [1]. In addition, due to their unique and remarkable electrical, chemical, mechanical and structural properties, CNTs are an ideal material to be functionalized as sensor [3], [4]. Ultimately, the integration of both CNT-based sensors and CNFET-based circuits could be the next major leap towards extremely-energy-efficient integrated sensors and sensor interfaces.

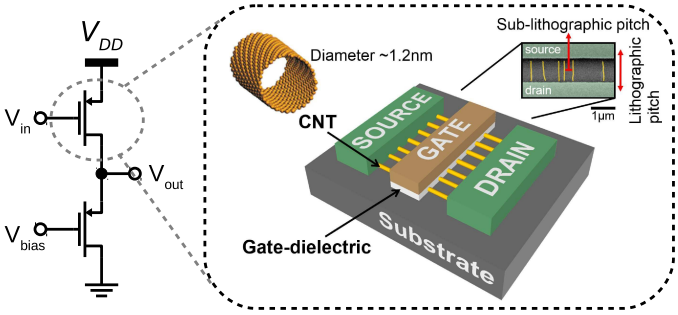


Fig. 1: A CNFET-based pMOS-only inverter and a schematic view of a single CNFET. The scanning electron microscopy image shows the source, the drain and the channel region of a CNFET.

This paper presents various sensor interface chip implementations in both CMOS and CNT technology. Although the sensor interface implementations reviewed in this work are targeted for general-purpose applications, the demonstrator designs take into account typical specification values for state-of-the-art sensors. In the case of the acquisition time/bandwidth, the typical range considered for sensor applications goes from Hz to a few kHz, while the resolution can range from low-resolution applications (8-10 bits) to medium-to-high resolutions, 14 bits and higher. In the latter case, oversampling and noise shaping can help to trade off the bandwidth for increased resolution. In the case of CMOS implementations, the work is focused on innovative architectures and techniques which

G. Gielen, J. Van Rethy and J. Marin are with KU Leuven, B-3001 Leuven, Belgium (e-mail: Georges.Gielen@esat.kuleuven.be; Jelle.VanRethy@esat.kuleuven.be, Jorge.Marinn@esat.kuleuven.be).

M.M. Shulaker, G. Hills, H.-S. P Wong and S. Mitra are with Stanford University, Stanford, CA 94305 USA (e-mail: maxms@stanford.edu; ghills@stanford.edu; hspwong@stanford.edu; subh@stanford.edu).

Manuscript received October 5, 2015; revised January 14, 2016.

TABLE I: Comparison of published CMOS amplitude-based and time-based sensor interfaces

	ISSCC '12 [5]	**JSSC '13 [6]**	**ISSCC '14 [7]**	**ESSCIRC '11 [8]**	**JSSC '13 [9]**
Technology	350 nm	160 nm	180 nm	130 nm	130 nm
Type	amplitude-based	amplitude-based	amplitude-based	time-based	time-based
FOM [pJ/conv]	1.95	1.36	0.447	2.1	13.3
Area [mm^2]	2.6	0.28	0.49	0.0725	0.207

explore the advantages of highly-digital implementations, including scalability, low operation voltages [8], robustness [9] and the option of easily embedding digitally-assisting circuits to improve the performance [10], [11]. On the other hand, the CNT technology implementations explore the feasibility of combination the advantages of time-based sensor interfaces, which are implemented in a digital manner, with a promising nanotechnology. A robust digital-circuit implementation, in combination with VLSI-compatible CNFET fabrication techniques, has resulted in the successful demonstration of two sensor interfaces in CNT technology [12], [13]. The focus in this paper is on the time-based, fully-digital circuit topologies, rather than on the CNT technology. Moreover, since the work reviewed comprises the first-ever presented full sensing system fabricated in CNT technology, the importance of the results discussed lies in the feasibility of implementing time-based sensor interfaces using this emerging technology, rather than the actual performance achieved, which of course will improve drastically with technological progress. For more details on the technology and fabrication side, the authors refer to [12], [13].

The paper is organized as follows. In section II a short overview of the sensor interface architectures is given, while section III pinpoints the current developments achieved in CMOS technology. Measurement results are provided, and digitally-assisted techniques for increasing conversion resolution are discussed. Section IV details the CNT demonstrations. The experimental CNT technology used is pMOS-only, which results in additional design constraints. Additionally, this section also discusses the experimental measurement results of the CNT implementations. Finally, section V concludes the paper.

II. Overview of time-based sensor interfaces

Time-based signal processing has received increasing attention due to the ability to implement the hardware in a highly digital manner. As a result, the hardware can benefit from the increased timing resolution, the reduced supply voltage and the decrease in footprint attributed to smaller technology nodes. In addition, digital circuitry tends to be more robust towards supply-voltage and temperature variations. Therefore, the proposed time-based architectures are based on processing the sensor information in the time/frequency domain, rather than in the voltage amplitude domain.

In order to process physical sensor information in the time domain, the sensor information initially needs to be converted to the time domain. In the proposed architectures, the sensor value is converted to a frequency/period-modulated signal by a sensor-controlled oscillator (SCO) (see Fig. 2). By controlling the period/frequency of the oscillator with a sensor (capacitive or resistive), the sensor information is incorporated in the

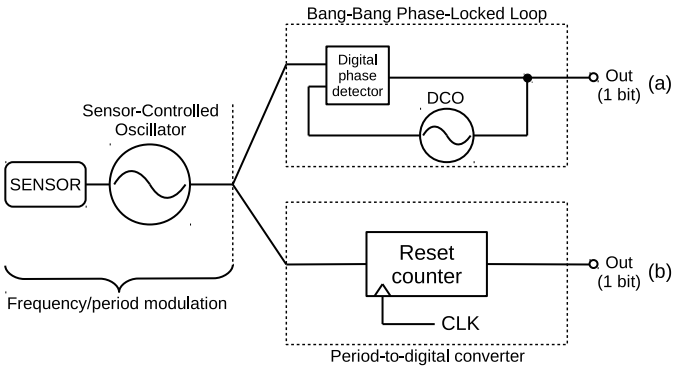


Fig. 2: Block diagram of the architecture of the presented sensor interfaces. (a) Proposed sensor-to-digital interface circuit, in which the demodulation is based on a digital phase-locked loop. (b) Proposed sensor-to-digital interface circuit, in which the conversion is based on a simple set-reset counter to do the digitization.

frequency/time domain. Once the sensor information is in the time domain, it needs to be converted to the digital domain to complete the sensor-to-digital conversion chain. In the first proposed architecture, this is done by using a digital phase-locked loop with a digitally-controlled oscillator (DCO) in the feedback loop [12]. The architecture is depicted in Fig. 2a: it can be seen that the total interfacing chain resembles frequency modulation and demodulation, while only using two oscillators and a simple digital single-bit phase detector. The single-bit output is oversampled, as in $\Delta\Sigma$ converters, to increase the resolution. In addition, due to the intrinsic integration integration in the oscillators, this converter also benefits from first-order quantization noise shaping, which significantly reduces the needed oversampling ratio (OSR) [1]. The OSR is defined as:

$$OSR = \frac{f_s}{2f_b} \tag{1}$$

where f_s is the sampling frequency of the system and f_b is the bandwidth of the signal of interest, outside which the noise is shaped and filtered.

A more straightforward architecture involves a set-reset counter to perform the digitization of the period-modulated signal [13] (see Fig. 2b). While this architecture is open loop, it also benefits from first-order quantization noise shaping and oversampling, identically to the BBPLL and the VCO-based quantizers [14]. The closed-loop PLL-based architecture in Fig. 2a also benefits from increased common-mode suppression of supply-voltage and temperature variations [9], while the open-loop variant is more susceptible to these variations.

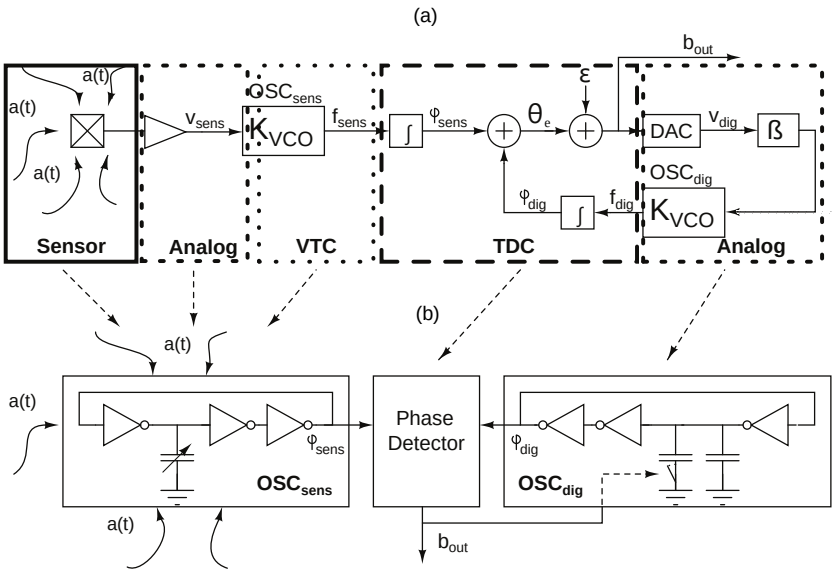


Fig. 3: On top (a), a schematic overview of the PLL system is given as it is described in [3]. The different zones, mentioned in Fig. 1a, are highlighted. The bottom schematic (b) displays the proposed, adapted configuration of the PLL-based converter where the sensor is directly integrated in the oscillator and analog processing is avoided.

This is a major advantage of the closed-loop implementation. Both architectures however can be implemented in a highly-digital manner, as will be shown in the following sections.

To illustrate the benefit of time-based sensor interface architectures in terms of area compactness and scalability, Table I compares the CMOS time-based designs in [8] and [9] with some published amplitude-based solutions [5], [6], [7]. For a similar FOM value (as defined in [15]), the time-based architectures have a smaller area compared to the amplitude-based cases, with the additional advantage of being technology scalable due to the highly-digital implementation.

III. Time-based sensor interfaces in CMOS technology

Due to its simplicity and robustness in the design phase, standard CMOS technology has been used to demonstrate the feasibility of the basic principles of the time-based sensor interface architecture. In this section, two sensor interface chip implementations in CMOS technology will be presented. The first circuit shows a complete functional sensor interface operating at 0.3V with a power consumption of only 270 nW. This interface is suited for applications with a very limited power consumption budget. The second implementation consists of a time-based Wheatstone-bridge interface with a high supply-noise and temperature drift resilience. This implemented circuit shows a PSRR of 52 dB for noise amplitudes up to +10 dB_{FS} . This type of architecture can be used in applications in which the operation conditions prevent to guarantee stability in voltage references and operation temperatures.

A. CMOS chip implementation details

The implementation of the two designs is done in UMC 130-nm CMOS technology, compatible with applications where great robustness is required, such as automotive sensor systems. These implementations are intended to validate sensor interfaces that are suitable for future autonomous wireless sensor applications, mainly focusing on three aspects: low power consumption, robustness and small area/low cost.

The first chip implementation consists of a BBPLL-based capacitive sensor interface, implemented in a fully-digital fashion. The interface is designed taking into account two principles which allow to benefit from the digital world: (a) direct sensor-to-frequency conversion to reduce the influence of noise and to process the information in a digital way, and (b) the use of feedback to relax the constraints in the different building blocks.

The block diagram of this system is shown in Fig. 3 (a), and illustrates the processing flow in the signal path. A capacitive sensor converts the physical quantity $a(t)$ to be sensed into a variable capacitance value. This capacitive sensor value is then directly converted to the time domain using a SCO (OSC_{sens} in Fig. 3 (a)) which creates a sensor dependent frequency f_{sens}. As explained before, the first step to convert to the digital domain is done by using a DCO (OSC_{dig} in Fig. 3 (a)) for demodulation. The steering signal b_{out}, needed to lock OSC_{dig} to OSC_{sens}, is a representation of the phase difference between the two oscillators. A binary phase detector is used to generate the signal b_{out}, which only provides two possible values, depending on if the output signal of OSC_{sens} leads or lags the one of OSC_{dig}. The output train of pulses

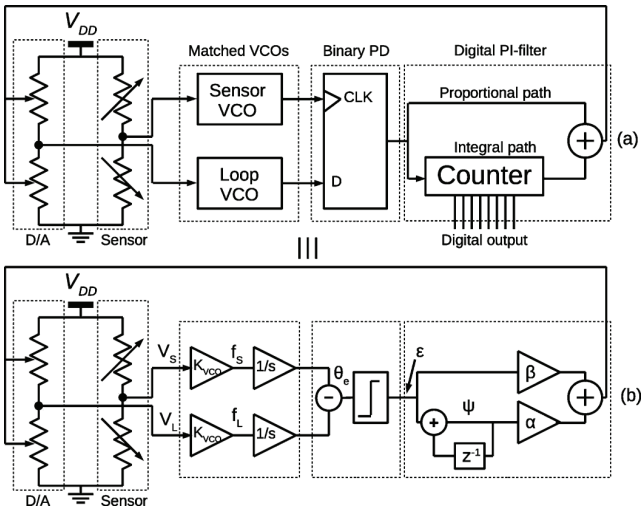


Fig. 4: Time-based architecture of (a) the BBPLL-based force-balanced Wheatstone-bridge resistive sensor interface and (b) equivalent block diagram.

due to this continuous comparison and adjustment process is a single-bit oversampled time representation of the sensor value.

An overview of the actual schematic of the implemented system is depicted in Fig. 3 (b); the relationship to the block diagram is established. The SCO and the DCO are implemented as ring oscillators, due to their highly-digital nature, low power and capability of being able to run at a lower supply voltage compared to differential relaxation oscillators. As a drawback, this oscillator topology has a lower noise immunity. The phase detector is implemented using a D-flipflop, which is a very simple digital block that also can operate at low voltages in a robust way.

The second CMOS sensor interface implementation consists of a supply-noise-resilient BBPLL-based resistive sensor interface, suited for modern applications where for instance EMI, digital switching and supply noise can degrade the performance of sensor-to-digital systems. This implementation demonstrates how the proposed BBPLL-based architecture can easily be adapted to applications in the field of autonomous sensor systems, while the reduced headroom in modern CMOS technologies makes supply noise and interference a big issue, due to the fact that power-hungry regulators need to be avoided. This implementation focuses on achieving both a high PSRR figure and a high resilience to temperature drift, which is also a matter of concern due to the wide range of applications in which sensor networks are used nowadays.

Fig. 4a depicts the circuit schematic of the implementation, based on a second-order BBPLL architecture. The implementation consists of two matched VCOs, a binary phase detector (implemented as a simple D-flipflop) and a digital PI-filter, which consists of a proportional and an integral path (implemented with a digital counter). The matched VCOs are implemented using the Maneatis oscillator [16], which provides a high supply- and substrate-noise rejection, and a large supply-voltage range. To obtain a high PSRR at all times, a force-balancing mechanism is employed to always force the Wheatstone bridge to its balanced position, where the supply noise is fully rejected. This is done by measuring the voltage difference between the two branches and actuating one branch of the Wheatstone bridge via a feedback loop to balance the bridge (which also means that only one branch can be used to incorporate the sensing elements). Due to this feedback mechanism, the sensor-to-digital conversion is done inherently.

An equivalent block diagram of the architecture is shown in Fig. 4b. The input frequency f_S is a representation of the sensor signal V_S, and the frequency of the loop VCO, f_L, results from the voltage generated by the actuated branch, controlled by the filtered output of the phase detector. As in the previous design, the locking condition ensures that the control signal at the output of the digital PI-filter is a digital representation of the sensor value.

B. CMOS chip measurement results

The functionality and performance of both CMOS chip designs presented above are now discussed. The first design is measured using a sealed container and an external reference pressure sensor. The quiescent frequency for this implementation is 825 kHz at at 300 mV supply voltage. For an acquisition time of 1 ms, this results in an OSR of 825. While the total power consumption is 270 nW for the entire interface, the Effective Number Of Bits (ENOB) is 6.1 bits. The input/output characteristic is displayed in Fig. 5. The FOM is 2.1 pJ/conv, and the active area of the implementation is only 0.0725 mm^2. This design demonstrates the low-supply-voltage capability of the BBPLL-based sensor interface architecture, together with the resulting low power consumption. Additionally, the area of the fabricated chip is extremely compact and scalable with technology due to the highly-digital implementation, which has a big impact in cost. These properties make the BBPLL-based sensor interface architecture a promising alternative for high-volume low-power wireless sensor network applications.

The second implementation has been prototyped in UMC130 CMOS technology (Fig. 6). A 10 kΩ potentiometer is used to emulate the resistive sensor, allowing to have a better control of the input of the sensor interface for good testability. With f_{sample} = 10 MHz (the resample frequency of the decimator) and OSR = 500, the SNR is measured to be 64.44 dB and the SNDR 55.46 dB for a bandwidth of 10 kHz, resulting in 10.4 bits of resolution and 8.9 bits of linearity. The complete sensor interface consumes maximum 124.5 μW from a 1-V dc supply. Regarding the performance as a function of the power supply, Fig. 7 shows the PSRR as a function of the supply-noise amplitude at 1 kHz and as a function of the frequency at 20 dB noise amplitude. The noise is only analyzed in the in-band frequency spectrum, since higher frequencies are filtered out digitally by the subsequent decimation filter. A noise-frequency-independent PSRR of 52 dB on average is measured, which corresponds to simulations. This is an improvement of 26 dB over the simulated Wheatstone bridge with ideal ADC. In addition, noise amplitudes up to +10 dB_{FS} are tolerated, which corresponds to a tolerance of 300 mV noise on a 1-V dc supply voltage, even though the absolute oscillation frequency changes hugely. The supply-noise-resilient sensor interface design demonstrates that the

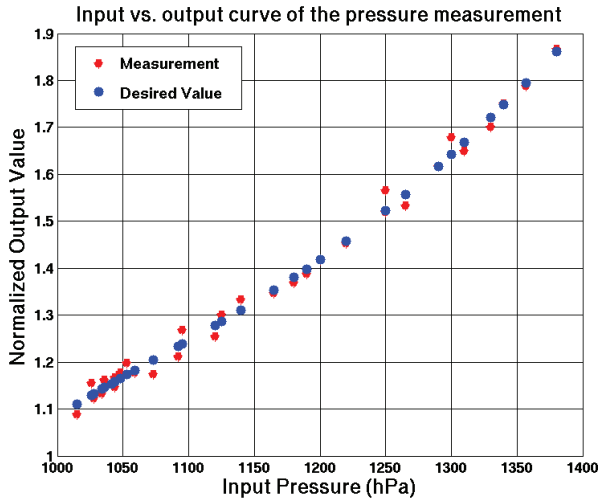


Fig. 5: Results for the pressure measurement from 1018 hPa to 1380 hPa. The measurement curve contains the measured values where an ENOB of 6.1 bits is obtained. The other curve corresponds to the desired curve. The nonlinearity is due to the nonlinear characteristic of the sensor.

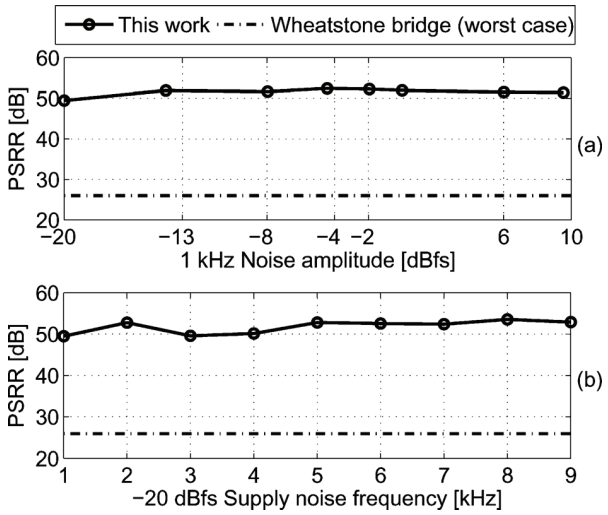


Fig. 7: (a) Measured PSRR as a function of -20 to 10-dB 1-kHz supply noise added to the DC supply voltage. (b) Measured PSRR as a function of 20-dB , 1-9 kHz added supply noise. Both measurements are compared with the worst case simulated results of the Wheatstone bridge of Fig. 1a and b.

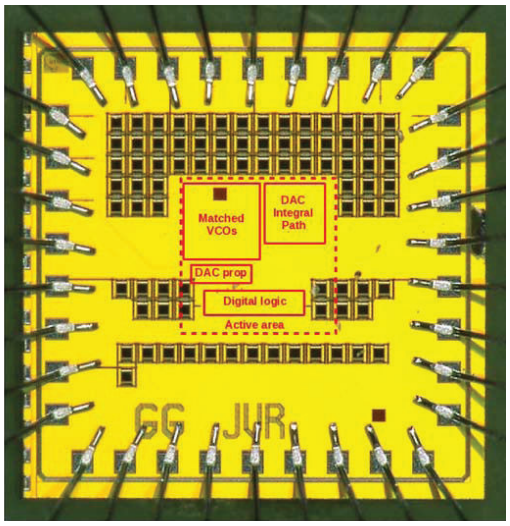


Fig. 6: Microphotograph of the bonded chip prototyped in UMC130 CMOS technology. The active area of 455μm x 435μm is indicated with a dashed box.

BBPLL-based architecture is suitable for applications where the supply voltage is not stable, such as very compact sensor nodes in which the reduced power budget makes the use of power-hungry voltage regulators unfeasible. On the other hand, the demonstration of the temperature-resilient property makes the BBPLL-based sensor interface architecture suitable for applications such as harsh-environment sensor systems.

C. Digitally-assisted technique for high-performance CMOS sensor interfaces

More and more, current applications in both industrial and civil context require sensor systems with resolutions higher than 14 bits. As seen previously, the resolution of the implemented BBPLL-based sensor interfaces has a limited performance in terms of SNR (ENOB), where the VCO phase noise is the dominant source of resolution performance degradation. Phase noise has been a dominant factor in the first CMOS implementation, due to the fact that the design was focused on power efficiency, which is in conflict with low phase noise for the VCOs. In the second CMOS implementation, the VCO topology used has high supply- and substrate-noise rejection capabilities, which provides 4.3 ENOB more in resolution, but still below the requirements needed in high-performance applications. To improve the phase noise performance, it is possible to find VCO topologies with acceptable power consumption and $1/f^2$ phase noise around or above -120 dBc/Hz calculated at an offset Δf = 100 kHz for a free-running frequency f_0 = 10 MHz, such as the one described in [17]. On the other hand, since the proposed architecture resembles a $\Delta\Sigma$ modulator, the quantization noise can be removed from the band of interest by noise shaping and oversampling, trading off resolution for bandwidth. However, test chip measurements show that for high oversampling rates/low bandwidths, the performance then becomes degraded by the 1/f noise from the oscillators and the bias circuits. In [10], a digital-domain chopping technique is presented for time-domain signals in PLL-based architectures to reduce the effect of the offset and 1/f noise produced by the oscillators, as shown in Fig. 8. To do this, first the reference node and the sensor-DAC node are interchanged at a frequency f_{chop} to upconvert the signal of interest. Next, the signal at the output side of the oscillators is chopped at the frequency f_{chop} to recover the original signal and to push the 1/f noise and the DC offset outside of the band of interest. As seen in Fig. 8, a multi-bit phase detector with 4 bits is used, which allows to have a smaller detection granularity, increasing the

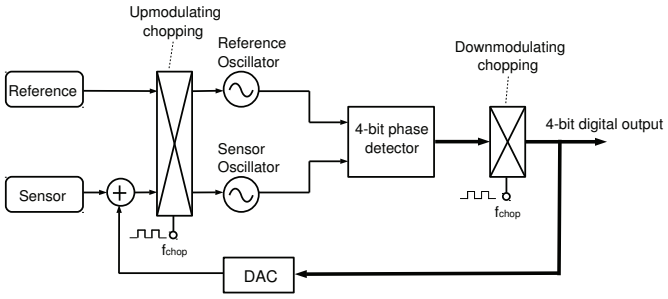
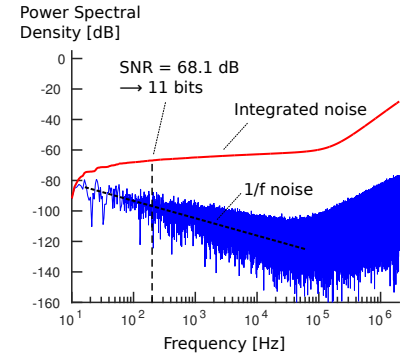


Fig. 8: The highly-digital, PLL-based sensor interface architecture compensates the sensor-induced changes on the same oscillator where the sensor is connected to, to achieve a high linearity. It outputs a 4-bit binary digital signal that represents the value of the sensor.

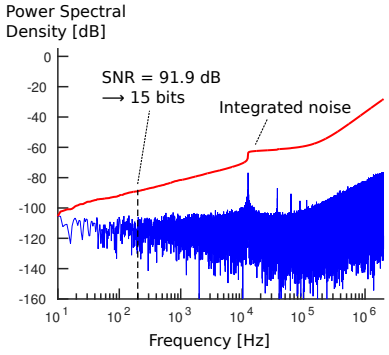
SQNR of the system [1]. In Fig. 9, the simulations using the model developed in [1] are shown. For an oversampling ratio of 5000 (and thus a bandwidth of 200 Hz for a reference operation frequency of 10 MHz), an SNR of only 68.1 dB or 11 ENOB is achieved (Fig. 9a). Using chopping, the 1/f noise is attenuated in the operation bandwidth and the SNR achieved is 91.9 dB or 15 bits ENOB (Fig. 9b). This demonstrates that the digital-domain chopping technique can increase the SNR of PLL-based sensor interface architectures with up to 4 bits, making the architecture suitable for applications in which the combination of area scalability, low power and medium-to-high resolution is required.

Another source of impairment for the BBPLL-based sensor interface is offset, due to the fact that sensor signals are very small compared to the possible values of offset. Additionally, the second CMOS design reviewed requires very good matching between the VCOs to have a high PSRR. Thus, the digital-domain chopping technique can also help in the reduction of offset between the VCOs. An alternative approach, the dynamic offset cancellation for PLL-based sensor interfaces, has been presented in [11]. This technique is based on trimmable VCO stages to externally compensate for any variations (including transistor mismatch, temperature and stress) that may affect the voltage-to-frequency characteristic of the oscillators. Using a 4-bit trimming circuit, the technique can reduce offsets from 10% down to around 0.5%, overcoming the negative effect of variations.

The techniques discussed above in CMOS technology make it possible to use the BBPLL-based architecture in different contexts, including medium-to-high-resolution applications. Since they are based on digitally-assisting circuits, their principles are compatible with highly scaled technologies, and thus they enable extended performance in implementations with highly-scaled CMOS technologies or even new emerging nanotechnologies such as CNTs.



(a)



(b)

Fig. 9: (a) The spectrum of the output for non-chopped operation with 200 Hz bandwidth reveals how the 1/f noise limits the SNR that can be achieved, even for high oversampling rates. (b) The spectrum of the output in the chopped sensor interface case with 200 Hz bandwidth and f_{chop} = 25 kHz shows an increase of 4 bits of resolution due to chopping.

IV. Time-based sensor interfaces in CNT technology

Low-power applications, such as wireless sensing, are becoming increasingly demanding in terms of minimizing the energy consumption while increasing the performance, motivating the search for alternative energy-efficient technologies. In this search we look for a technology with a steep subthreshold slope and a decent current drive. The steep subthreshold slope means that the supply voltage can be reduced further, while having the leakage power minimized and under control. As a result of the supply-voltage scaling, the power consumption decreases. In this sense, carbon nanotubes - among possible other nanotechnologies - are a very promising material due to their excellent electrical, thermal, and physical properties. CNTs can be used to form CNT field-effect transistors (CNFETs) which, owing to their ultra-thin body diameter of $\sim$1 nm, exhibit excellent electrostatic control and simultaneously a high mobility [18], [19]. Experimental results have shown that, at highly-scaled nodes (9-nm channel length and below), CNFETs can outperform FINFETs and Si-nanowires, providing the best current density at a low operating voltage of 0.5 V [20]. Due to such device-level improvements, CNFET circuits are projected to outperform current Si CMOS circuits by over an order of magnitude improvement in energy-delay

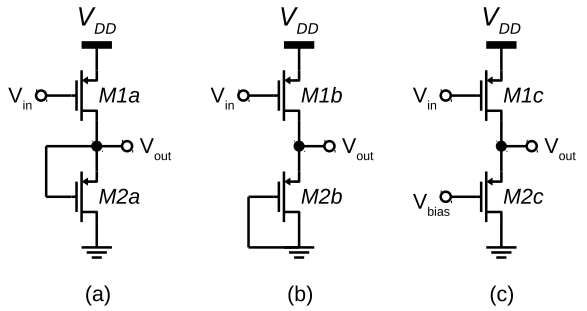


Fig. 10: PMOS-only inverter with the transistor *M1* being the driver and the transistor *M2* being the load: (a) zero-V_{GS} load, (b) diode-connected load, (c) biased load.

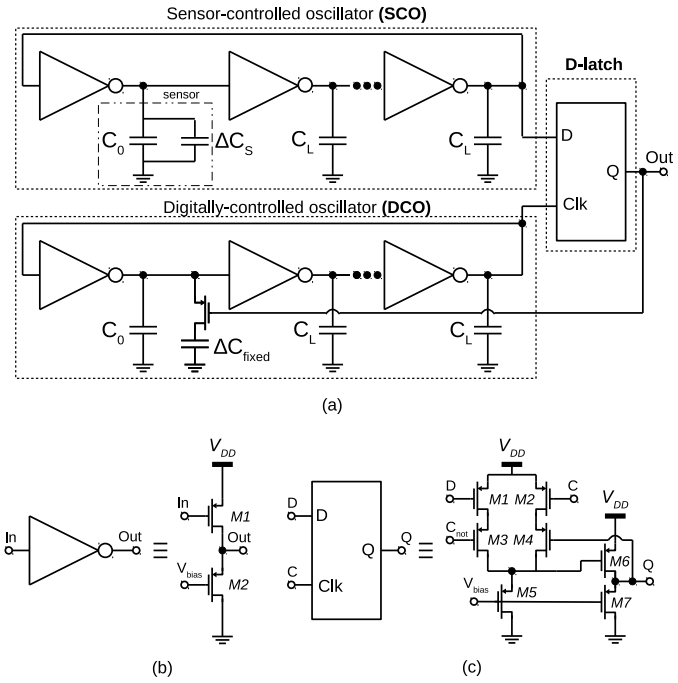


Fig. 11: First presented CNT design: circuit implementation of the capacitive BBPLL-based sensor interface in CNT technology. (a) System implementation, (b) inverter implementation and (c) D-flipflop implementation.

product at highly-scaled technology nodes [20].

A key advance which enabled the experimental demonstrations of CNT-based circuit implementations is the recent progress in fabricating CNT circuits in a VLSI-compatible manner [12]. This fabrication capability is enabled by the imperfection-immune paradigm, a unique combination of design techniques, such as mispositioned CNT-immune design, and processing techniques, such as VLSI-compatible metallic CNT removal. In addition, future developments could lead to CNT circuits and CMOS circuits to be integrated by stacking chips or by growing CNT layers on top of CMOS structures. Alternatively, the first demonstration of a basic CNT computer based on state-of-the-art CNT technology techniques has also been demonstrated recently [21]. This indicates that entire systems including both sensor interfaces and digital processing circuits may be implemented in CNT technology in the future, if the performance and the scaling properties become superior to CMOS.

In combination with digital-oriented architectures such as the time-based sensor interface from the previous section demonstrated in CMOS technology, the time-based sensor interfaces have also fully been fabricated in CNT technology. In addition, it has experimentally been demonstrated that these techniques can scale to aggressively scaled technology nodes [13], without limiting their functionality. This has enabled the design of a sensor interface in a 32-nm CNT technology [13], which will be presented below.

The designs presented here are implemented using an experimental pMOS-only CNT technology. While pMOS-only conflicts with energy-efficient designs, it is not a fundamental issue in CNT technology, as there are several experimental demonstrations of fully-complementary CNFET circuits [22], [23]. For pMOS-only circuits, several configurations can be used to form an inverter, which is the basic building block used to implement the time-based CNT interfaces. Since depletion transistors are not available in the technology used (Fig. 10a), and a diode-connected load does not provide tunability and limits the voltage swing (Fig. 10b), the inverters are implemented with a biased load. The configuration can be seen in Fig. 10c. To ensure sufficient voltage gain and voltage swing in the inverter, the ratio of the width of the driver transistor ($M1c$) to the load transistor ($M2c$) is chosen to be 10:1 for each inverter. In addition, V_{bias} offers some tuneability to compensate for technology variations. But it is emphasized that only one single bias voltage is used for the entire chip and there is no per-unit customization of any sort, resulting in a completely VLSI-compatible flow.

A. CNT implementation details

In this section, two designs are implemented with a pMOS-only CNT technology at the 1-μm and 32-nm technology node, respectively, from Stanford University. The first chip implementation is the BBPLL-based sensor interface (Fig. 2a) for a capacitive sensor. As seen in Fig. 11a, the capacitive sensor functions as the load of one delay stage of the SCO, while the DCO is single-bit digitally controlled by switching in or out an extra load capacitance in one stage. The two oscillators (SCO and DCO) are implemented using the inverter ring topology as in the first CMOS design presented, due to its highly-digital nature. As shown in Fig. 11, the nine-stage oscillators use the biased load inverter (Fig. 11b). Similar to the CMOS implementations discussed above, the D-latch (Fig. 11a) functions as the single-bit phase detector, while the single-bit output is also the digital output of the system that is decimated to increase the resolution. The sensor in the SCO is an external non-CNT capacitive sensor.

In the second implementation (Fig. 2b), only one oscillator is used (the SCO). This design corresponds to the open-loop interface using a set-reset counter, shown in Fig. 2b. The period-modulated signal is digitized by using an off-chip set-reset counter (not implemented with CNTs) [13]. Furthermore, this design also implements a CNT-based InfraRed (IR) sensor

TABLE II: Overview of the four implemented time-based sensor interfaces

	CMOS design 1	CMOS design 2	CNT design 1	CNT design 2
Technology	130 nm	130 nm	1 μm	32 nm
Sensor	external cap. sensor	external potentiometer	external cap. sensor	integrated IR sensor
Supply voltage	0.3 V	0.85 - 1.15 V	3 V	2 V
Power	270 nW	124.5 μW	336 μW	130 nW
Speed	1 kHz	20 kHz	kHz range	100 kHz

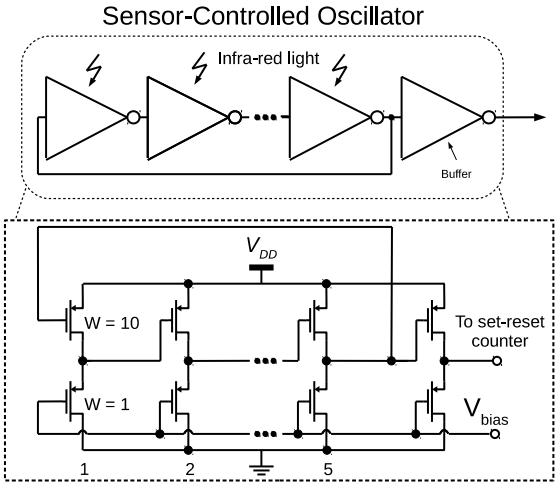


Fig. 12: Second presented design: circuit schematic of the integrated CNFET-based IR sensor and sensor interface. It consists of two blocks: a sensor-to-period converter and a period-to-digital converter. The sensor-to-period converter is implemented entirely with CNFETs as a 5-stage sensor-controlled inverter-based ring oscillator, with the IR sensor integrated in the oscillator itself.

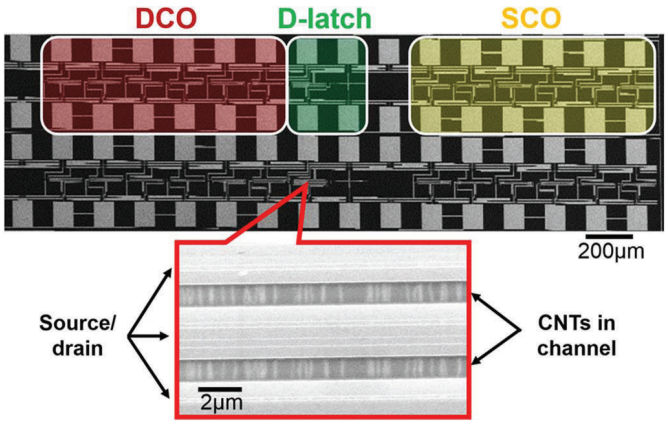


Fig. 13: SEM image of the first CNFET-based sensor interface circuit. Top: two full circuits. Bottom: magnified view of two vertically stacked CNFETs following the aligned-active layout.

by incorporating the sensor functionality in the oscillator itself, which consists of a 5-stage ring topology implemented with biased load inverters like in the first CNT design (see Fig. 12). The sensor is incorporated as follows: when a CNFET in the inverters is exposed to IR light, its drive current increases depending on the intensity and the wavelength of the IR light. The relationship between the oscillation frequency and the drive current of the CNFETs permits the IR light to change the frequency/period of the signal. This results in the oscillator itself functioning as a sensor. The IR-modulated oscillator output signal is digitized afterwards by the set-reset counter. This design has been implemented in a 32-nm CNT technology, which demonstrates both the ability to scale the CNT technology, as well as the ability to combine sensor and interfacing functionality.

B. Measurements of the CNT implementations

The two CNT designs presented have experimentally been measured. The results for both sensor interfaces are shown below, demonstrating their functionality. The capacitive sensor interface circuit in the first design was fabricated in 1-μm CNT technology. A SEM image of the fabricated chip is shown in Fig. 13. It is operated at V_{DD} = 3 V and consumes 336 μW. The measurement results in Fig. 14a show the digital single-bit output signal as a function of the input sensor capacitance. The operating frequency is in the range of kHz. The duty cycle and average output value of the single-bit output changes as a function of the sensor capacitance, as can be seen in Fig. 14b. Due to the noise present in the output waveforms measured, the duty cycle has been extracted using a high threshold value for detecting the ON state. The results presented demonstrate the feasibility of the implemented circuit in an emerging technology such as CNTs.

The second CNT design, the IR sensor and its sensor interface circuit, is implemented in a scaled 32-nm CNT technology and is operated at a reduced supply voltage of 2 V, while consuming only ∼130 nW of power. Measurement results are depicted in Fig. 15a and show the output signal as a function of the IR light power. The measurements show that without IR light, the oscillation frequency is ∼100 kHz. The oscillation frequency increases to ∼115 kHz, when illuminated with IR light (880 nm wavelength, 100 mW power), which shows the sensitivity to IR light. The values of the oscillation frequencies are extracted from the resonant peaks of the output power spectral density measured for each case [13].

Table II presents an overview of the four presented time-based designs - two in CMOS technology and two in CNT technology - discussed in this paper. In the case of the CMOS implementations, the first design shows an extremely-low-voltage operation and power consumption. The second CMOS design operates at a higher supply voltage, but tolerates a 0.3 V variation on the supply voltage and rejects supply noise

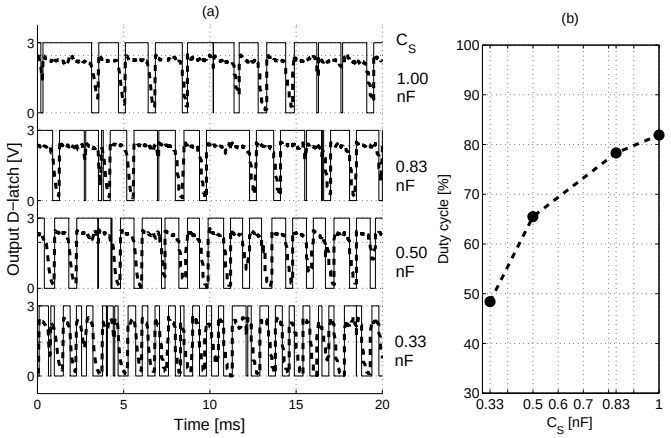


Fig. 14: (a) Experimentally measured (dotted lines) and digitized (solid lines) single-bit outputs of the CNT sensor interface over time for different values of the capacitive sensor. (b) Increasing duty cycle as a function of an increasing input sensor capacitance. It shows the correct functionality of the complete CNFET interface circuit.

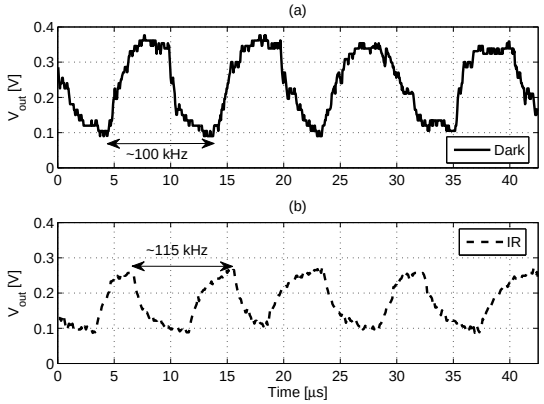


Fig. 15: (a) Output signal of the CNFET ring oscillator in the dark: it oscillates at ∼100 kHz. (b) Output signal of the CNFET ring oscillator under IR illumination: the oscillation frequency increases to ∼115 kHz.

amplitudes up to +10 dB_{FS}. The higher supply voltage, the higher oscillator frequency and the use of the noise-tolerant Maneatis topology, with better phase noise performance but higher power consumption than the inverter-based oscillator, increase the total power consumption with respect to the first CMOS design. This design decision is however justified by the 4.3 bits increase in resolution for a comparable oversampling ratio. Additionally, there is a 20x acquisition speed improvement with respect to the first CMOS implementation.

In the case of the CNT sensor interfaces, the first implementation demonstrates the correct functioning of the BBPLL-based implementation in a pMOS-only CNFET technology. The high power consumption, as compared to the CMOS implementations, has two main reasons: first, the supply voltage needs to be high to provide enough current density due to the high threshold voltage of the experimental CNT technology used. Secondly, the oscillators include bonding pads in each stage's node to facilitate measurements, which heavily load the circuit. High currents are required to load these nodes in each cycle, increasing the power consumption. Furthermore, the oscillators need to have more stages (9 stages in the implemented case) to optimize the amplitude of the output signal, which needs to be big enough to activate the D-latch. For the second CNT implementation, both the operating speed and the power consumption show a significant improvement compared to the first presented CNT sensor interface. There is a 1000x improvement in power consumption, due to the fact that the supply voltage is lower and that the single oscillator is not loaded by bonding pads. This also explains that less stages are needed in the oscillator to provide enough signal amplitude. The 200x improvement in operation frequency has to do with the scaled technology and a better implementation of the oscillator.

V. Conclusion

This paper has given an overview of time-based, highly-digital sensor interface circuits implemented both in CMOS and CNT technologies. On the one hand, the robustness, versatility, low area and low power consumption of the proposed digitally-oriented sensor interface architecture have been verified with two implementations using standard 130-nm CMOS technologies. The first CMOS implementation demonstrates a fully-digital BBPLL-based capacitor sensor interface which operates at a supply voltage of 0.3 V, with a power consumption of only 270 nW for the entire interface and an ENOB of 6.1 bits. The second CMOS implementation demonstrates a BBPLL-based resistive sensor interface which combines an energy-efficient time-based design with a high supply-noise and temperature-drift tolerance. The interface works at a supply voltage range of 0.85-1.15 V, with a power consumption of 124.5 μW. The PSRR achieved is 52 dB at noise amplitudes up to +10 dB_{FS}. It achieves 10.4 bits of resolution, which is 4.3 bits of resolution more than the first CMOS design. The bandwidth is 10 kHz, one order of magnitude better than the first design presented. The two CMOS designs presented confirm that the time-based sensor interface is a good candidate for the next generation of sensor system implementations, due to its high energy efficiency, its robustness and its highly-digital nature which makes it scalable with technology. The architecture is also compatible with digitally-assisted techniques to improve the resolution performance and offset immunity. On the other hand, the combination of these principles and techniques with recent advances in fabricating beyond-CMOS nanotechnology such as CNT circuits in a VLSI-compatible manner, has led to the successful demonstration of two sensor interfaces in CNT technology. The first CNT implementation has demonstrated the feasibility of a capacitive BBPLL-based sensor interface in a 1-μm CNT technology operating at 3 V in the kHz operating range, while consuming 336 μW. The second CNT implementation demonstrates an open-loop period-modulation-based sensor interface with an integrated

IR sensor, in the 32-nm CNT technology node. The sensor is a CNFET-based IR sensor that is integrated in the oscillator itself, resulting in an oscillation frequency that depends on the IR light intensity. Measurements show that the operating frequency of the oscillator is at ∼100 kHz while consuming only 130 nW at 2 V supply voltage. Compared to the first implementation in the 1-μm CNT technology node, this second design shows a 100x speed improvement and a 2500x power consumption improvement, and demonstrates the feasibility of scaling in the CNT technology. In addition, it illustrates the unique possibility of implementing both the sensor and the sensor interface circuitry with CNFETs integrated on a single die. This paves the way towards future fully-integrated energy-efficient sensor systems on chip.

ACKNOWLEDGMENT

The authors acknowledge the support of NSF, FCRP C2S2, FCRP FENA, STARNet SONIC, FWO Flanders (for Jelle Van Rethy), and the Stanford Graduate Fellowship and the Hertz Foundation Fellowship (for Max Shulaker).

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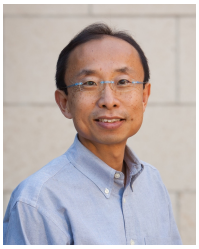
Georges Gielen received the MSc and PhD degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. He is full professor at the Department of Electrical Engineering (ESAT). From August 2013 Georges Gielen is also appointed as vice rector for the Group Science, Engineering and Technology and Academic Personnel of the KU Leuven. His research interests are in the design of analog and mixedsignal integrated circuits, and especially in analog and mixedsignal CAD tools and design automation. He is coordinator or partner of several (industrial) research projects in this area, including several European projects. He has authored or coauthored 7 books and more than 450 papers in edited books, international journals and conference proceedings. He is Fellow of the IEEE since 2002.

Jelle Van Rethy was born in Geel, Belgium, in 1986. He received the M.Sc. and Ph.D. degrees in electrical engineering from the KU Leuven, Leuven, Belgium, in 2010 and 2014, respectively. He is currently with Melexis Technologies Tessenderlo, Belgium, where he is working in the design and implementation of analog building blocks for ICs used in various automotive applications.

Jorge Marin was born in 1982 in Santiago, Chile. He received the B.Sc. and M.Sc. in electrical engineering from the University of Chile in 2007 and 2010, respectively. In 2012 he received the M.Sc. in electrical engineering from the KU Leuven, where he is currently working toward the Ph.D. degree. His current research interests include design of digitally-assisted, drift-independent mixed-signal ICs for data conversion and sensor interfacing.

Max M. Shulaker received his B.S. in Electrical Engineering from Stanford University in 2011. He is currently a PhD candidate at Stanford University, and works on experimentally demonstrating nano-systems with emerging technologies. His current research focus is on realizing increased levels of integration for carbon-nanotube based digital logic circuits. He is a Stanford Graduate Fellow and a Fannie and John Hertz Fellow.

Gage Hills received the B.S. degree in electrical engineering and computer science from Yale University, New Haven, CT, USA, in 2007, and the M.S. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2012, where he is currently pursuing the Ph.D. degree. His current research interests include experimental demonstrations and statistical modeling of very large-scale carbon nanotube-based digital circuits.



H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. At IBM, he held various positions from Research Staff Member to Manager, and Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBMs strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. His present research covers a broad range of topics including carbon electronics, 2D layered materials, wireless implantable biosensors, directed self-assembly, nanoelectromechanical relays, device modeling, brain-inspired computing, and non-volatile memory devices such as phase change memory, conductive bridge memory, and metal oxide resistance change memory. He is a Fellow of the IEEE. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology in 2005 2006, sub-committee Chair of the ISSCC (2003 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He is the founding Faculty Co-Director of the Stanford SystemX Alliance an industrial affiliate program focused on building systems.

Subhasish Mitra received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA. He directs the Robust Systems Group in the Department of Electrical Engineering and the Department of Computer Science of Stanford University, where he is the Chambers Faculty Scholar of Engineering. Before joining Stanford, he was a Principal Engineer at Intel.

Prof. Mitra's research interests include robust systems, VLSI design, CAD, validation and test, emerging nanotechnologies, and emerging neuroscience applications. His X-Compact technique for test compression has been key to cost-effective manufacturing and high-quality testing of a vast majority of electronic systems, including numerous Intel products. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools. He, jointly with his students and collaborators, demonstrated the first carbon nanotube computer, and it was featured on the cover of NATURE. The US National Science Foundation presented this work as a Research Highlight to the US Congress, and it also was highlighted as "an important, scientific breakthrough" by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, National Public Radio, New York Times, Scientific American, Time, Wall Street Journal, Washington Post, and numerous other organizations worldwide.

Prof. Mitra's honors include the Presidential Early Career Award for Scientists and Engineers from the White House, the highest US honor for early-career outstanding scientists and engineers, the ACM SIGDA/IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation, "a test of time honor" for an outstanding technical contribution, the Semiconductor Research Corporation's Technical Excellence Award, and the Intel Achievement Award, Intel's highest corporate honor. He and his students published several award-winning papers at major venues: IEEE/ACM Design Automation Conference, IEEE International Solid-State Circuits Conference, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, Intel Design and Test Technology Conference, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors "for being important to them during their time at Stanford."

Prof. Mitra has served on numerous conference committees and journal editorial boards. He served on DARPA's Information Science and Technology Board as an invited member. He is a Fellow of the ACM and the IEEE.