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(article begins on next page)

High-speed single cable synchronization system for data-converters

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Abstract A clock-cycle accurate synchronization technique for fully integrated data-converters is presented. Only a single cable is needed to distribute both the required synchronization signal and the converter clock. Different possible implementations, both to generate and decompose the distributed signal, are presented. A discrete component generator circuit is discussed. To avoid setup and hold time violations, on-chip signal reconstruction is unavoidable. A 40 nm CMOS recovery circuit was developed. Simulation results, including layout parasitics, show the wide frequency operating range of the proposed technique.

Keywords Data converters · Synchronization · Reference distribution · Clock distribution · CMOS

1 Introduction

Several systems employ multiple data-converters at different locations, that require clock cycle accurate synchronization. One example are time difference of arrival based localization systems [1, 2]. The signal's time of flight to each basestation (data-converter) is determined. This generally involves a correlation method [3]. Therefore, it is crucial that signal capturing in each data-converter starts synchronously. Only static start time differences can be calibrated and therefore tolerated.

To achieve clock cycle accurate synchronization, there should be no setup and hold time violations and no

metastability in the system. Otherwise a one sample period ambiguity is introduced, that can drastically impact system performance. If synchronization and clock signal are distributed by separate cables, this can only be achieved when both electrical lengths are matched. The timing difference between synchronization and clock has to be controlled. Matching becomes more difficult with increasing sample rates as wavelength shortens.

The one clock cycle ambiguity is also present when each basestation uses a separate PLL to generate the sample clock. At some point the synchronization pulse needs to align with the faster PLL generated clock. Setup and hold times in this circuit can not be guaranteed, even if the synchronization signal is sufficiently steep and aligned to the PLL's reference. In order to avoid metastability, the phase difference between reference and PLL output should be smaller than 1 period of the data-converter clock. This can not be guaranteed, the exact phase difference is even unknown.

One solution is to only distribute the clock when the data-converter needs to sample. A drawback of this method is that a separate reference clock for generation of the front-end or up-converter LO still has to be distributed. To avoid these problems, a short duration "amplitude shift" of the distributed clock signal is proposed. This shift embeds the synchronization (*Sync*) in the clock line. No separate *Sync* or reference cable is needed.

2 Amplitude shift generation and signal recovery

Amplitude shifting changes the amplitude of the clock signal to indicate a sync event. The depth of this amplitude modulation, should be high enough to accurately recover

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the synchronization signal. But, at the same time low enough for the LO generation loop PLL to hold lock.

Figure 1 illustrates the resulting amplitude shifted clock signal. To get precise, clock sample accurate, synchronization it is mandatory that the shifted clock signal has converged to a decent signal at the evaluation moment of the recovery circuit. Therefore, all transient effects due to the amplitude change should disappear in half a clock period. In this case during the negative phase.

This technique is insensitive to the signals DC component. Both square and sine waves can be used, as only the amplitude change is important for correct recovery. AC-coupled amplifiers can be used to boost the clock before passive splitting. AC coupled power splitters can be used, that don't require any resistive components and therefore have less loss.

By using this clocking scheme every data converter is guaranteed to start at the same clock edge. Only the jitter on that clock edge introduces uncertainty about when the data converter processes the sample. The remaining offsets, due to electrical cable length and recovery circuit delays, are static. Static offsets are time invariant, and can therefore be calibrated out at system level.

2.1 Shifting topologies

It is important that the signal change settles within half a clock period. If the data converter samples at the positive clock edge, the amplitude transition therefore ideally occurs at the falling edge and vice versa. For this purpose, both circuits presented below employ a phase shifter. As positive edge sampling is assumed, the amplitude change event is aligned to the zero crossing of the falling edge of the reference clock.

2.1.1 VGA based shifting

To generate the amplitude variation of the clock signal, two methods were practically implemented. First, a variable

Fig. 1 Waveforms of the amplitude shifted clock, combining both clock and sync signal on a single distribution wire

gain amplifier (VGA) topology is proposed. A digital input VGA is used to change the amplitude of the clock. The circuit concept is given in Fig. 2. When the input is high the VGA has the highest amplification. When low, the gain changes to indicate a synchronization event (i.e. by 6 dB). The D Flip-flop synchronizes the sync signal with the clock edge. The phase shifter is necessary to tune out any delay from the flip-flop or amplifier.

The bandwidth of the VGA should be large enough to accommodate the clock frequency. The settling time also needs to be well defined and has to be lower than half a period as specified before. VGA's typically have a settling time of over 36 ns [4], which limits the maximum clock frequency to about 14 MHz. For higher frequencies, transition will take more than one clock period to settle as illustrated in Fig. 3.

Multi-cycle amplitude transition is problematic for the recovery circuit. Ideally only two well defined amplitude values are present at the sampling moments. A slower transition requires a lower offset comparator, as values close to the threshold can otherwise cause false triggering. Therefore, a slow transition also lowers the systems noise margin.

2.1.2 Mixer based shifting

Another way to generate the amplitude shifted clock signal is by using a mixer. The idea is to multiply two different DC voltages with the clock, a low voltage for a logic 0 and a high voltage for a logic 1 on the Sync input. Figure 4 shows the topology's block diagram. A DC level shift is needed to present the correct voltage levels to the analog mixer input.

If the bandwidth of the IF input, used to modulate the signal, is high enough the settling time problem is solved. A passive mixers is needed, because of the large bandwidth. The amplifier after the mixer needs to compensate for the conversion loss. A phase shifter is again needed to compensate for mixer and flip-flop delays.

Fig. 2 Block diagram of the VGA based generator

Fig. 3 Simulated amplitude transition of the VGA based shifter output, for a 2 GHz clock

2.2 Recovering topologies

In the data converter, clock and synchronization signal (*Sync*) need to be separated again. First the clock gets recovered. The amplitude variation needs to be removed. This can be done with a high speed comparator, limiter or any other high gain block with.

The next step is to retrieve the amplitude information. Two methods are presented. The first method is the use of an envelope detector, the other makes use of delayed coherent sampling.

2.2.1 Envelope detection

One solution uses an envelope detector to filter out the amplitude variation (Fig. 5). Comparison of the resulting signal recovers the *Sync* signal. The bandwidth of the detector should be high enough to ensure the signal settles in half a period. A comparator followed by a D flip-flop samples the output at the falling edge of the clock. The

Fig. 4 Block diagram of the mixer based generator

second D flip-flop synchronizes the signal to the positive edge of the amplitude shifted clock.

This method has the advantage of not requiring any reconfiguration when clock frequency changes. A drawback of the circuit is that a very fast settling time envelope detector is needed. The analog components in this structure need to be very fast.

2.2.2 Delayed coherent sampling

For the coherent sampling approach, a delayed version of the recovered data-converter clock is introduced. The delayed clock determines the moment on which the output of the comparator is sampled. The comparator threshold voltage is ideally placed in the middle of both amplitude levels.

The delay is tuned in order to capture the comparator output at the moment when the amplitude shifted clock is at its maximum value. This corresponds to the peaks in the circuit's input signal. Therefore a delay by one fourth of a period has to be used.

Figure 6 shows a block diagram of the delayed coherent sampling technique. The amplitude shifted clock passes through a gain stage to remove any amplitude information. Afterwards the recovered clock is fed into a variable delay element. This generates a delayed clock that goes to a D flip-flop that samples the output of the comparator. The output of the first D flip-flop is synchronized back to the normal clock, by a second D flip-flop clocked by the not delayed recovered clock. A rising edge on *Sync* signals the synchronization event.

The minimum frequency of the distributed clock, is defined by the clock delay element and equal to four times the maximal delay. The maximum frequency is set by circuit parasitics and by the minimum delay. A positive property of this circuit is that most of the processing happens in the digital domain, and therefore can be integrated without consuming a lot of area in a standard CMOS process. No analog filters, that require tuning, are needed. On the downside, the delay has to be tuned for each amplitude shifted clock frequency. However, tuning can be done in the digital domain.

Fig. 5 Envelop detector based recovery circuit

Fig. 6 Delayed coherent sampling recovery circuit

3 Generation circuit

The amplitude shift clock generator with the double balanced mixer has a large bandwidth and a better settling time for the application. Therefore this topology is used in the proposed discrete component solution. Figure 7 shows the detailed circuit implementation.

A Mini-Circuits passive double balanced mixer is used [5]. The most important selection parameter is the IF bandwidth. A large enough bandwidth is needed to guarantee all transient effects settle in half a period. To get a continuous sine wave output at the RF port, there shouldn't be any high pass filtering on the IF path. With the chosen mixer a constant carrier can be generated by biasing the mixer at a proper DC voltage.

The level-shifter input is connected to a positive emitter coupled logic D flip-flop. The chosen D flip-flop can handle data rates up to a few Gbps, with a fairly constant propagation delay. Also the output rise and fall times are significantly lower than the half a clock period mark.

Therefore, the main limitation on the amplitude transition comes from the mixer circuit.

A low phase noise clock is connected to the *Clk* connector. It is split to the phase shifter and the PECL D flip-flop [6]. A resistive splitter is used, to have a good wide band response, but it has a loss of 6 dB. The phase shifter has a loss of 3 dB. The mixer needs at least 8 dBm LO power, so to provide some extra margin the input clock should deliver at least 16 dBm.

The synchronization signal (*Sync*) is buffered by a TTL to PECL chip to generate a steep edge at the D flip-flop input. The outputs of the D flip-flop are AC coupled to allow easier level shifting. The voltage levels of the PECL logic need to be shifted down to get a better amplitude change ratio. The normal PECL levels of 4.2 V for high and 3.4 V for low, are shifted to 0.8 V and 0.4 V respectively to achieve good mixing performance. All mixer diodes need to get evenly into forward and reverse bias. Simulations, incorporating the mixer, have shown these voltage levels to lead to the best output signal.

The implementation of this level shift circuit is shown in Fig. 7. A constant 0.8 V input is provided to the mixer input. When a *Sync* pulse needs to be transmitted, the PECL D flip-flop will subtract a configurable voltage from the input of the mixer, to make sure it only sees 0.4 V. This halves the amplitude, and generates the amplitude shift. By using a short *Sync Pulse*, the transient behavior of the AC coupling capacitor is avoided. It will work as a short circuit for that instant.

Fig. 7 Detail of the generator circuit

Due to the high conversion loss, the shifted clock power at mixer output is quite low because. A wide band amplifier is used to boost the signal to a higher level before it can be distributed to the different data converters. The final step is a power amplifier with enough gain and high output power. The used amplifier, Mini-Circuits GALI-84+ [7], has a gain of 20 dB at 2 GHz. As the mixer has an output power of around 0 dBm, the additional amplifier raises circuit output power to 18 dBm.

4 On-chip detection circuit

As described earlier, the use of envelope detection to detect the amplitude shift is not trivial. The envelope detector uses a rectifier, followed by a low-pass filter. The filter is needed to remove the carrier and harmonics, generated by the rectification, from the extracted envelope. A good suppression is needed, requiring a large filtering capacitor. As on-chip capacitors have a low density, a large capacitor uses a lot of area. Furthermore a wide operating range is needed, both for flexibility reasons and to increase robustness against process variations. Therefore, the filter in the envelope detector needs to be tuneable. This is difficult to realize, especially in an on-chip implementation.

For these reasons, the coherent sampling method is used to detect the start of the synchronization signal. It is crucial that the *Sync* signal is settled before the clock edge (*Clk*) of the data converter arrives. Otherwise setup and hold time violations would occur, and the exact moment of conversion can not be guaranteed. Therefore, a discrete implementation requires phase matching of the *Sync* and *Clk* signals. This can be alleviated by putting the recovery circuit on the same die as the data converter. The phase difference is lower and easier to control. On-chip, when properly buffered, the delay between both signals is negligible. Therefore on-chip recovery is preferred.

The architecture of the on-chip recovery circuit, designed and implemented in a 40 nm CMOS technology, is given in Fig. 8. First, the clock signal (*Clk*) is reconstructed from the distributed amplitude shifted clock by means of a replica biased comparator. From *Clk* the differential clock for the data-converter is extracted. A 128 element delay line, in combination with a 128 input MUX, is used to generate the $T_{Clk}/4$ delayed clock signal (*Delay_N* and *Delay_P*).

Delay_N and *Delay_P* clock the clocked comparator that detects the amplitude change. The reference level (V_{ref}) can be changed externally and is applied off-chip with sufficient on-chip decoupling. A negative edge triggered D flip-flop is used to synchronize the comparator output signal with the delayed clock. A second D flip-flop synchronizes the recovered *Sync* with the data-converter input clock signal (*Clk*). This way setup and hold time violations are avoided.

The distributed clock signal is on-chip AC coupled by a MOM capacitor of around 500 fF, to avoid DC problems. The schematic of the replica-biased comparator is given in Fig. 9. The size, relative to minimal transistor size, is also indicated. The replica biasing inverter on the left ensures the right inverter, that acts as a comparator, is biased at optimal trip point. This guarantees fast operation and high sensitivity. The replica biasing also provides a stable DC voltage to the on-chip signal. This is necessary for correct amplitude change detection by the clocked comparator.

The schematic of the clocked comparator, used to detect the decrease in amplitude, is given in Fig. 10. The relative size, compared to a minimal transistor, is also indicated. For speed reasons a sense amplifier based comparator, similar to the one in [8], is used. When *Clk* is low both inputs *In_N* and *In_P* are connected to the latch structure in the center. In this phase the latch is also disconnected from the supply. Imbalance in *In_N* and *In_P* causes an imbalance at the input of the inverters that make up the latch. When *Clk* goes high, the latch is connected to the supply, inputs are disconnected and the comparator makes a quick evaluation.

The delay cells, used by the delay line, consist of a cascade of 2 minimal sized inverters. Minimal inverters can be used, as mismatch is determined by the manufacturing process and therefore remains static once manufactured. This will not cause additional jitter. Each delay cell has a delay of around 41 ps, including layout parasitics. As the delay line is 128 elements long, the lowest frequency of *Clk* is limited to 47 MHz. For lower frequencies, maximum delay is less than 1/4 of a period and correct *Sync* detection can not be guaranteed. The upper limit on *Clk* is determined by the delay of a single cell, resulting in a maximum frequency of 6 GHz.

The circuit in Fig. 8 outputs an *Sync* signal that is high during the full modulation period of the amplitude shifted clock. When a pulse is required the circuit in Fig. 11 can be used. The result of the clocked comparator is passed through a cascade of 2 flip-flops, both clocked by the $T_{Clk}/4$ delayed clock signal. The current and previous state of the output are sampled and stored. Passing both signals, inverting one of them, through an AND-gate creates an edge detector circuit. The output is a *Sync* pulse with a duration of 1 *Clk* period, when the amplitude variation is detected.

The circuit was implemented in a 40 nm CMOS technology. Figure 12 shows the simulated results of the *Sync* recovery for a 3 GHz input signal. 100 mV peak-to-peak voltage noise is added to the supply to evaluate jitter performance. A modulation depth of 66% is used, changing the peak-to-peak amplitude between 0.9 and 0.33 V. The comparator reference voltage (V_{ref}) is placed exactly in the middle of both for optimal detection. Simulation shows correct operation up to 6 GHz.

Figure 13 shows simulated sampling clock (*Clk*) recovery for a 3 GHz amplitude shifted clock. With a

Fig. 8 Architecture of the on-chip recovery circuit

Fig. 9 Transistor implementation of the replica biased comparator

Fig. 10 Transistor implementation of the clocked comparator

Fig. 11 Generation of a synchronization pulse

Fig. 12 Simulated output of the Sync recovery circuit

supply noise of 100 mV, the jitter on Clk is smaller than 20 ps and this for an input signal up to 6 GHz. The 20 ps requirement is set by the ranging algorithm. The ADC start pulse ($Sync$) has a simulated jitter smaller than 5 ps for the same supply variation. Layout parasitics are included in all simulations.

Fig. 13 ADC sample clock recovered from the amplitude shifted clock

5 Conclusion

In this paper a single cable synchronization system for high speed data-converters was presented. It eliminates setup and hold time associated problems due to incorrect timing between the converter clock and synchronization signal, while at the same time providing a constant reference signal. The technique distributes an amplitude shifted clock signal. The amplitude of the reference clock is reduced to indicate the needed synchronization event.

The essential signal constraints were discussed. Transients due to the amplitude change have to decay in half a clock period. Generation of the amplitude shifted signal is addressed, and a practical implementation using discrete components is provided. The circuit allows signal generation up to 3 GHz, as verified by measurements.

At the data converter side, the amplitude shifted clock signal has to be decomposed again in clock and synchronization signal. An on-chip implementation in a 40 nm CMOS technology is presented. The recovery circuit uses the delayed coherent sampling approach. The clock frequency is tuneable by means of a digitally controlled delay line. Successful recovery of clock signals between 47 MHz and 6 GHz is achieved, as verified by layout parasitic enabled simulations.

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References

- Redant, T., Ayhan, T., De Clercq, N., Verhelst, M., Reynaert, P., & Dehaene, W. (2014). 20.1 A 40 nm CMOS receiver for 60 GHz

discrete-carrier indoor localization achieving mm-precision at 4 m range. In *IEEE international solid-state circuits conference digest of technical papers* (vol. 57, pp. 342–343).

- Indirayanti, P., Ayhan, T., Verhelst, M., Dehaene, W., & Reynaert, P. (2014). A 60 GHz transmitter in 40 nm CMOS achieving mm-precision for discrete-carrier localization. In *ESSCIRC 2014—40th European solid state circuits conference (ESSCIRC)*, (vol. 2, pp. 291–294).
- Ayhan, T., Redant, T., Verhelst, M., & Dehaene, W. (2012). Towards a fast and hardware efficient sub-mm precision ranging system. In *IEEE workshop on signal processing systems (SiPS)* (pp. 203–208).
- Analog Devices, ADL5243 100 MHz to 4000 MHz RF/IF Digitally Controlled VGA. (online). <http://www.analog.com/media/en/technical-documentation/evaluation-documentation/ADL5243.pdf>.
- Mini-Circuits, SIM-792LH+ Frequency Mixer. (online). <http://194.75.38.69/pdfs/SIM-792LH+.pdf>.
- ON Semiconductor, MC100EP52 3.3V/5V ECL Differential Data and Clock D Flip-Flop. (online). http://www.onsemi.com/pub_link/Collateral/MC100EP52-D.PDF.
- Mini-Circuits, GALI-84+ Monolithic Amplifier. (online). <http://194.75.38.69/pdfs/GALI-84+.pdf>.
- Rooseleer, B., Cosemans, S., & Dehaene, W. (2012). A 65 nm, 850 MHz, 256 kbit, 4.3 pJ/access, ultra low leakage power memory using dynamic cell stability and a dual swing data link. *IEEE Journal of Solid-State Circuits*, 47(7), 1784–1796.

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