A 36.4dB SNDR @ 5GHz 1.25GS/s 7b 3.56mW Single-Channel SAR ADC in 28nm Bulk CMOS

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***Abstract*—A 1.25GS/s 7b single-channel SAR ADC is presented with an SNDR/SFDR of 41.4dB/51dB at low frequencies, while the SNDR/SFDR at Nyquist are 40.1dB/52dB and remain still 36.4dB/50.1dB at 5GHz. The high input frequency linearity is enabled by a fast bootstrap circuit for the input switch, while the high sampling rate, the highest among recently published >34dB SNDR single-channel SAR ADCs is achieved by a Triple-Tail dynamic comparator and a Unit-Switch-Plus-Cap (USPC) DAC. The prototype ADC in 28nm CMOS consumes only 3.56mW from a 1V supply, leading to a Walden FoM of 34.4fJ/conv-step at Nyquist for a core chip area of 0.0071mm^2.**

***Index Terms*—Successive approximation register, high sampling rate, high bandwidth, low power, bootstrapped input switch, capacitive DAC (CDAC), dynamic comparator.**

I. Introduction

To support the continuous bandwidth growth of modern high-speed serial links, medium-resolution, power-efficient GHz-sampling-rate ADCs are highly demanded. SAR ADCs show an admirable power-efficiency due to their highly digital nature, allowing them to scale excellently into deep-submicron nodes. Prior works have shown an increase in SAR ADC sampling rate by employing multi-bit per step decisions [1], [4], capacitive DAC redundancy and alternate comparators [2], various interleaving schemes [3]-[5] and interrupted settling [6]. However, the increased complexity of these designs (i.e. extra components, complex logic), results in a significant SNDR degradation. Calibration is often employed to partially compensate for the lost SNDR [1]-[5], which further increases complexity and limits robustness.

This work aims to tackle the aforementioned issues with a 7b calibration-free SAR ADC, able to achieve 1.25GS/s and 5GHz input sampling ability by employing 1) a high-speed bootstrap circuit for the input switch, 2) a Unit-Switch-Plus-Cap (USPC) DAC and 3) a Triple-Tail fully dynamic comparator, aggressively optimized for maximum speed/power and optimally combined in minimum hardware. As such, the added complexity of redundancy, alternate comparators and multi-bit per step decisions is alleviated, resulting in only 1.3dB SNDR drop between low frequencies and Nyquist and allowing for higher speed interleaving with minimum extra design overhead.

This paper is organized as follows. Section II describes the overall ADC architecture and the bootstrapped input switch. Sections III and IV present the Unit-Switch-Plus-Cap DAC and the Triple-Tail comparator architecture. Section V summarizes the measurement results along with a recent state-of-the-art comparison. Finally, in Section VI conclusions are drawn.

II. Proposed ADC Architecture and Input Switch

Fig. 1 illustrates the top-level ADC architecture and its timing diagram. The sampling clock (SAM), with a 12.5% duty cycle drives the T/H and initiates the internal logic, responsible for generating the bit phases, controlling the comparator, storing its decisions and switching the CDAC. During every fixed bit cycle of 100ps, the comparator shares its timing with the CDAC to fully exploit the nature of the successive approximation algorithm which imposes on average a worst case (slowest) comparison once for every sample. The logic, therefore, senses the comparator in a semi-asynchronous fashion [5] and passes its decision to the DAC with a maximum delay of 3 gates in the critical path, taking advantage of fast comparator decisions to assist CDAC settling whenever possible by allocating more time to it. The output bits are collected serially at full speed (10Gb/s) to a Bit Error Rate Tester (BERT) for performance evaluation.

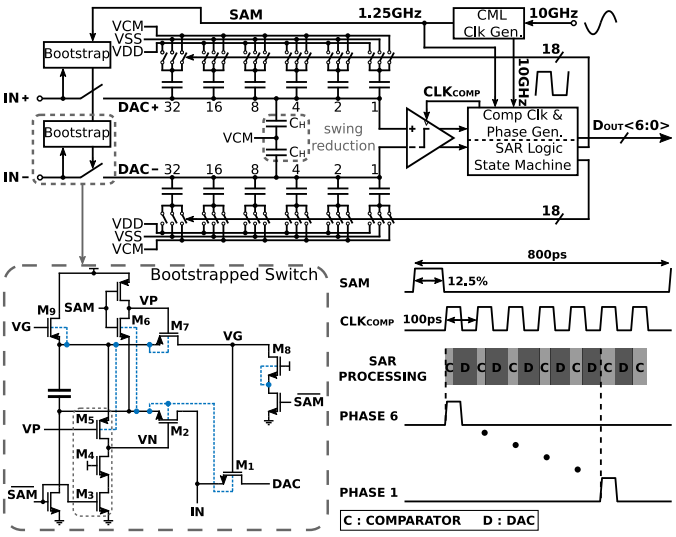

Fig. 1. Top-level ADC architecture (top), its timing diagram (bottom-right) and the circuit schematic of the bootstrapped switch (bottom-left).

Top-plate sampling is utilized in the T/H for maximum speed and the input switch is bootstrapped to improve linearity at high input frequencies. The bootstrap circuit (Fig. 1, bottom-left), utilizes transistors M_3-M_5 to immediately turn on M_2 with maximum overdrive voltage, relieving at the same time VG from its load, which in combination with the optimal bulk connections of the critical transistors, ensure steep rise and fall transients of VG. As a result, the on-resistance of M_1 is kept low and constant, which leads to an enhanced linearity at high frequencies compared to [7] and the typical bootstrap circuit [8], while the reliability is ensured and the area is reduced (no charge-pump [7]). Post-extracted simulations indicate on average a linearity improvement of 4dB and 7dB compared to [7] and [8] respectively at 1.25GS/s.

III. Unit-Switch-Plus-Cap DAC

The CDAC employs a symmetrical switching scheme similar to [3], adjusted to the top-plate sampling, allowing a constant current to be drawn from the references, regardless of the input voltage, and requiring only 6 capacitors for 7b resolution. A total input capacitance of 200fF, realized with custom-made 1.25fF unit cells is chosen, for low noise and good matching performance. 40% of it is switchable and the rest (C_H) is responsible for attenuating the CDAC signal range.

CDAC settling is one of the major delays in every SAR ADC, determined by the unit capacitance (C_U), the reference switch on-resistance (R_{ON}), as well as the wiring resistance (R_W) and capacitance (C_W) (Fig. 2). Conventionally, the switches are placed along the path between the logic and the CDAC [3], leading to a large R_W and/or C_W, significantly stalling the settling, especially for very small unit capacitors (C_U∼1fF), where these parasitics start dominating. This design introduces a Unit-Switch-Plus-Cap (USPC) technique which reduces CDAC settling by merging the reference switches with C_U, making them part of the CDAC. Both R_W and C_W are minimized in the critical path, while the switches are kept small and easy to drive without extra logic delay (Fig. 2). For our design, this results in 40% faster and more uniform settling/cycle and a 14% faster ADC (post-extracted simulations) with no area penalty.

IV. Triple-Tail Dynamic Comparator

The proposed comparator comprises a cascoded preamplifier followed by an amplifier/half-latch driving a latching stage in a fully dynamic Triple-Tail configuration (Fig. 3). The first amplification stage is designed for high gain and low offset, with the NMOS cascode further isolating the input pair from reset kickback, while the last stage is optimized for speed. The second stage suppresses the output latch noise and provides further signal amplification prior to the latch, thus minimizing its regeneration time. The intermediate devices M_{2P}-M_{2N} and M_{3P}-M_{3N} provide further shielding from latch output noise as well as reset nodes YP/YN and OP/ON respectively, obviating the need for extra reset transistors, which reduces the capacitance at those nodes. This comparator shows a fast

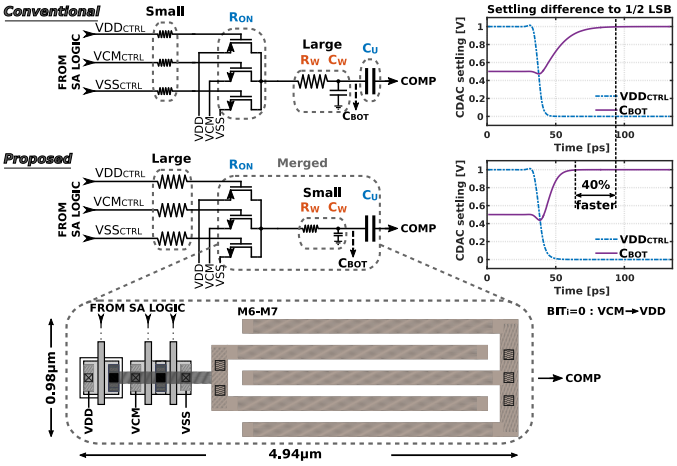

Fig. 2. Simplified schematics, comparison between conventional unit-cap CDAC and the proposed USPC CDAC (extracted at 50°C) (right) and USPC unit cell layout view (bottom).

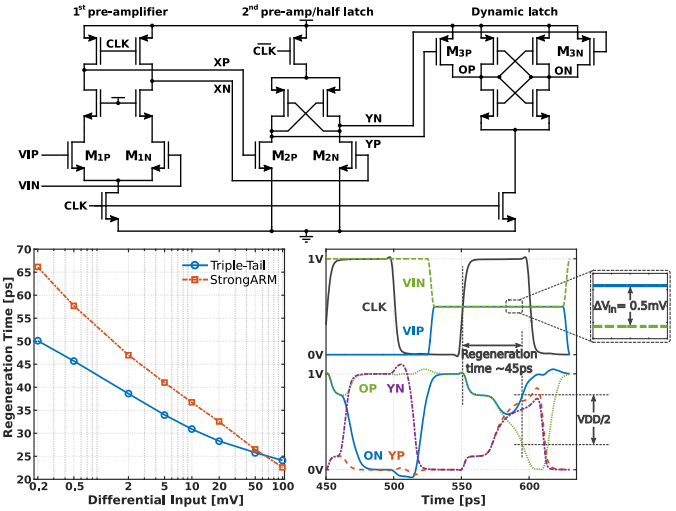

Fig. 3. Triple-Tail comparator schematic (top) with simulated performance under the overdrive recovery test (bottom-right) and comparison with the conventional Strong-ARM (bottom-left) (extracted at 50°C).

regeneration time of ∼45ps for a 0.5mV input with low delay sensitivity to input common mode variations and increases the ADC speed by about 10% compared to the conventional StrongARM architecture [2] (post-layout simulation) with the same offset performance (Fig. 3).

V. Measurement Results

The prototype chip is fabricated in 28nm bulk CMOS with a core area of 49x145μm^2 (Fig. 4). The ADC full-scale input is 800mVpp-diff with a common mode of 500mV. The measured power consumption of 3.56mW (excluding Clk Gen. & CML outputs) at 1V supply and 1.25GS/s partitions into 1.07mW for the bootstrapped switch and DAC, 1.06mW for the comparator and 1.43mW for the phase and SAR logic.

The measured static performance at 1.25GS/s sampling rate for an input frequency of 160kHz is illustrated in Fig. 5. Both INL and DNL are within ± 0.5 LSB and they show small

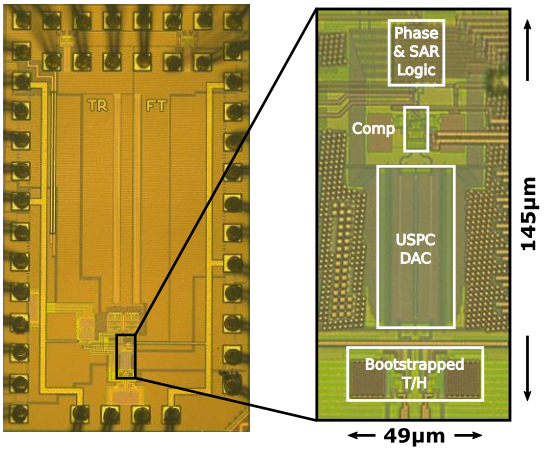

Fig. 4. Die micrograph of the 28nm chip with a zoomed-in view of the ADC core occupying an active area of 0.0071mm^2.

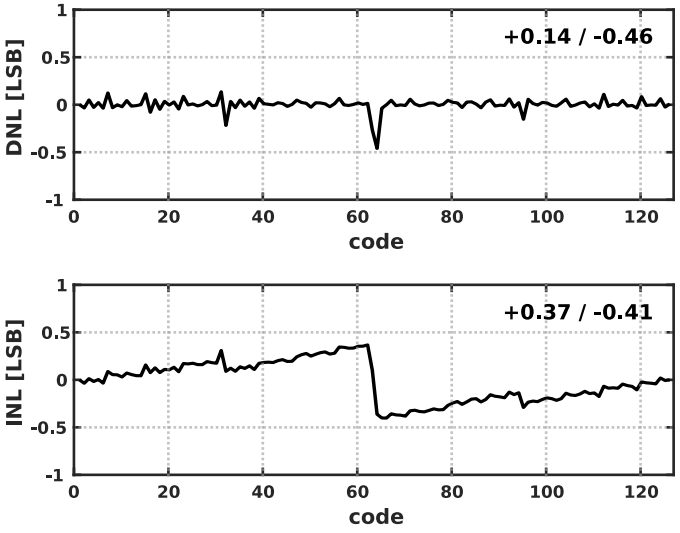

Fig. 5. Measured DNL/INL with the Histogram (Code Density) test at 1.25GS/s for a sinusoidal input of 160kHz.

systematic mismatch from the layout of the CDAC for the MSB and MSB-1 capacitors.

Fig. 6 shows the measured output spectra at 1.25GS/s for Nyquist and 5GHz (8th Nyquist zone) input frequencies respectively, as well as SNDR and SFDR vs. input frequency at 1.25GS/s. The SNDR is 41.4dB at low input frequencies, while at Nyquist it is 40.1dB, limited by thermal noise. At a 5GHz input the SNDR remains still 36.4dB, limited by the T/H bandwidth. The high linearity and speed of the implemented bootstrapped switch, allow for an SFDR in excess of 50dB all the way up to 5GHz, making higher-speed interleaving of this ADC, a mere addition of sub-units.

Fig. 7 illustrates the measured ENOB and FoM vs. sampling rate at an input frequency of 76MHz for 4 different samples. The speed benefits of the proposed comparator and USPC DAC result in >6.5b ENOB up to 1.125GS/s, while the FoM has an optimum of about 30fJ/conv-step. Both start degrading smoothly above 1.25GS/s as the cycle time becomes too short

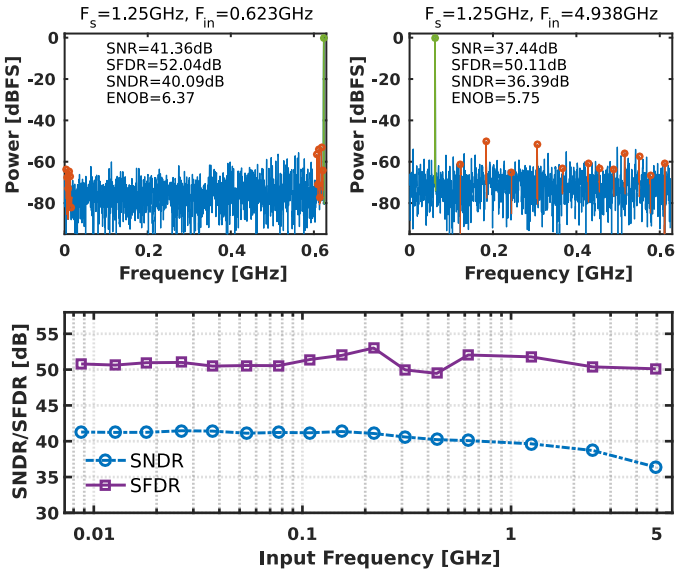

Fig. 6. Measured output spectra at 1.25GS/s (top) and SNDR/SFDR vs. input frequency at 1.25GS/s (bottom).

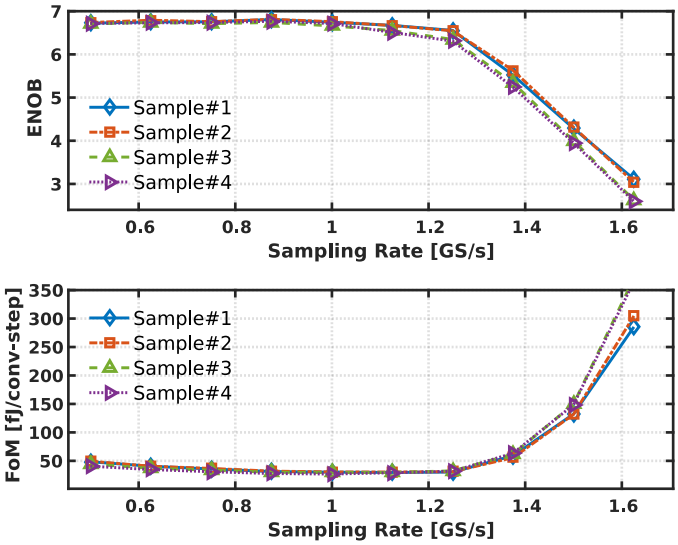

Fig. 7. Measured ENOB and FoM vs. sampling rate for 4 different samples at an input frequency of 76MHz.

for the input switch to track linearly enough and the internal components to fulfill their timings successfully.

This work compares favorably with recent state-of-the-art SAR ADCs of similar performance [9], as can be summarized in TABLE I and illustrated in Fig. 8. This ADC achieves the highest sampling rate among previously reported >34dB/channel SNDR SAR ADCs, including those in SOI technology. It shows >9dB SNDR from the closest competitor in Bulk CMOS and >6dB SNDR from the closest SOI competitor with the same sampling rate. It also achieves the lowest FoM for the lowest SNDR drop among previous >6b, >0.8GS/s/channel ADCs, with zero extra hardware complexity or any calibration requirement.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ADCS

	This Work	Wei ISSCC'11[1]	Kull ISSCC'13[2]	Le Tual ISSCC'14[3]	Chan ISSCC'15[4]	Choo ISSCC'16[6]
Technology [nm]	**28nm CMOS**	65nm CMOS	32nm SOI	28nm FDSOI	65nm CMOS	40nm CMOS
Architecture	**SAR**	2b/c SAR	2 comp SAR	TI-SAR	3b/c TI-SAR	ci-SAR
Calibration	**NO**	YES	YES	YES	YES	N.A.
Interleaving Factor	**1x**	1x	1x	8x	4x	1x
Resolution [bits]	**7**	8	8	6	6	6
Supply [V]	**1.0**	1.2	1.0	1.0	1.0	1.0
Sample Rate [GS/s]	**1.25**	0.4	1.2	1.25*	1.25*	1.0
Power Consumption [mW]	**3.56**	4.0	3.1	4.0*	1.375*	1.26
Active Area [mm^2]	**0.0071**	0.024	0.0031	0.00072*	0.0225*	0.00058
SNDR @ Nyq. [dB]	**40.1**	40.4	39.3	33.8	30.8	34.6
Max. Fin [GHz]	**5.0**	0.2	0.6	20.0	2.5	0.5
FoM @ Nyq. [fJ/conv-step]	**34.4**	116.9	34.0	80.4	39.0	28.7

* Metric per channel

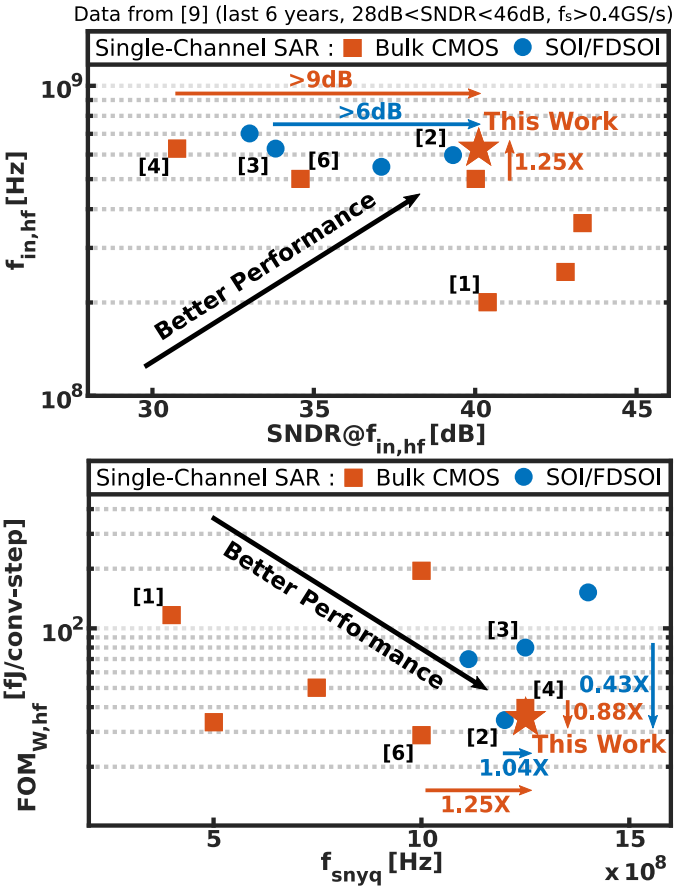

Fig. 8. Comparison with state-of-the-art single-channel SAR and one channel of TI-SAR ADCs based on [9].

VI. CONCLUSION

A 7b 1.25GS/s single-channel SAR ADC has been presented. The proposed bootstrap circuit for the input switch enables high input frequency linearity, while the USPC DAC and the Triple-Tail fully dynamic comparator enable short internal SAR-cycles, resulting in an increased sampling rate. The prototype achieves 40.1dB SNDR and 52dB SFDR at Nyquist, while at a 5GHz input frequency the SNDR and SFDR remain still 36.4dB and 50.1dB respectively, consumes 3.56mW from a 1V supply and occupies 0.0071mm^2 in 28nm CMOS, leading to a Nyquist FoM of 34.4fJ/conv-step.

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