High Speed Time-multiplexed Continuous Time Sigma-Delta Converters

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Abstract—**This paper presents a time-interleaved continuous time Sigma-Delta converter, which uses 4 identical channels clocked at equally shifted time moments of a 4 GHz clock. The data in each channel is filtered and afterwards recombined in a multiplexer, leading to an output signal at 4 GHz before decimation. Time-interleaving as proposed in this paper makes it possible to increase the signal-to-noise and distortion ratio (SNDR) in a specified bandwidth with 3 dB every time the number of channels is doubled. By exchanging the gain in accuracy for bandwidth, a high-speed Sigma-Delta converter with 250 MHz signal bandwidth and 65 dB SNDR is obtained in simulations. The simulated converter achieves a dynamic range of 72 dB and consumes 626 mW, leading to a Schreier FOM of 158 dB and a Walden FOM of 864.5 fJ/conv. This paper briefly discusses the different building blocks of the interleaved converter and their influence on the performance.**

Keywords—**Analog-to-digital conversion, Sigma-Delta modulation, interleaved data converters, bandwidth, SNDR**

I. INTRODUCTION

Analog circuits are moving to the front-end and back-end of current electronic applications. On the other hand, interface circuits in the form of analog-to-digital (ADC) and digital-to-analog (DAC) converters are gaining popularity. Flash-converters result in very large bandwidths (BW), whereas Sigma-Delta ($\Sigma\Delta$) converters achieve the highest precision. These accuracies are often expressed in signal-to-noise and distortion ratio's (SNDR) or effective number of bits (ENOB). High BW combined with high accuracy is still a challenge.

Block Digital Filtering [1], Hadamard $\Sigma\Delta$ modulation [2], and K-Delta-1-Sigma modulation [3] are some of the techniques mentioned in literature as 'time-multiplexed' Sigma-Delta converters. Despite their high gain in SNR (signal-to-noise ratio), extra complex blocks are needed next to the Sigma-Delta converters in each channel, which sometimes need to fulfill high speed-requirements. Furthermore, literature shows that channel mismatch in these time-multiplexed converters is important [3].

This paper explains the use of time-multiplexed $\Sigma\Delta$-converters to keep a high SNDR while achieving larger bandwidths in AD-conversion. The continuous time converter of this document uses the basic principle of time-interleaving in which M identical $\Sigma\Delta$-modulators and some simple digital blocks are used. The frequency of the output signal is only the sample frequency f_S of one channel due to the use of filters and a multiplexer for recombination of the channels' data.

Section II shows the theoretical concept of the time-interleaved $\Sigma\Delta$-converter. The system level implementation of the $\Sigma\Delta$-modulator is shown in section III, whereas section IV explains the building blocks at transistor level. Finally, results of Matlab [4] and Cadence Virtuoso [5] simulations are shown.

II. THEORETICAL CONCEPT: TIME-MULTIPLEXING

A. Basic principle

The basic principle of time-interleaving is shown in Fig. 1, in which T_S is the sample period. In this converter M identical Sigma-Delta modulators work in parallel on the same input signal. The clock in the different channels is shifted by T_S/M in such a way that each channel creates different samples. All data is interleaved at the output giving rise to a sample frequency of $M \cdot f_S$. After recombination, the data is decimated [6].
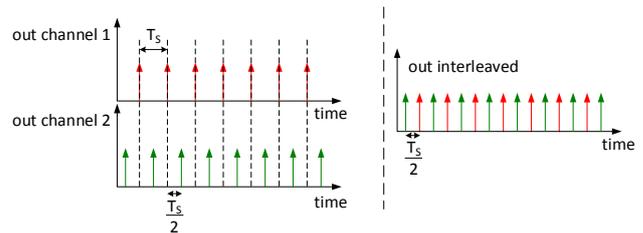

Fig. 1: Basic principle of time-multiplexing.

Assuming correlated signals in each channel, the signal powers of each channel V_{si}^2 add in amplitude as shown in equation (1), whereas the uncorrelated quantization noise V_{ni}^2 adds in power (2) [7]. Therefore the time-interleaved idea of Fig. 1 results in a 3 dB SNDR gain (= 0.5 bit) for each doubling in the number of channels (3), which can be traded for a higher bandwidth. Here $SNDR_1$ and $SNDR_{tot}$ are the SNDR of 1 channel, respectively the interleaved converter. The drawback of this structure is the high sample rate after recombination, imposing high requirements to the digital logic following the $\Sigma\Delta$-modulation.

$$P_{sig} \approx (V_{s1} + V_{s2} + ... + V_{sM})^2 \qquad (1)$$

$$P_{noise} \approx (V_{n1}^2 + V_{n2}^2 + ... + V_{nM}^2) \qquad (2)$$

$$SNDR_{tot} = \frac{P_{sig}}{P_{noise}} \approx \frac{(M \cdot V_{s1})^2}{M \cdot V_{n1}^2} \approx M \cdot SNDR_1 \qquad (3)$$

B. Adapted structure

The basic time-interleaved $\Sigma\Delta$-converter is adapted to the system in Fig. 2. Again, *M* identical Sigma-Delta modulators clocked at f_S are used in the different channels, generating data at shifted moments in time. Before recombining the data, the output signal of each channel is filtered. A multiplexer interleaves the channel-data into an output signal at sample rate f_S, this way creating an M times smaller sample rate than the basic time-interleaved converter of Fig. 2. The same 3 dB gain is possible.
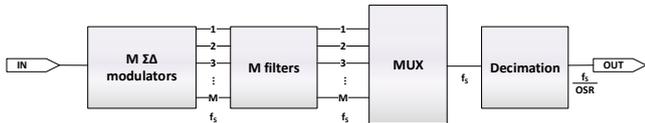

Fig. 2: Investigated time-interleaved structure.

Each of the different blocks in Fig. 2 influence the performance of the time-interleaved $\Sigma\Delta$-converter:

- $\Sigma\Delta$-*modulators*: The modulators in the different channels are identical, leading to simplicity of the proposed converter. In theory existing modulators can easily be plugged into each channel. Since time-interleaving can lower the quantization noise floor, but cannot remove noise in the signal band, each channel still needs to be able to process the desired bandwidth with sufficient accuracy. The high intended bandwidths demand amplifiers with a high gainbandwidth (GBW) and a large power consumption in each channel. Implementations at transistor level will show if the gain in BW and SNR is worth the extra power consumption.
- *Filters*: The sample frequency in Fig. 2 is never higher than f_S of one channel. This implicitly leads to a down-sampling since in total M samples are generated every period T_s. Filters are needed to avoid aliasing due to downsampling, which imposes a limit to the achievable bandwidth of the converter. Combining M channels in 1 multiplexer leads to the maximum bandwidth in eq. (4) due to aliasing. The transition band of the filters will limit the BW even more. Other data-recombination structures leading to a higher bandwidth are possible.

  Throwing *M-1* samples away every sample period seems contradictory in achieving higher SNDR and BW. The filters however provide averaging, which implies that data of the removed samples is combined in the taken samples and part of the quantization noise is already removed.

$$f_{BW,max} = \frac{f_S}{2 \cdot M} \quad (4)$$

- *Multiplexer*: The multiplexer recombines data of the different channels. The quantization noise is spread over a larger bandwidth since the bandwidth in each channel is limited by the filters and after the multiplexer, the bandwidth is $f_S/2$ again.
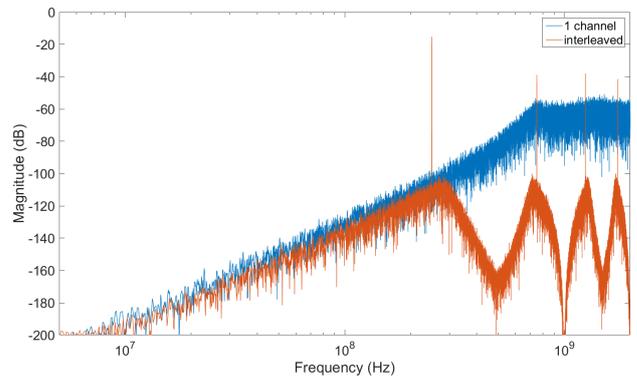- *Decimator*: Performs the decimation as in every Sigma-Delta converter. This part is assumed to be ideal.

Fig. 3: Amplitude spectrum of interleaved Sigma-Delta.

C. Trading SNR for BW

The system in Fig. 2 is implemented in Matlab. In each channel a third order 4-bit continuous time Sigma-Delta modulator with feed-forward structure is used with sample frequency of 4 GHz. The modulator type and f_S are based on [8], [9] in order to achieve the desired specifications of 250 MHz BW and 62 dB SNDR. A total of 4 channels are used for which the time-interleaved converter is able to achieve an extra 6 dB SNDR in the signal bandwidth. Since Sigma-Delta modulators already achieve a high SNDR, this gain is traded for more bandwidth by lowering the oversampling ratio (OSR).

Figure 3 shows the simulated output frequency spectrum of a 1 channel system and the proposed 4 channel system before decimation. Inside each channel a Butterworth filter with order 16, passband at 270 MHz and stopband at 500 MHz is used. The interleaved-converter achieves an SNDR of 71 dB inside a bandwidth of 250 MHz. The SNDR of this Matlab model is kept higher than the intended 62 dB, because non-idealities will degrade this performance. From the frequency spectrum in Fig. 3 it is clear that time-interleaving lowers the quantization noise floor. All effects in the spectrum at frequencies higher than 250 MHz are due to filtering and interleaving.

Theory shows that time-interleaving gives rise to AD-converters with higher BW and/or SNR. It is important to see the drawback of these improvements. Using M channels means that the power consumption will be M times higher than using only 1 channel. For high precision converters, the power-bandwidth-accuracy trade-off is best expressed by the Schreier figure-of-merit (5) from [10]. Here DR is the dynamic range corresponding to the ratio of the voltages at peak SNDR and 0 dB SNDR. The Walden FOM (6) can also be used, but this one is less appropriate for high precision converters. Since the power consumption (P) depends on the implementation of the Sigma-Delta modulators in each channel, the next 2 sections give the high- and low-level implementation details.

$$FOM_{Schreier} = DR[dB] + 10log\left(\frac{BW}{P}\right) \quad (5)$$

$$FOM_{Walden} = \frac{P}{2^{ENOB} \cdot 2 \cdot BW} \quad (6)$$

III. High-level design

Figure 4 shows the $\Sigma\Delta$-modulator used in each channel. Below follows a high-level discussion on the building blocks of Fig. 4.
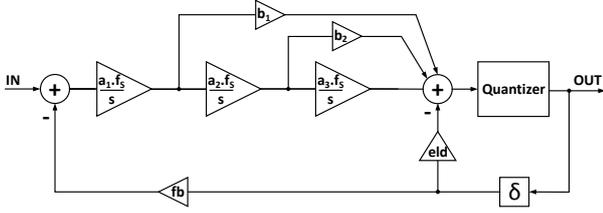

Fig. 4: Block-diagram of $\Sigma\Delta$-modulator in each channel.

A. Loop filter

Noise, linearity and signal swing are important for the first integrator in Fig. 4. An RC-integrator was determined to be the best option for these requirements [8]. For a better suppression of noise and non-linearities, an RC-integrator is also chosen for the 2nd integrator. Finite DC-gain A_{DC} of the amplifiers in the integrators limits the low frequency performance of the converter whereas the extra pole due to the finite GBW of the amplifiers results in instabilities. Table I shows the specifications for the first 2 amplifiers based on Cadence Virtuoso simulations with ideal blocks for the different parts in Fig. 4. Noise of the first integrator is important, since it is directly fed to the output without noise shaping. The resistance of the first integrator should be lower than 2.16 kΩ such that thermal noise will not dominate.

TABLE I:
Desired specifications for amplifiers in 1st and 2nd integrator.

$\mathbf{A_{DC,1}}$	$\geq 40 dB$
$\mathbf{GBW_1}$	10 GHz
$\mathbf{A_{DC,2}}$	$\geq 40 dB$
$\mathbf{GBW_2}$	≈ 7 GHz

The used feed-forward structure in the $\Sigma\Delta$-modulators calls for a gmC-integrator in the third stage. Signals are summed by adding currents and integrating them on a capacitance C_l. Furthermore noise and linearity are less important for this third stage, further justifying the use of gmC-integration.
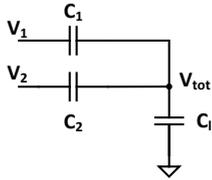

Fig. 5: Summation with capacitors.

The feed-forward in Fig. 4 demands a summation in front of the quantizer. An inverting amplifier and resistors allow to sum voltages at the expense of an extra power consuming amplifier

and less stability in the $\Sigma\Delta$-loop. Capacitive summation as shown in Fig. 5 is preferred in this high-speed converter [9]. Capacitors C_1 and C_2 create currents representing the differentiated version of the input voltages. These currents are summed and integrated on C_2, leading to the output voltage V_{tot} (7).

$$V_{tot} = \frac{V_1 \cdot C_1 + V_2 \cdot C_2}{C_1 + C_2 + C_l} \qquad (7)$$

Combination of the integrators and feed-forward results in the loop filter of Fig. 6. A differential structure is preferred due to its larger signal swing and eliminated even harmonics.
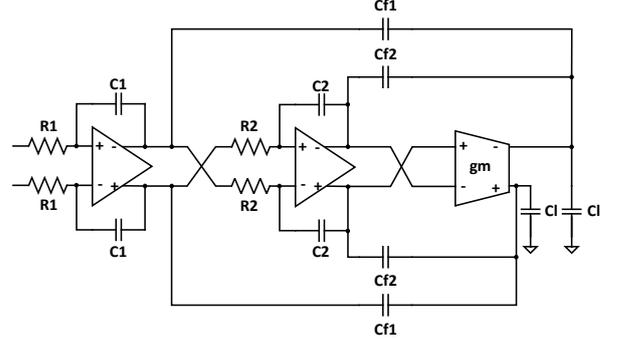

Fig. 6: Loop filter.

B. Quantizer and feedback

The system level choices for the other parts in Fig. 4 are briefly summarized:

- The quantizer requires a high speed low accuracy (4-bit) ADC. A flash-converter is preferred due to its high speed and basic implementation.
- Since summation of current is desired, a current-steering DAC is chosen in all feedback paths. This is also a fast implementation with limited mismatch. In case of too much mismatch, calibration techniques like Data Weighted Averaging (DWA) can be used [11]. The DAC uses non-return-to-zero pulses.
- Figure 4 shows a feedback path from the output of the $\Sigma\Delta$-modulator to the summation node in front of the quantizer for the compensation of excess loop delay (ELD). The capacitive summation leads to an integration of the current of the feedback DAC, which is undesired. A differentiation in the digital domain is added before the feedback-current is summed with the other signals.

Cadence Virtuoso simulations with each of the previous blocks implemented ideally achieve the same 250 MHz BW and 71 dB SNDR as the Matlab simulations.

IV. Low-level design

This part focuses on the transistor level implementation of the building blocks explained in the previous section. The amplifier used in the first 2 integrators is the same to reduce the design complexity. The feedback-DACs are implemented with ideal current sources, since this already gives a good approximation of the power consumption of this component.
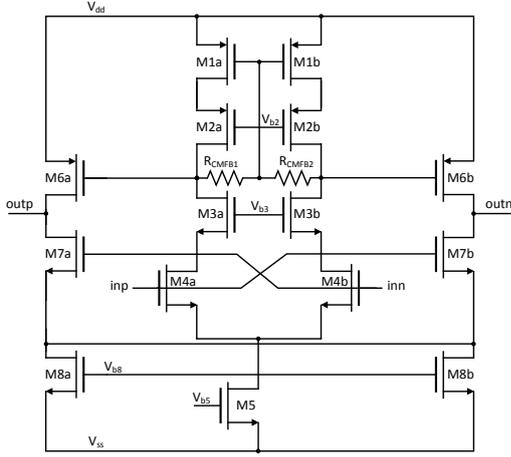
Fig. 7: OTA used in first and second integrator [12].

A. Integrator 1 and 2

The main performance limiting factors of the first 2 integrators are the gain and GBW as shown in table I. When implementing the amplifiers for the integrators at low level, one should also look at:

- Phase margin (PM): This specification should lie between 50° and 70°. Since the amplifier is used in feedback, instability could occur with a too low PM.
- Signal swing and linearity: The output swing of the amplifiers should be as high as possible together with a linear gain in order not to introduce harmonics.
- Noise: The noise contribution of the first amplifier is almost as important as the noise of the input resistance and feedback DAC. A directive based on noise calculations is to make the gm of the input stage larger than 155 μS.

Combining 40 dB DC-gain with a GBW of 10 GHz and enough phase margin asks for a deliberate design. Comparison of different amplifier structures shows that the OTA in Fig. 7 fits best for this converter. The telescopic OTA of the first stage and the second stage result in a high gain together with a high signal swing [12]. The feed-forward path formed by transistor $M7a$, $M7b$ and $M8a$, $M8b$ cancels the non-dominant pole of the amplifier by the creation of a zero. This leads to a better high-frequency behavior than using Miller compensation, because the latter splits the poles, but does not cancel them.
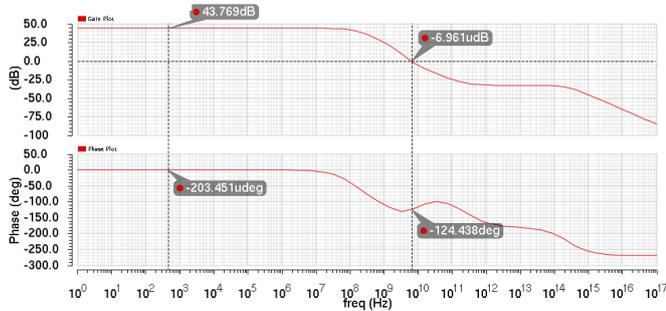

Fig. 8: Bode diagram of OTA in Fig. 7.

Using this OTA a gain of 43.8 dB, a GBW of 21.56 GHz and PM of 55° is obtained. The resulting bode-diagram is shown in Fig. 8. Since common-mode DC-problems often occur in differential circuits, an extra common-mode feedback (CMFB) circuit from the output to the gates of $M8a$ and $M8b$ is added to the OTA in Fig. 7 [13].

B. Integrator 3

The OTA for the third integrator demands a different design strategy, since gmC-integration desires a constant gm over the frequency band. This means that, when looking at the voltage gain of the OTA, the bandwidth is desired to be as low as possible, while the non-dominant pole should be as high as possible. Cadence Virtuoso simulations show that a basic differential pair as well as a cascode OTA and symmetrical OTA achieve the desired gm-specification, but create too much harmonic distortion (HD), due to their use in open-loop.

The OTA in Fig. 9 uses a distortion canceling technique proposed in [14]. The cross-coupled input pairs ($M3a$, $M3b$ and $M4a$, $M4b$) lead to a lower distortion while the cascode output stage gives the low bandwidth. According to formulas (8) to (11), it is possible to reduce the 3rd order intermodulation distortion (IM_3) to a minimum by choosing appropriate bias points. Taking α too high would lead to a high power consumption to achieve the desired gm and would give a higher sensitivity to V_{GS} variations, a value of 0.25 is advised [14].
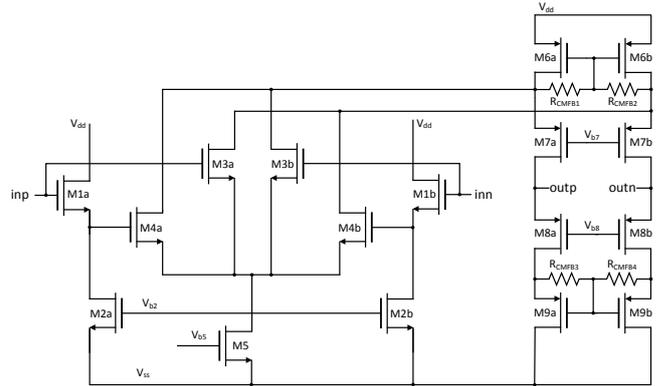

Fig. 9: OTA used in third integrator.

$$IM_3 \sim \frac{1 - \alpha v^3}{1 - \alpha v} \tag{8}$$

$$\alpha = \frac{I_{BIAS,4a,b}}{I_{BIAS,3a,b}} \tag{9}$$

$$v = \frac{V_{GST,3a,b}}{V_{GST,4a,b}} \tag{10}$$

$$I_{out} = gm_{3a,b} \cdot (1 - \alpha^{2/3}) \cdot v_{in} \tag{11}$$

C. Quantizer

As mentioned, a flash-ADC is chosen for the quantizer. This converter consists of a resistor-ladder with 16 resistors to generate the reference levels and 15 comparators.
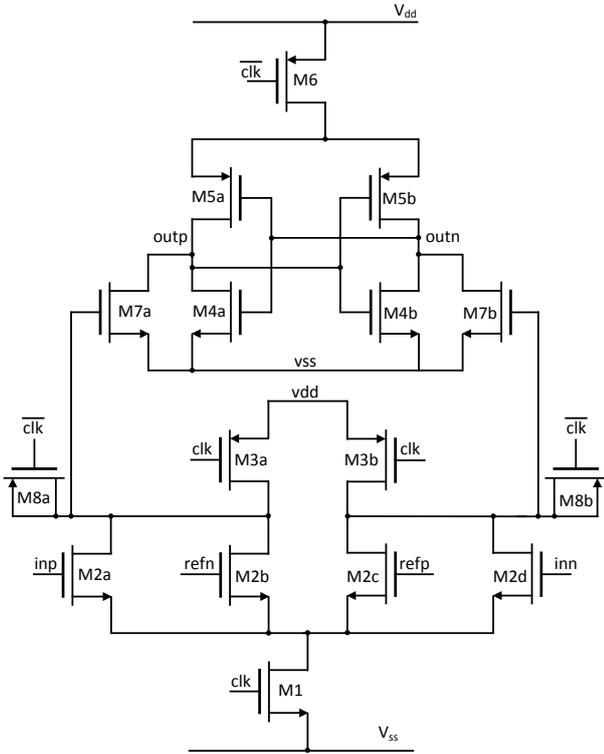Low noise and fast current delivery demand a small resistance

Fig. 10: Double-Tail Sense Amplifier [15].

value in the reference ladder. Low power requires a high resistance value. A value of 60 Ω is chosen as compromise. Extra capacitors on the other hand, are added to reduce the kickback noise. Calculations on the offset of the comparators based on the desired 4-bit resolution of the quantizer demand input transistors with $WL \geq 226 \cdot 10^{-15}$ m^2. The quantizer should decide in half a period of the 4 GHz clock (125 ps).

Each comparator consists of 3 elements:

- *Double-Tail Sense Amplifier (SA)*: This circuit, shown in Fig. 10, makes the decisions. A double-tail SA [15] is preferred over a StrongARM comparator [16]. The SA is faster than the StrongARM and requires for this design smaller input transistors, leading to lower kickback noise and a smaller load for the loop filter. The double-tail comparator makes correct decisions when the input difference is larger than 80 µV.
- *SR-latch*: The double-tail comparator in Fig. 10 resets its outputs every time the clock goes low. To keep the output of the quantizer at the right level, a set-reset latch is added. The double-tail with the SR-latch gives an average decision time of 76 ps.
- *Clocked SR-latch*: To lower meta-stability and to give the same decision moment every clock-period, a clocked latched is added. The clock of this latch is shifted from the clock of the double-tail comparator, so the total delay time is better matched to the 125 ps for which the ELD feedback is designed.

V. RESULTS

Cadence Virtuoso simulations of the 4-channel time-interleaved Sigma-Delta converter show that an SNDR of 65 dB with 250 MHz bandwidth is possible. The difference with the ideal 71 dB is due to the finite GBW of the amplifiers and the addition of noise (1 dB reduction). Simulations with the real quantizer are not possible due to problems with the simulator when using a combination of ideal and real circuits and an interface problem between the quantizer and DACs. The main goal of the low level implementation is to estimate the power consumption of the time-interleaved structure. Supposing the quantizer and DAC will not degrade the performance much, table II gives the achievable specifications of the time-interleaved converter.

TABLE II: Specifications of the time-interleaved system.

Specification	Value
Power consumption	625.96 mW
Energy consumption	156.49 pJ/conv.
BW	250 MHz
f_S	4 GHz
OSR	8
SNDR	65 dB
ENOB	10.5 bits
DR	72 dBV
Schreier FOM	158 dB
Walden FOM	864.5 fJ/conv.

Table III summarizes the power consumption of the total circuit. The digital filtering and decimation are assumed to be negligible compared to the consumption of the analog blocks. The total power consumption is about 626 mW, which is high but acceptable due to the well known power-accuracy-speed trade-off [17]. The most power consuming elements are the integrators. The GBW of the 2 first amplifiers is still higher than the specified values, which is why tuning of the transistor sizes will give a lower power consumption of the amplifiers. Probably some calibration will be needed for the DAC, which increases the power consumption again. 626 mW or 156.5 pJ/conv. can be taken as a good estimate for the consumption.

TABLE III: Power consumption of different parts of the time-interleaved ΣΔ-converter.

Component	Average Power	Energy per cycle
Integrator 1	59.3 mW	14.82 pJ
Integrator 2	59.3 mW	14.82 pJ
Integrator 3	6.4 mW	1.6 pJ
Quantizer	13.06 mW	3.26 pJ
DAC FB	1.43 mW	357.5 fJ
DAC ELD 1	8.5 mW	2.125 pJ
DAC ELD 2	8.5 mW	2.125 pJ
Total 1 channel	156.49 mW	39.12 pJ
Total time-interleaved	625.96 mW	156.49 pJ

A good way to compare the implemented converter with literature is by using a FOM (5). Figure 11 shows the Schreier FOM versus BW for state-of-the-art Sigma-Delta converters [18] and the time interleaved converter. The simulated time-multiplexed converter gives a higher BW and achieves a com-
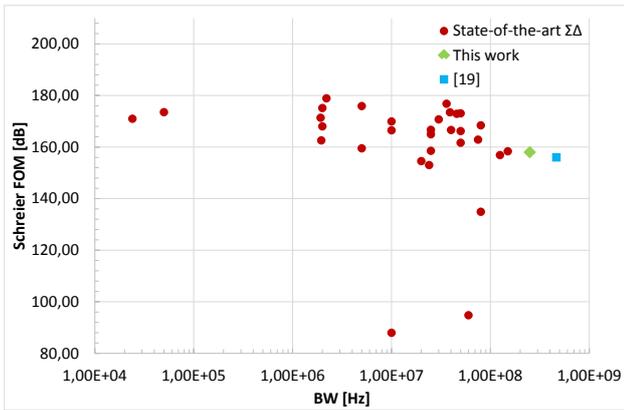
Fig. 11: FOM versus BW [18], [19].

parable FOM to the state-of-the-art converters. A recent publication [19] shows a continuous time Sigma-Delta converter with a 1-2 MASH structure, achieving the specifications in table IV. The Schreier FOM of the simulated time-multiplexed converter (158 dB) is a little better than the one of [19], which achieves 156 dB in a 3 times smaller technology. This is a first indication that time-interleaving is a good approach to achieve high bandwidths. Nevertheless, one should notice the better power-speed trade-off of the converter in [19]. The power consumption in the time-interleaved converter scales with the number of channels, whereas the BW does not scale in the same linear way due to noise shaping. This shows that there is still some room for improvement.

TABLE IV: Comparison of converter in this paper and [19].

Specification	This paper	MASH ADC [19]
BW	250 MHz	465 MHz
f_S	4 GHz	8 GHz
OSR	8	8.6
DR	72 dB	69 dB
SNDR	65 dB	65 dB
P	626 mW	930 mW
Walden FOM	864.5 fJ/conv.	690.5 fJ/conv.
Schreier FOM	158 dB	156 dB
CMOS L_{MIN}	90 nm	28 nm

Channel mismatches and component mismatches were modeled in Matlab. The time-interleaved structure is not more susceptible for mismatches than a single channel Sigma-Delta modulator. Simulations show that the performance of the time-interleaved converter only starts degrading when one of the channels starts to have a degradation in SNDR.

VI. Conclusion

This paper showed the theoretical concept of time-multiplexed Sigma-Delta converters. The high sample frequencies at the output were tackled by using filters and a multiplexer to recombine the data. The gain in SNR due to time-interleaving can be exchanged for a higher bandwidth.

A Sigma-Delta converter with theoretical SNDR of 71 dB and 250 MHz BW was designed in Matlab. The main drawback of this type of interleaving is the still high requirements for the modulators in each channel. This results in a difficult design of the amplifiers in the $\Sigma\Delta$-converters and an inevitable higher power consumption. Simulations with real integrators in the Sigma-Delta converter showed a degradation to 65 dB SNDR. Nevertheless, the BW of 250 MHz was still achieved. Comparing the simulated design to state-of-the-art shows a better performance for BW and a comparable FOM.

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