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Author contact	Maxime.dewit@esat.kuleuven.be + 32 (0)16 328745

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An F-band Active Phase Shifter in 28nm CMOS

Maxime De Wit, Patrick Reynaert
 KU Leuven ESAT-MICAS
 Kasteelpark Arenberg 10, 3001 Leuven, Belgium
 {maxime.dewit,patrick.reynaert}@esat.kuleuven.be

Abstract—In this paper an active phase shifter with high linear frequency dependency is presented for a FSK quadrature demodulator. The circuit is based on a coupled resonator to increase the linear phase shifting range and bandwidth. A capacitor bank, implemented as a digitally controlled artificial dielectric transmission line, is used to realize the phase shifting operation. The design methodology is explained and measurements of an implementation in a 28nm bulk CMOS are given. The design has a phase range of 123° and a phase resolution of 7.2° with a frequency dependent phase difference of $12.2^\circ/\text{GHz}$. The circuit occupies an active area of 0.01 mm^2 and draws a current of 9.5 mA from a 900 mV power supply.

Index Terms—Phase shifter, F-band, FSK, receiver, DiCAD

I. INTRODUCTION

The constant demand for higher data rates can be answered by going towards mm-wave frequencies and exploiting the readily available higher absolute bandwidth. As it becomes more challenging to design at mm-wave frequencies, where the available gain is limited by f_{max} , less complex modulation schemes tend to be more favorable. Although FSK is not the most bandwidth efficient modulation scheme, low-complexity and low-power modulation and demodulation structures can be implemented [1], [2]. A possible FSK receiver topology is based on a quadrature demodulator, as shown in figure 1. A frequency dependent phase difference between the two paths allows the mixer to act as a phase detector. The higher this frequency dependent phase difference, the more sensitive the receiver will be. As discussed in [1], the center frequency of the quadrature demodulator or transmitter might drift over time due to process and temperature variations, thus degrading the overall performance. Feedback from the baseband signal to the phase shifter can counteract this undesirable effect. This paper presents an active shifter, aiming for a wide bandwidth with a high and linear frequency dependent phase difference.

II. SYSTEM ARCHITECTURE

In this work, a coupled resonator is used to achieve a broadband and linear frequency dependent phase difference [3], [4]. The schematic is depicted in figure 2a, which consists of two Gm-stages and a transformer. The output (C_o , R_o) and input (C_i , R_i) impedance of the buffers are included in the resonator. Based on the derivation in [4], the influence of the k-factor on the bandwidth and phase are demonstrated in figure 2b. Tuning down the coupling factor of the transformer will result in a wide linear phase shift. The lowest coupling factor provides the highest frequency dependent phase shift. However, bandwidth decreases and the magnitude of the transimpedance drops drastically. A trade off rises between

Fig. 1. FSK quadrature demodulation architecture with a tunable frequency dependent phase shifter.

bandwidth and frequency dependent phase difference. Both of these elements also highly depend on the Q-factor of the entire resonator. High-Q inductors can be achieved by using the top routing metals. A variable capacitor (C_{var}) on both sides of the coupled resonator provides the phase shifting operation. Capacitors in the fF range can provide a decent tuning range while achieving high-Q values. A digitally controlled artificial dielectric transmission line (DiCAD) [5] can be considered as a distributed capacitor [6]. Routing parasitics are included and combined with the rest of the coupled resonator. A DiCAD and its equivalent distributed capacitor model are shown in figure 3. The capacitor C_{var} from figure 2a consists of the capacitance that is present within a transmission line and the extra capacitance formed by the underlying metal strips which can be included by using switching transistors.

III. IMPLEMENTATION

The coupled resonator structure is implemented as shown in figure 4. The primary (L_p) and secondary (L_s) inductors have an inductance of 115 pH and 137 pH with a Q-factor of 16 and 14, respectively. As can be seen in figure 4, the two inductors have a small overlap resulting in a k-factor of only 0.117.

The distributed capacitance bank is implemented as shown in figure 5. As the parasitic inductance will decrease the center frequency, it is paramount that the DiCAD is kept short to

(a)

Fig. 2. Schematic overview of the design with two buffers and a coupled resonator (a) and the magnitude and phase of the transimpedance Z_{21} for different values of k (b).

Fig. 3. Basic structure of a digitally controlled artificial dielectric transmission line and its distributed capacitance model.

provide sufficient tuning range at 120GHz. Since the lower metals are vertically closer to each other, this increases the capacitance for a given strip area, effectively decreasing the length of the DiCAD. The amount of strips per unit length of the DiCAD will determine the phase shifters' tuning resolution. Whereas the switches introduce parasitic capacitance, thus decreasing the tuning range and center frequency. In this design, a spacing of $4\mu\text{m}$ and $40\mu\text{m}$ in length with 16 strips make up the distributed capacitance bank.

In order to maximize the tuning range, the parasitic capac-

Fig. 4. 3D overview of the passive structure of the coupled resonator.

Fig. 5. The switch implementation which minimizes parasitics (a) and the simplified model used for design with the passive components. (b)

Fig. 6. A neutralized common-source stage used as a buffer within the frequency dependent phase shifter.

itance of the switch and the resistance in the ON state should be minimized. To achieve this, the switches are implemented as suggested in [7] and are shown in figure 5.

The two Gm-stages are implemented as neutralized common source stages and are shown in figure 6. As explained in [8], this technique improves the stability and gain at mm-wave frequencies. To keep the parasitic capacitance small and the Q-factor of the system high, the transistors were designed with a width of $5\mu\text{m}$ and minimal length.

In order not to influence the measured performance of the phase shifter, wideband input and output matching is desired. However, the high input and output impedances make wideband matching to 50Ω very challenging. Therefore, resistors in combination with transmission lines and transformers are used in the matching networks. As these resistors dissipate most of the input and output power, the measured gain of phase shifter will be lower than the actual performance.

Fig. 7. Magnitude (a) and phase (b) variation of the S21 for a gradual increase of the amount of switches which are ON.

IV. MEASUREMENTS

The phase shifter is measured on a probe station with a ZVA Rhode & Schwarz network analyzer and 90-140 GHz extenders. An input and output match under -10 dB from 92 GHz to 125 GHz is measured. The magnitude and phase of S21 are shown in figure 7. The phase shifting range is 123° with a resolution of 7.2° . The system has a frequency dependent phase difference of $12.4^\circ/\text{GHz}$. This measurement result agrees with full-chip simulations, indicating that the standalone coupled resonator also has a high frequency dependent phase difference. The maximum measured gain is -12 dB, which results in a de-embedded gain of 4 dB. In figure 8 the variation of the phase and magnitude for the center frequency are shown. Less than 3 dB of magnitude variation is achieved. The chip draws a current of 9.7 mA from a 0.9 V power supply. A die photograph is shown in figure 9. The chip has a size of $0.34 \times 0.74 \text{ mm}^2$ including the bondpads and a core resonator area of $0.2 \times 0.05 \text{ mm}^2$. A performance summary and comparison with state of the art are shown in Table I. Since the frequency dependent phase difference is of much less concern in other phase shifters, it is a difficult comparison. The design is nonetheless competitive on power, area, resolution and phase difference.

V. CONCLUSION

The design procedure and measurements of an active phase shifter with high linear frequency dependent difference were

Fig. 8. Magnitude and phase variation at the center frequency.

Fig. 9. Chip photograph of the implemented phase shifter with the core area highlighted.

presented in this paper. This design is suitable for an FSK quadrature demodulator where a high frequency dependent phase difference and accurate phase tuning are desirable, while consuming less power consumption and area in comparison with other phase shifters in the W-band and higher.

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TABLE I
COMPARISON OF RECENTLY PUBLISHED ACTIVE PHASE SHIFTERS FOR W-BAND AND HIGHER IN CMOS

	This work	[9]	[10]
Technology	28nm CMOS	28nm FDSOI	65nm CMOS
Frequency [GHz]	106-122	78.8-92.8	80-94
Resolution [$^\circ$]	7.2	22.5	22.5
Range [$^\circ$]	123	360	360
Gain [dB]	4*	2.3	3.8***
P_{DC} [mW]	8.73	21.6	43
Area [mm^2]	0.01	0.17	-
[$^\circ/\text{GHz}$]	12.4	12**	30***

* Input and output matching de-embedded

** Not mentioned in text, but extrapolated from figure

*** For the whole transmitter: phase shifter and PA

REFERENCES

- [1] H. Wang, M. Hung, Y. Yeh, and J. Lee. A 60-GHz FSK transceiver with automatically-calibrated demodulator in 90-nm CMOS. In *Symp. VLSI Circuits Dig. Tech. Papers*, pages 95–96, 2010.
- [2] W. Volckaerts, N. Van Thienen, and P. Reynaert. An FSK plastic waveguide communication link in 40nm CMOS. In *Digest of Technical Papers-IEEE International Solid-State Circuits Conference*, volume 58. IEEE, 2015.
- [3] H. Jia, B. Chi, L. Kuang, and Z. Wang. A 38-to 40-GHz current-reused active phase shifter based on the coupled resonator. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 61(12):917–921, 2014.
- [4] U. Decanis, A. Ghilioni, E. Monaco, A. Mazzanti, and F. Svelto. A low-noise quadrature VCO based on magnetically coupled resonators and a wideband frequency divider at millimeter waves. *Solid-State Circuits, IEEE Journal of*, 46(12):2943–2955, 2011.
- [5] T. LaRocca, S. Tam, D. Huang, Q. Gu, E. Socher, W. Hant, and F. Chang. Millimeter-wave CMOS digital controlled artificial dielectric differential mode transmission lines for reconfigurable ICs. In *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pages 181–184. IEEE, 2008.
- [6] D. Murphy, Q. J. Gu, Y. Wu, H. Jian, Z. Xu, A. Tang, F. Wang, and M. F. Chang. A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15. 3c transceiver. *Solid-State Circuits, IEEE Journal of*, 46(7):1606–1617, 2011.
- [7] W. Wu, J. R. Long, and R. B. Staszewski. High-resolution millimeter-wave digitally controlled oscillators with reconfigurable passive resonators. *Solid-State Circuits, IEEE Journal of*, 48(11):2785–2794, 2013.
- [8] D. Zhao and P. Reynaert. An e-band power amplifier with broadband parallel-series power combiner in 40-nm CMOS. *Microwave Theory and Techniques, IEEE Transactions on*, 63(2):683–690, 2015.
- [9] D. Pepe and D. Zito. A 78.8–92.8 GHz 4-bit 0–360 degrees active phase shifter in 28nm FDSOI CMOS with 2.3 dB average peak gain. In *European Solid-State Circuits Conference (ESSCIRC), ESSCIRC 2015-41st*, pages 64–67. IEEE, 2015.
- [10] I. Sarkas, M. Khanpour, A. Tomkins, P. Chevalier, P. Garcia, and S. P. Voinigescu. W-band 65-nm CMOS and SiGe BiCMOS transmitter and receiver with lumped IQ phase shifters. In *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, pages 441–444. IEEE, 2009.