Citation	Umut Çelik, Wouter Steyaert, Patrick Reynaert, 2017, A 230.5–238.8-GHz magnetically coupled triple-push oscillator with inductive tuning for data transmission in 45-nm CMOS Ph.D. Research in Microelectronics and Electronics (PRIME), 2017 13th Conference on, 185-188.
Archived version	Author manuscript: the content is identical to the content of the published paper, but without the final typesetting by the publisher
Published version	http://ieeexplore.ieee.org/document/7974138/
Journal homepage	http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=7964017
Author contact	umut.celik@esat.kuleuven.be + 32 (0)16 379122

(article begins on next page)

As discussed in [5], there is an optimal phase shift for every technology to design N-Push oscillators for maximum output power with high efficiency. For the predictive 45nm CMOS technology that is used, optimal phase is around 120 degrees up to 200GHz for NMOS transistors with the size of $12\mu m/45nm$. As a result, triple-push oscillator with

fundamental frequency between 70GHz and 90GHz is used to achieve third harmonic oscillation frequency above 200GHz.

Figure 1 shows the schematic of the circuit. NMOS transistors $M_1 - M_3$ are used for positive feedback to maintain the oscillation. If NMOS transistors are also used for switching, the tuning range is severely limited because of the high on resistance. It is caused by the high DC voltage at the drain of the transistors. Moreover, when switches are turned on, the on resistance varies considerably with the fundamental oscillation frequency and results in very high phase noise. When PMOS switches are used, the problem shifts to turning off however variation of the impedance over off resistance is much less for this case. Therefore, PMOS transistors $M_4 - M_6$ are used to switch L_{G2} on and off to change the oscillation frequency of the VCO.

B. Transistor Design

Transistor sizes are very important to determine power consumption and inductor sizes as well. If NMOS transistors are very large, parasitic capacitances are also very large which limits the inductance values in the LC tank for a certain oscillation frequency and it becomes harder to do inductive tuning. If they are very small then the negative resistance provided by NMOS transistors is not enough to meet Barkhausen's criteria because of the parasitic resistances of transmission lines and inductors. $12\mu\text{m}/45\text{nm}$ transistors are determined to be optimal to compensate for the losses as well as enabling inductive tuning for the VCO.

In [6], the advantage of roundtable layout is demonstrated compared to traditional layout for large transistor sizes to be used in power amplifiers however it is not known if this advantages on f_{max} exist for smaller transistors as well. Roundtable interconnects of the NMOS transistors are shown in Figure 2.

Fig. 2. Roundtable transistor interconnects

In the simulations that are done with roundtable layout and standard two fold layout f_{max} difference is less than 25GHz

but still results around 1.4dB output power difference. Because of this, roundtable layout is preferred for the transistors in this design.

PMOS transistors also contribute to the parasitic capacitances of oscillator's LC tank, therefore they need to be sized optimally as well. If they are very large, they limit the inductance values that can be implemented and especially C_{ds} becomes an issue, leaking signal to the L_{G2} even though the transistors are turned off. If they are very small, large on resistance limits the impedance variation when transistors are turned on which results smaller turning range. $12\mu\text{m}/45\text{nm}$ transistors sizes are determined to be optimal for PMOS switches.

C. Inductor Design

Inductors are the most crucial part of the VCO since the whole tuning range, output power, efficiency and phase noise is deeply influenced by the quality factors of the inductors.

The predictive 45nm CMOS technology that is used in this design has 11 Metal layers where three top layers are thick that allows higher quality factors to implement inductors.

Switchable inductor techniques are already used for mmwave VCOs: [8] and [9] utilize the guard rings for changing oscillation frequency. Guard rings are also commonly used to avoid coupling between different inductors. Although this technique can be used for single core VCOs at THz range as well, since they generally have very limited output power, it is not possible to achieve wide tuning range as well as high output power with this technique if magnetic coupling is desired to increase output power.

A new inductive tuning technique is proposed to enable both magnetic coupling as well as frequency tuning to achieve wideband, high output power VCOs in THz range.

Fig. 3. Proposed switched gate inductor

The proposed gate inductor has a width of $64\mu\text{m}$, length of $52\mu\text{m}$ and presented in Figure 3. Inductance value of L_{G1} is 50pH whereas L_{G2} is 30pH. EM simulations for each inductor and transmission lines are performed using ADS Momentum. Quality factors with PMOS transistors are given in Figure 4. As it can be seen, quality factor is 14.4 at 74.6GHz and 25.3 at 77.1GHz at the fundamental frequency. Resonance frequency of the gate inductors is above 400GHz which is high enough

to eliminate resonance at the third harmonic frequency. Slow-wave technique and combined multiple top metal layers are used to further improve the quality factors.

Gate inductor and switch parasitics can be modeled as in Figure 5. C_{sb} and C_{sg} of the $M_4/M_5/M_6$ always contribute to the LC tank no matter if the switch is turned off or on. In order to reduce the effect of C_{sg} , gate node of the PMOS needs to be very well shorted for ac signals so that the signal does not flow through C_{sg} and C_{gd} to form a path when the switch is turned off. Another crucial capacitance is C_{sd} . If it is very large then it is simply impossible to turn off PMOS switches due to potential signal leakage.

Fig. 4. Gate inductor models for when PMOS is switched off and on

Gate inductors restrict the area where drain inductors is needed to be implemented for triple-push configuration therefore, spiral drain inductor with multiple layers are used to achieve desired inductance values.

Fig. 5. Quality factors of gate inductors when PMOS is turned off and on

L_{choke} in Figure 1 is a quarter wave transmission line at the third harmonic to decrease the leakage of the signal through V_{DD} and it acts as an inductor for the fundamental and second harmonics. Metal layers from Metal 11 down to Metal 4 is used to reduce series losses of L_{choke} . Both Metal 1 and Metal 2 are used to shorten the length of L_{choke} by slow-wave technique. Metal strips have $1\mu m$ gap in between each other, and covers all substrate below the transmission line, minimizing substrate losses. C_{Block} in Figure 1 is used for DC blocking and output matching at the third harmonic to enhance output power.

D. Coupling Oscillators

Inductive injection locked coupling is preferred to couple VCOs which offers compact size, and minimal extra parasitic loading due to coupling.

Since it is not possible to couple VCOs from all gate inductors, only one inductor from each VCO is used for coupling as in [4]. In-phase coupling is preferred to couple VCOs. Coupling factor $k \approx 0.2$ is used to avoid any frequency locking issues that might be caused by process variation.

Fig. 6. Layout of the coupled triple-push VCOs

As it is seen from the layout in Figure 6, all supply feeding and output combination transmission lines are passed through coupled inductors and then other gate inductors are tuned to remove symmetry problems.

III. SIMULATION RESULTS

The proposed circuit is simulated in a predictive 45nm bulk CMOS technology. Both transient and modulated signal simulations are done. Firstly single core simulations are done afterwards two cores are magnetically coupled to increase output power. All transmission lines and inductors seen in Figure 6 are defined as multiple-port structures in ADS Momentum. Parasitic extraction up to the thick metal layers has been included for the transistors. Single core VCO achieves -12.6dBm output power at 224GHz and -12.4dBm output power at 231.4GHz whereas the two coupled VCOs achieve -10.5dBm output power at 238.8GHz and -12.3dBm output power at 230.5GHz. Total bandwidth of 8.25GHz is achieved. The simulated output spectrum for the coupled VCOs is given in Figure 7.

A 12.3Gbps data rate transmission is simulated with 0.67 modulation index. Output spectrum for data transmission is given in Figure 8.

All harmonics are below -35dBm. Compared to single core the output power is up to 1.9dB higher. It is below the theoretical 3dB increase. This suggests that further optimization is needed for coupling. Moreover, unwanted harmonics would decrease due to better waveform symmetry with further optimization. Worst case phase noise for coupled VCO is

TABLE I
COMPARISON WITH STATE-OF-ART CMOS VCOS ABOVE 200GHz

	This Work Single Core	This Work Coupled	[1]	[7]
Frequency [GHz]	231.4	238.8	240	210
P_{DC} [mW]	15.5	30.4	220	421
P_{OUT} [dBm]	-12.4	-10.5	0	-1.3
$P_{OUT,Var}$ [dB]	0.2	1.8	-	3.7 ¹
Tuning R. [%]	3.3	3.5	-	3.8
Phase N. [dBc/Hz]	-65.5@ 1MHz -94.6@ 10MHz	-67.2 -96.2	-105 -113	-86.7 -
Efficiency [%]	0.37	0.29	0.45	0.17
Mod. Tech.	BFSK	BFSK	QPSK	OOK
DataRate [Gbps]	11	12.3	16	10.7
Area [mm ²]	0.065	0.13	2	-
Tech	45nm pred.	45nm pred.	65nm	40nm

¹ Retrieved from graphs

-67.2dBc/Hz at 1MHz and -96.2dBc/Hz at 10MHz. A comparison table with state-of-the-art VCOs that are used for data transmission beyond 200GHz is given in Table 1.

Fig. 7. Coupled VCO output power spectrum

This is the first FSK implementation to transmit data above 200GHz in CMOS utilizing a switched inductor to the authors' knowledge. This VCO also has minimal output power variation over large bandwidth. All values are achieved with nominal 1.1 V power supply. Unlike [1] and [7], this design is scalable to achieve higher output powers depending on the requirements. Active area for coupled VCO is 0.13 mm². Area and design complexity is less than other implementations that are proposed in [1] and [7]. Area can further be reduced with replacing quarter wave transmission line with inductors that will be used for matching at the output at the expense of slightly reduced power.

Fig. 8. Output spectrum for 12.3Gbps data rate with coupled VCO

IV. CONCLUSION

A 238GHz magnetically coupled triple-push VCO with 3.5% tuning range for data transmission up to 12.3Gbps is presented. This paper suggests inductive tuning with CMOS technology above 200GHz is possible to achieve high data rates with FSK modulation. This is the first inductive tuning implementation that uses BFSK at THz range. Furthermore, proposed implementation offers scalability depending on the needs of the application in terms of output power. A novel inductor design is proposed for THz range CMOS VCOs that enables frequency tuning as well as magnetic coupling at the same time with good efficiency figures.

REFERENCES

- [1] S. Kang, S. V. Thyagarajan and A. M. Niknejad, "A 240GHz Fully Integrated Wideband QPSK Transmitter in 65nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 50, no. 10, pp. 2256-2267, 2015.
- [2] W. Steyaert and P. Reynaert, "A 0.54 THz Signal Generator in 40nm Bulk CMOS with 22 GHz Tuning Range and Integrated Planar Antenna," *IEEE Journal of Solid State Circuits*, vol. 49, no. 7, pp. 1617-1626, 2014.
- [3] D. Huang, T. R. LaRocca, M.-C. F. Chang, L. Samoska, A. Fung, R. L. Campbell and M. Andrews, "Terahertz CMOS Frequency Generator Using Linear Superposition Technique," *IEEE Journal of Solid State Circuits*, vol. 43, no. 12, pp. 2730-2738, 2008.
- [4] J. Grzyb and U. R. Pfeiffer, "A 228-GHz Lens Integrated Balanced Triple-Push Source in 65nm CMOS Technology," *IEEE Journal of Solid State Circuits*, vol. 48, no. 7, pp. 1751-1761, 2013.
- [5] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid State Circuits*, vol. 46, no. 3, pp. 583-597, 2011.
- [6] B. Heydari and P. Reynaert, E. Adabi, M. Bohsali, B. Afshar, M. A. Arbaban and A. M. Niknejad "A 60 GHz 90nm CMOS Cascode Amplifier with Interstage Matching," *Proceedings of 2nd European Microwave Integrated Circuits Conference*, pp. 88-91, 2007.
- [7] S. Moghadami, F. Hajilou, P. Agrawal, and S. Ardalan "A 210 GHz Fully-Integrated OOK transceiver for Short-Range Wireless Chip-to-Chip Communication in 40nm CMOS Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 5, pp. 737-741, 2015.
- [8] P.-L. You, and T.H. Huang "A Switched Inductor Topology Using a Switchable Artificial Grounded Metal Guard Ring for Wide-FTR MMW VCO Applications," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 759-766, 2013.
- [9] T.-H. Huang, P.-L. You, C.-H. Chiu and C.-Y. Wu "A Switched Inductor Topology Using a Switchable Artificial Grounded Metal Guard Ring for Wide-FTR MMW VCO Applications," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 759-766, 2013.