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Automatic Testing of Analog ICs for Latent Defects using Topology Modification

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Abstract—An automatic, defect-oriented method is proposed for activating latent defects in analog and mixed-signal integrated circuits. Based on the topology modification technique, added stress transistors generate voltage stress that activates these latent defects. This contrasts with burn-in testing which uses increased temperatures as a fault activation mechanism. Moreover, this Design-for-Testability algorithm gives the trade-off between fault activation rate, silicon area cost and testing time for different test solutions. Both CMOS and DMOS devices are handled to accommodate the testing of high-voltage circuits. When applied to latent gate oxide defects in a voltage regulator circuit, an activation rate of up to 76.7% is achieved. In comparison, the stressing by increased supply voltage only reaches 28%. For the same testing time, this improvement comes at the expense of three additional stress transistors with a silicon area overhead of less than 1%.

I. INTRODUCTION

As the automotive industry is pushing further towards autonomous vehicles, it becomes vital to ensure that the electronic systems controlling these vehicles never break down in the field. A breakdown may be caused by either parametric or catastrophic failures of one or more electronic components [1]. Digital integrated circuits (IC) can be tested with coverage rates close to 100%, while analog IC testing still shows much lower coverage rates [2].

Test methods and metrics have been developed to test analog circuits [3], [4]. However, these methods and metrics do not consider latent defects. To remedy this, burn-in testing is widely used to ensure a good reliability is burn-in testing, which is based on artificially aging the chips by increased temperature.

Fig. 1 shows a standard bathtub curve, which gives the failure rate of chips as a function of their lifetime [5]. Latent defects within a circuit may become catastrophic defects at any point throughout the lifetime of the chip. This paper aims at ensuring that no chips are in the field where such defects could occur during normal use. The core concept relies on activating the faults during production testing, thereby forcing these defects to show their effect during the early life.

An example production burn-in testing has a duration in the range of 24 hours, whereby special furnaces are used together with special sockets that can withstand temperatures that can reach over 150 °C [6]. This increases the test equipment cost, in addition to the high testing time. In order to reduce the total testing cost, burn-in testing has to be either improved

Fig. 1. Bathtub curve showing the failure rate during the life of a chip [5].

or completely replaced. In this way the testing time, the equipment cost or both can be reduced.

The need for high-voltage devices such as DMOS in the automotive industry has urged new methods to test this type of device. An example of such a method has been proposed using built-in test structures [7]. This method is part of the larger concept of built-in self test (BIST).

In the past, time-dependent failures, such as latent gate oxide breakdown, were considered more of a reliability issue [8], [9]. In that context, the reliability of digital CMOS circuits was characterized by methods using IC reliability simulators, such as BERT [10]. However, these methods still rely on burn-in testing.

In this paper, a novel method is presented that uses topology modification, which is based on adding additional stress transistors to a circuit. The proposed algorithm automatically finds the trade-off between fault activation rate, silicon area overhead and testing time. The method uses a well-known model for time-dependent dielectric breakdown to build this trade-off. In Section II the model for latent defects is described in more detail. Section III then outlines the methodology, i.e. how topology modification is used in the proposed algorithm to maximize the fault activation rate. In order to quantify the effectiveness of the proposed method, a case study is given in Section V. Finally, conclusions are drawn in Section VI.

II. FAULT MODEL

The proposed test method follows a defect-oriented approach where physical defects are represented by fault models. For latent defects in particular, the model must take into account the time aspect of the physical defect. In the

scope of with work, the model for time-dependent dielectric breakdown (TDDB) is used, however the method can be used for any kind of latent defect. TDDB has been studied and modeled in the past [8], [9], leading to the following expression for the time to breakdown τ_{BD} :

$$\tau_{BD}(T, V) = \tau_0(T) \cdot \exp\left(\frac{G(T) \cdot t_{ox,eff}}{V_{ox}}\right) \quad (1)$$

where the fitting parameters $\tau_0(T)$ and $G(T)$ only depend on the temperature T . For room temperature ($T = 300$ K), τ_0 and G are equal to 10^{-11} s and 350 MV/cm². The remaining parameters, $t_{ox,eff}$ and V_{ox} , are the effective oxide thickness and the voltage at this effective oxide thickness. This expression shows that both temperature and voltage can be used to decrease the time to breakdown. In the context of this work, voltage is chosen as the aging mechanism. In this way burn-in testing can be avoided.

In order to find an expression for required activation stress voltage V_{stress} , the model in (1) is used twice, first with (V_{nom}, τ_{life}) and second with $(V_{stress}, \tau_{test})$. Combining both results in the expression:

$$V_{stress} = \frac{\ln(\tau_{life}) - \ln(\tau_0)}{\ln(\tau_{test}) - \ln(\tau_0)} \cdot V_{nom} \quad (2)$$

where τ_{life} and τ_{test} are the required lifetime and testing time of the circuit and V_{nom} is the voltage across the oxide in nominal operation mode. τ_{life} is specified by the application of the circuit. τ_{test} is taken as variable, which leaves V_{nom} as a parameter that needs deeper analysis. Therefore, a closer look is taken at the different devices to find the values of V_{nom} .

Latent gate oxide breakdown is assumed to occur differently for CMOS and DMOS devices, therefore a distinction is made. The gate oxide of symmetrical CMOS devices can be stressed at the source side, the drain side and anywhere in between, as shown in Fig. 2(a). Here the simplification is made that each CMOS device can have two possible faults, one at the source and one at the drain side. This means that the required stress V_{ox} has to be calculated for both gate-source (V_{GS}) and gate-drain (V_{GD}) voltages. DMOS devices on the other hand do not have a symmetric source and drain, as shown in Fig. 2(b). Because of this, only faults at the source side of the transistor are considered.

III. METHODOLOGY

Based on the fault model presented in the previous section, a method is presented to optimize the activation of latent faults. First, the impact of different aspects of topology modification technique are explained. Then, optimality metrics of topology modifications are given, followed by the algorithm. The time complexity of the algorithm is given next. Finally, the test procedure is given, once topology modifications are chosen.

A. Topology Modification

The technique of topology modification to test circuits has been introduced in [12]. The idea is to enable different topologies $C_{mod,i}$ of a circuit C by adding transistors. The

Fig. 2. (a) CMOS and (b) DMOS device structures with designated doping regions. Adapted from [11].

addition of these stress transistors changes the behavior of the circuit when one or more stress transistors are turned on, resulting in voltage stress within the circuit. If the stress transistors are added between a node and supply voltage or ground, they are called pull-up (PU) or pull-down (PD) transistors. The impact of topology modification on the design of the circuit and controllability of the stress transistors is discussed further.

1) *Design stage*: As this is a DfT solution, the designer must account for the impact that the added transistors have on the design of the circuit. Certain RF circuits, for example, have nodes that are easily influenced by adding additional capacitance, which may reduce the performance of the circuit. This influence also depends on the used technology. Older technologies are less influenced compared to newer ones [13]. This possibly means that some nodes should remain unmodified, thus being excluded from the list of possible nodes. Exclusions depend on the circuit and its specifications and are taken into account by the proposed method.

2) *Controllability*: The behavior of the nodes is defined as either normal use, pull-up or pull-down. This is controlled by the gate of the stress transistors. Which, in turn, are controlled by shift registers with drivers, which was also introduced as the preferred solution in [12]. This control method only needs two test pads and has digital control circuitry whereby the state of the testing transistors can be scanned out. The main advantage is the limited number of necessary test pads, but it brings more complexity and more area overhead to the circuit.

B. Metrics of optimization

Three metrics of optimization are introduced to quantify the merit of a topology modification. The first one is the fault activation rate, i.e. the number of faults activated divided by

the total number of possible latent faults. The other two metrics are related to the cost of a topology modification. This cost is, on the one hand, the time required to perform a test with a certain topology modification, and on the other hand the cost of extra silicon area due to the stress transistors. These two different aspects of testing cost can be combined together if the financial value of both aspects is known. In the following developments, the two costs are handled separately in order to maintain generality.

In the scope of this paper, the added cost of controlling the stress transistors will be omitted from the cost calculation. This decision is made because the choice of either digital shift registers or dedicated test pads is an option to the circuit designers. This also depends heavily on the circuit, its function and the technology used. If this cost is quantified, the additional cost can easily be added to the cost function described above.

C. Algorithm

The proposed algorithm consists of five successive steps. Given a circuit C presenting K nodes $\{N_1, N_2, \dots, N_K\}$ and J transistors $\{T_1, T_2, \dots, T_J\}$:

Step 1) The nominal voltage $V_{nom,k}$ for each node N_k and maximum safe current $I_{max,j}$ for each transistor T_j with $k = 1, \dots, K$ and $j = 1, \dots, J$ are calculated.

Step 2) Topologies $C_{mod,l}$ with $l = 1, \dots, 2K$ are generated such that for each node N_k ($k = 1, \dots, K$) there is a topology with a PU and a PD transistor connected to that node. If there are violations of the electrical design rules of the technology for at least one T_j , the topology supply voltage $V_{supply,l}$ is decreased by V_{step} until violations no longer occur, then the currents $I_{j,l}$ through each transistor T_j ($j = 1, \dots, J$) for each topology $C_{mod,l}$ are calculated.

Step 3) For each topology $C_{mod,l}$ ($l = 1, \dots, 2K$) and for each transistor T_j ($j = 1, \dots, J$) the design-specific rules and the condition $I_{j,l} > \alpha \cdot I_{max,j}$ are checked, $C_{mod,l}$ is removed if any condition is not satisfied.

Step 4) The stress voltage $V_{stress,j}$ is calculated for each transistor T_j ($j = 1, \dots, J$) in function of testing time τ_{test} and used to find all activated transistors T_j for each topology $C_{mod,l}$ ($l = 1, \dots, 2K$).

Step 5) A genetic optimizer is used to select a number of $C_{mod,l}$, resulting in pareto-optimal test solutions, each with a silicon area cost, testing time and activation rate.

First, in step 1, the circuit is characterized in its nominal mode. Each transistor T_j is extracted and simulated using the highest allowed voltages for that transistor, which are specified by the technology. This simulation gives the maximum allowed current through each transistor $I_{max,j}$, which is used in step 3.

Next, during the step 2, the circuit topology is modified by adding PU or PD transistors to circuit nodes as proposed by the topology modifications technique described in Subsection III-A. The result is $2K$ different topologies $C_{mod,l}$ where the stress transistor are all minimally sized. In circuits that use more than one voltage domain, such as voltage regulators,

nodes can be pulled up to different voltages. In this last case, DMOS transistors can be used to facilitate pulling nodes from voltage domains that are too high for ordinary CMOS transistors. However, the use of DMOS devices comes at the cost of a larger silicon area overhead [11]. Pulling certain nodes to higher voltage domains can result in damageable voltages across certain devices, depending on the used technology. In order to deal with this, the supply voltage $V_{supply,l}$ is decreased in steps of V_{step} for each topology $C_{mod,l}$ until there is no longer a problem.

In step 3, every alternative topology is explicitly checked for violations of design-specific rules. The currents $C_{j,l}$ are also checked by comparing them to the calculation of $I_{max,j}$ in step 1. This work assumes that the currents during stress can be higher than the maximum safe values. The algorithm accounts for this with the factor α , which is a design choice. In the implementation this is chosen to be 10.

During step 4, the required voltage stress $V_{stress,j}$ is calculated for each transistor according to the equations described in Section II. The set of $V_{stress,j}$ is then used to calculate the activation rate for each topology $C_{mod,l}$ as a function of the testing time.

Finally, in step 5, the results from step 4 are used to create test solutions. Such a test solution is characterized by a number of topology modifications, which have a certain area cost, testing time and activation rate. The selection process itself is carried out by means of a multi-objective optimization system [14], which aims at maximizing the activation rate, while minimizing both the area cost and the total testing time. This genetic optimizer generates a set of pareto-optimal test solutions. This means that every solution in this set is better than any other test solution for at least one objective. The main benefit of using this type of optimization is that a number of test solutions are given, instead of only one, allowing more flexibility to the designer by giving more options.

D. Time complexity

An expression for the calculation time needed by the algorithm can be found by analyzing the amount of time the entire circuit is simulated. Steps 1, 3 and 4 of the algorithm have negligible calculation. Step 2, however, requires a number of simulations for each topology modification. The following expression gives the worst case total number of simulations: $2K \cdot \left(\frac{(V_{upper} - V_{lower})}{V_{step}} + 1 \right)$ where $2K$ is the number of single topology modifications, V_{upper} and V_{lower} are the upper and lower limit of voltage supplies and V_{step} is the amount with which the supply is decreased. The final step consists of running a genetic optimizer whose implementation has a time complexity of $\mathcal{O}(G \cdot M \cdot P^2)$, where G is the number of generations, P the population size and M the number of objectives [15].

In conclusion the time complexity of the algorithm is mainly determined by the circuit size on one hand and by the desired accuracy of the solution on the other. The circuit size is expressed in the number of nodes and affects the calculation

Fig. 3. (a) Cascoded common-source amplifier based on [18]. (b) Available nodes for modification. (c) All possible modifications. (d) Optimal set of modifications.

time of step 2. The accuracy is a design parameter and has an effect on both steps 2 and 5.

E. Fault activation procedure

The actual fault activation procedure consists in completely turning each stress transistor on and off one after another. For each stress transistor the stress duration and supply voltage are determined by the proposed algorithm. If there is more than one stress transistor, the sequence can be determined trivially by the lowest supply first, thereby minimizing the supply ramp time.

Detection relies on the creation of new ohmic connection in the transistor [16] when defects are activated. These defects can be modeled by gate-source or gate-drain shorts, which are part of the 5-fault model of MOSFETS. There are already techniques proposed to detect such faults [1], [17]. Therefore, this work will further focus on the fault activation aspect only.

IV. THEORETICAL EXAMPLES

Before tackling industrial circuits, a simple circuit is analyzed in order to validate the concept of the proposed algorithm. This circuit is shown in Fig. 3(a) and is based on [18]. This circuit is a cascoded common-source amplifier, consisting of only four transistors, two of p-type and two of n-type. A predictive 0.18 μm technology [19] is used to simulate this circuit. For the sake of simplicity, the assumption is made that only the ground and supply nodes can be accessed through pins. Furthermore, nodes with bias voltages such as V_{IN} and V_{BIAS} cannot be modified. Fig. 3b shows the remaining nodes that are eligible to be used by the proposed algorithm.

Increasing the supply voltage beyond the nominal voltage is used as the benchmark method of the fault activation. For the example circuit this is done by increasing the supply voltage from 1.8 V to 2.5 V and 4 V. This results in an activation rate of 25% for both cases, as shown in Table I.

The algorithm, as explained in Subsection III-C, is then used to produce the set of pareto-optimal topology modifications. The testing time per transistor (τ_{test}) is limited to 1 s to simplify the necessary calculations. First, the circuit is simulated

TABLE I
ACTIVATION RATE AND AREA COST OF CASCODED AMPLIFIER

Activation method	Activation rate [%]	Area increase [%]
Increase supply to 2.5V	25	0
Increase supply to 4V	25	0
Proposed algorithm		
Test solution 1	25	0.25
Test solution 2	50	1
Test solution 3	62.5	1.25
Test solution 4	75	3.4

in the nominal operating mode, as shown in Fig. 3(a). From this, V_{stress} is calculated by taking a circuit lifetime τ_{life} of 1 hour. Then, all the possible modifications are generated. These transistors are the gray transistors shown in Fig. 3(c). This technology uses only one voltage domain, which is 1.8 V and as such no supply voltage reduction is required. From these stress transistors, different subsets of stress transistors are chosen as shown Table I. The solution that costs the least has the same activation rate as increasing the supply voltage beyond nominal levels. However, for a higher cost of silicon area, activation rates up to 75% can be reached. Finally, the test solution with the highest activation rate is shown in gray in Fig. 3(d).

V. CASE STUDY

An industrial circuit is analyzed by the proposed algorithm, its schematic diagram is illustrated in Fig. 4 and is adapted from [17]. This circuit is a voltage regulator used in the automotive industry with a power supply voltage of 12 V, which typically comes from a car battery. It is chosen because it presents CMOS and DMOS devices of both p-type and n-type. This circuit is implemented in ON Semiconductor's I3T50 technology, which is a 0.35 μm technology. Also, only the supply, the ground and the regulated output are externally accessible; all other internal nodes are candidate to be used by the algorithm. Furthermore, the regulated output

Fig. 4. Schematic diagram of the regulator used as a case study [17]. In gray are the stress transistors needed to reach 76.7% activation rate with 8 ms total testing time and 0.756% area cost. The required supply voltage for each stress transistors is also given.

Fig. 5. Constant Voltage stress using different stress durations.

can potentially be used as a pull-up voltage source for low-voltage nodes. As this is a circuit for the automotive industry, the lifetime assumption is made that a vehicles has 4000 hours of active lifetime.

Analogous to Section IV, a benchmark is set using constant voltage stress. This is done for supply voltages ranging from 15 V to 40 V and for testing times ranging from 10 ms to 1000 ms. Fig. 5 shows the corresponding activation rates. For the aforementioned parameters, this rate does not reach values higher than 35%, with 40 V supply voltage and 1000 ms testing time.

The set of pareto-optimal test solutions is shown in Fig. 6. The test solutions are grouped by their cost in silicon area, which is determined by the type and number of stress transistors. In this figure the type and number of stress transistors used in each group are indicated by #C+#D, which stands for the number of CMOS and DMOS stress transistors re-

Fig. 6. Test solutions with their fault activation rate in function of testing time. Each group of solutions has the same area cost. #C and #D indicate the number of CMOS respectively DMOS devices for each group.

spectively. Even though the PU and PD transistors are all minimally sized, the difference between the size of CMOS and DMOS transistors is significant. Nevertheless, the silicon area overhead does not exceed 1.5%, because of the relatively large DMOS transistors already present in the circuit.

The lower and upper limits of the testing time per stress

TABLE II
TEST SOLUTIONS WITH HIGHEST ACHIEVED ACTIVATION RATE

Act. rate [%]	Area cost [%]	Testing time [ms]	Stress transistors [#C+#D]
76.7	1.507	5	2C+2D
76.7	0.756	8	2C+1D
76.7	0.754	32	1C+1D

transistor are set to 1 ms and 50 ms. ATE voltage settling times are neglected in the calculation. Their effect weighs more with test solutions that have more than one stress transistor. If these settling time would be known, however, they can easily be taken into account in the total testing time for each solution.

The total runtime of the algorithm for this case is approximately 27 minutes. This is dominated by steps 2 and 5, described in Subsection III-C, which take 21 and 5 minutes respectively. The runtime of the other steps combined is less than 1 minute.

It is expected that in the automotive industry the highest possible activation rate is required. To this end, these test solutions are given in Table II. The trade-off is therefore reduced to the silicon area cost versus the total testing time. As a practical example, the 2C+1D test solution is chosen. The argument is that a very small increase in the area cost (a single, minimal-size CMOS transistor), has 4 times lower testing time compared to the 1C+1D solution. Increasing the area cost even further by adding an extra DMOS stress transistor reduces the testing time by only 3 ms. The hardware implementation corresponding to the 2C+1D solution is shown by the gray transistors in Fig. 4.

In real applications, the trade-off between silicon area versus testing time can better be expressed by calculating the cost of the time required on the ATE against the silicon area cost. Additional restrictions on time or area can be further introduced when all other tests are determined.

VI. CONCLUSION

This work has presented an algorithm to generate test solutions for activating latent defects in analog and mixed-signal ICs. The development has been presented for circuits consisting of CMOS and DMOS devices. As a result, the method generates a set of test solutions that are pareto-optimal in terms of area cost, testing time and fault activation rate. Furthermore, the algorithm also takes into account restrictions set by both the technology used and the design itself. This allows a circuit designer to finally choose a test solution that best fits the design and the use of the considered circuit.

For the industrial case study of a voltage regulator circuit, an activation rate of 76.7% is achieved for latent gate oxide defects. This activation rate is reached by 3 different pareto-optimal test solutions with total testing times down to 5 ms and silicon area overhead down to 0.754%.

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REFERENCES

- [1] S. Sunter and N. Nagi, "Test metrics for analog parametric faults," in *Proceedings 17th IEEE VLSI Test Symposium (Cat. No. PR00146)*, 1999, pp. 226–234.
- [2] W. Dobbelaere, R. Vanhooren, W. D. Man, K. Matthijs, A. Coyette, B. Esen, and G. Gielen, "Analog Fault Coverage Improvement using Final-Test Dynamic Part Average Testing," in *Proceedings. International Test Conference*, 2016.
- [3] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature Testing of Analog and RF Circuits: Algorithms and Methodology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1018–1031, May 2007.
- [4] H. G. Stratigopoulos, "Test Metrics Model for Analog Test Development," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 1116–1128, July 2012.
- [5] W. B. Nelson, *Applied life data analysis*. John Wiley & Sons, 2005, vol. 557.
- [6] W. Kuo and Y. Kuo, "Facing the headaches of early failures: A state-of-the-art review of burn-in decisions," *Proceedings of the IEEE*, vol. 71, no. 11, pp. 1257–1266, Nov 1983.
- [7] V. Malandrucolo, M. Ciappa, W. Fichtner, and H. Rothleitner, "Novel Solution for the Built-in Gate Oxide Stress Test of LDMOS in Integrated Circuits for Automotive Applications," in *2009 14th IEEE European Test Symposium*, May 2009, pp. 67–72.
- [8] J. C. Lee, C. Ih-Chin, and H. Chenming, "Modeling and characterization of gate oxide reliability," *IEEE Transactions on Electron Devices*, vol. 35, no. 12, pp. 2268–2278, Dec 1988.
- [9] T. Kim and W. Kuo, "Modeling manufacturing yield and reliability," *IEEE Transactions on Semiconductor Manufacturing*, vol. 12, no. 4, pp. 485–492, Nov 1999.
- [10] R. H. Tu, E. Rosenbaum, W. Y. Chan, C. C. Li, E. Minami, K. Quader, P. K. Ko, and C. Hu, "Berkeley reliability tools-BERT," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 10, pp. 1524–1534, Oct 1993.
- [11] S. Sze and M.-K. Lee, *Semiconductor Devices : Physics and Technology*, 3rd ed. Wiley, 2013.
- [12] A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, "Automated testing of mixed-signal integrated circuits by topology modification," in *2015 IEEE 33rd VLSI Test Symposium (VTS)*, April 2015, pp. 1–6.
- [13] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1036, Jul 1998.
- [14] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation*, vol. 6, no. 2, pp. 182–197, Apr 2002.
- [15] M. T. Jensen, "Reducing the run-time complexity of multiobjective EAs: The NSGA-II and other algorithms," *IEEE Transactions on Evolutionary Computation*, vol. 7, no. 5, pp. 503–515, Oct 2003.
- [16] J. W. McPherson, R. B. Khamankar, and A. Shanware, "Complementary model for intrinsic time-dependent dielectric breakdown in sio2 dielectrics," *Journal of Applied Physics*, vol. 88, no. 9, pp. 5351–5359, 2000.
- [17] A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, "Automatic generation of lightweight controllability and observability structures for analog circuits," in *2015 SMACD*, Sept 2015, pp. 1–4.
- [18] W. M. Sansen, *Analog design essentials*. Springer Science & Business Media, 2007, vol. 859.
- [19] N. Krishnapura, <http://aiweb.techfak.uni-bielefeld.de/content/bworld-robot-control-software/>, 2012, [Online; 1-November-2016].