A 65 nm Analogue front-end for a RAD-HARD Single-Shot Time-to-Digital Converter with 8 ps resolution

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1. Introduction

Time-to-digital converters (TDCs) have recently gained interest due to technology scaling and the need for more accurate time measurements. With decreasing transistor dimensions, the power supply voltage also decreases, which limits the dynamic range of, for instance, Analog-to-Digital Converters (ADCs). One solution to this problem is to digitize an analogue time instead of a voltage and move from ADCs to TDCs.

TDCs prove to be useful in a lot of applications, like time of flight (ToF) measurements and high-energy physics [1]. Furthermore, a TDC can be used to digitize the phase error of an oscillator or to sense timing skew. In this abstract a radiation tolerant TDC is proposed, which can be used in harsh environments [2] [3] [4]. The TDC is designed in 65 nm CMOS and has a simulated resolution of 8 ps. The analogue part is surrounded by a delay locked loop (DLL) in order to compensate for possible external influences like temperature, ageing and radiation and to cope with intrinsic process variability [5] . Other techniques, which result in a fast recovery from a single event upset (SEU), a short conversion time and a more precise time measurement, will be discussed in this abstract. First the different blocks of the analogue front-end of the TDC will be described. Next simulation results will be discussed and finally, conclusions are drawn.

2. Analogue TDC core blocks

To acquire a stable time measurement, the analogue front-end is based on a delay locked loop (DLL). An overview of the analogue front-end of the TDC is shown in Figure 1. The DLL continuously ensures that the delay line is synchronised to the reference clock. This is done by the phase detector (PD) and the charge pump (CP). The PD will measure the phase difference between its two input signals. According to this phase difference the charge pump is switched to change the control voltage, steering the total delay of the delay line in the right direction.

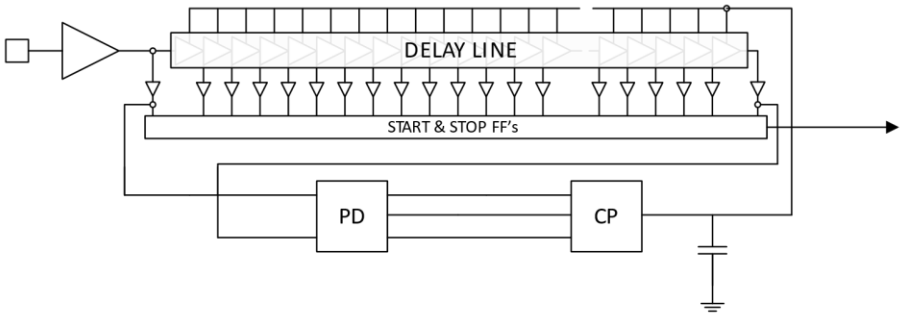

Figure 1: General diagram of the analogue TDC front-end

a. Phase Detector

The phase detector proposed in this design has two important features: (1) the ability to generate four different output levels, depending on the time difference at the input and (2) an extremely low hysteresis. The first feature results in the ability to distinguish the phase between two signals in four levels: *very-early*, *early, late*, and *very-late*. The transfer function of the PD is shown in Figure 2. The four levels are achieved by use of a small TDC with only two delay elements, the output of this small TDC represents the four different modes. In the larger TDC these modes are used to quickly recover from an out of lock state, which can happen in case of a SEU, where it will take much longer for a regular bang-bang PD to recover. An example of this fast recovery is shown in Figure 4. In this simulation, the different modes of the PD can clearly be distinguished. In the beginning, the loop filter of the DLL has a low control voltage, which results in a small delay. The PD detects this very-small delay and turns on the large charge pump which results in a quick adjustment of the delay line. When eventually the delayed signal enters the early-late range, the fast charge pump is switched-off and only small adjustments are applied. By using this principle, the DLL is able to recover from a SEU in less than 2 µs.

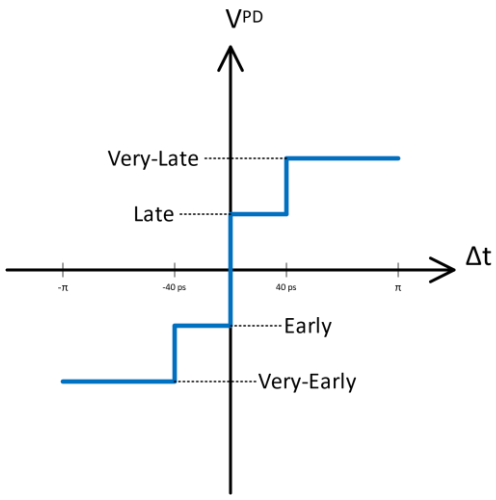

Figure 2: Transfer function triple level phase detector

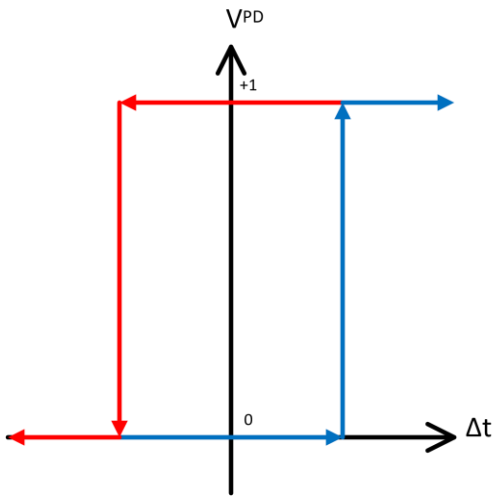

Figure 3: Bang-bang phase detector in hysteresis

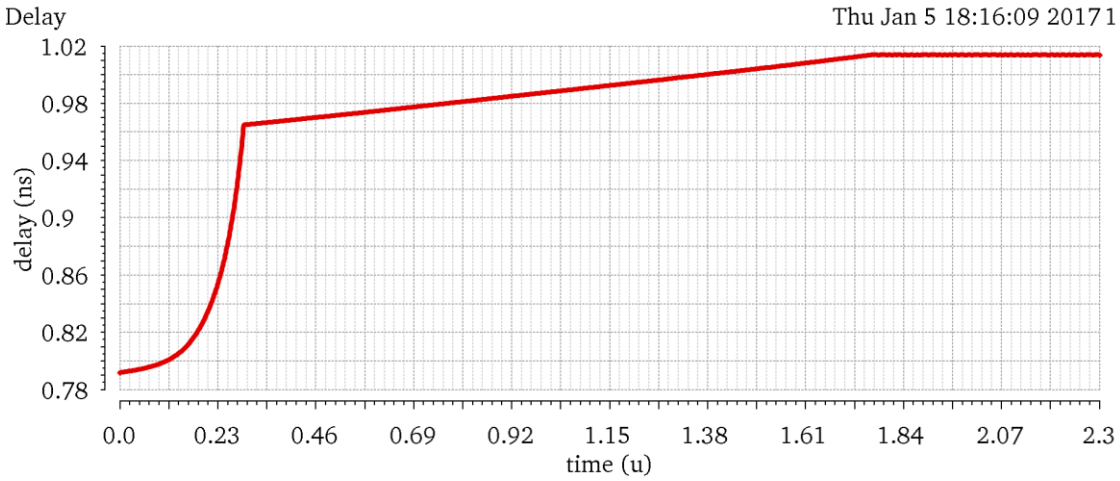

Figure 4: Delayed signal in DLL start-up

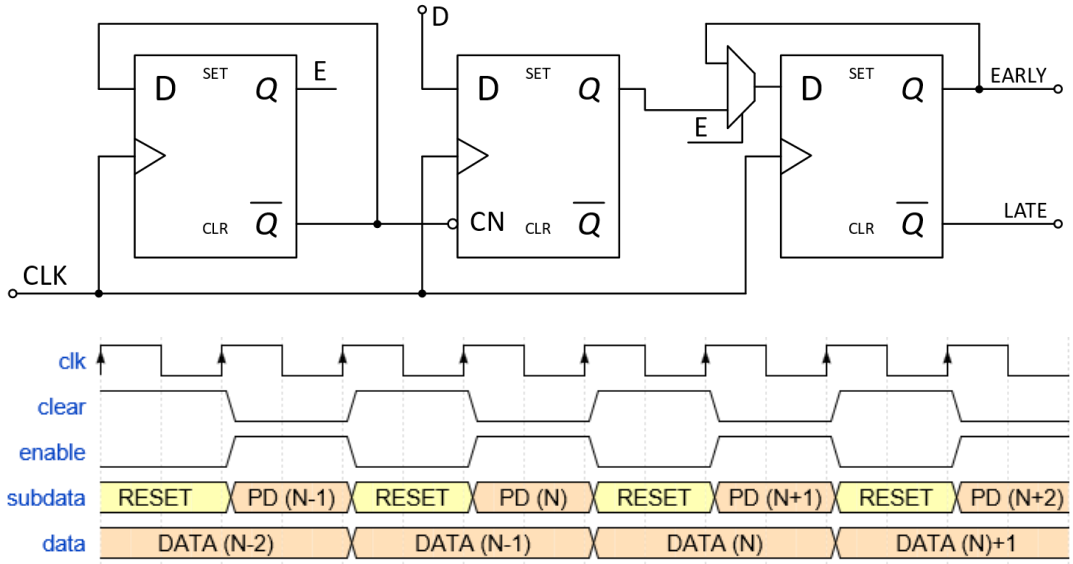

Figure 5: Signal waveform of low hysteresis phase detector

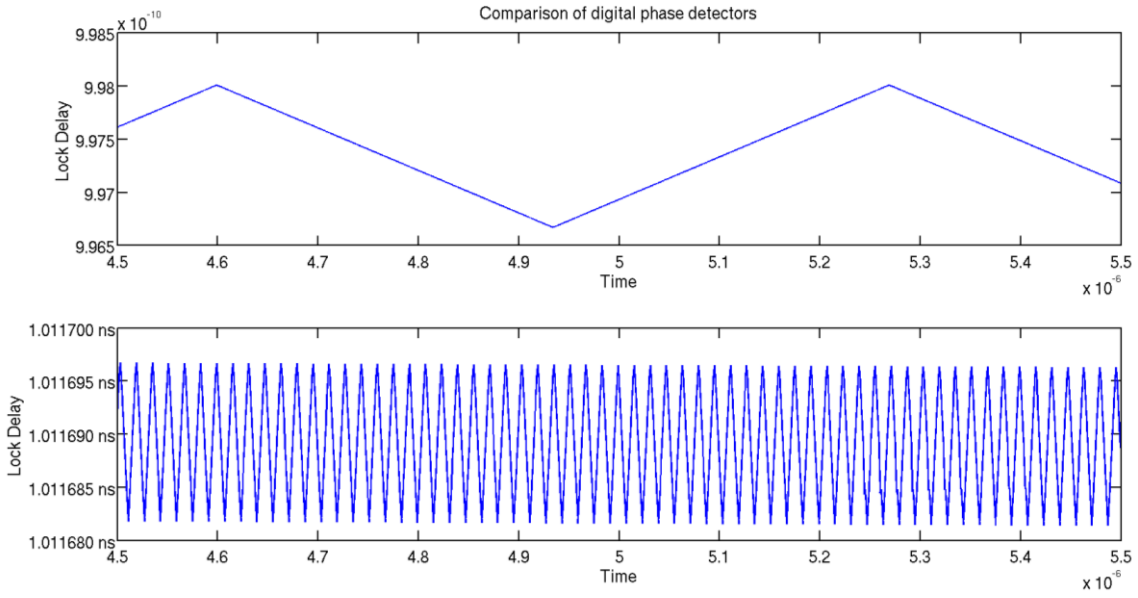

Figure 6: Comparison of two digital phase detectors

The second feature, the low hysteresis of the early-late detector, addresses the problem of the sticky output of the phase detector (Figure 23), resulting in an unstable lock state [6]. This issue is solved by using a modified phase detector (figure 6) and placing a reset period before every phase detecting period. In this way, every phase detection starts from the same output state. A typical timing diagram of this phase detector is shown in Figure 5. By using this technique, the phase detection hysteresis is reduced but also the detection speed is divided by 2. This, however, results in a more stable lock state of the DLL, resulting in a decreased output jitter. As shown in Figure 66, simulations show that the benefits of having a lower hysteresis, outweigh the lower phase detection speed. The upper graph shows the variation of the in-lock delay when using a pin load matched phase detector, which is supposed to have a low hysteresis. The lower graph shows the delay when using the improver phase detector. Comparing the two, the used phase detector results in a delay variation which is 40 times smaller than when using the pin load matched phase detector.

b. The delay line

One of the goals of this TDC is the ability to make the TDC work in harsh environments. Therefore, it is important to foresee the ability to compensate for intrinsic process variability, while still aiming for a high resolution. The worst-case buffer delay in a 65 nm CMOS technology is around 50 ps. To realize an acceptable resolution every delay element is interpolated eight times, meeting the requirement of having 2^Nth output levels. The delay of the buffer itself can be adjusted by means of an analogue control voltage, which controls the current inside the (current-starved) delay-cell. Inside the DLL, the delay line is constantly adjusted to fit the period of the clock reference.

c. The charge pump

As mentioned before, the DLL uses two charge pumps with different output currents. The CP with a small current is used when the delayed signal is either *early* or *late*. This means that the DLL is almost in the lock state and only small adjustments are required. If the delayed signal is *very-early* or *very-late*, the CP with a larger current is switched on, resulting in larger adjustments to bring the DLL faster to its lock state [7].

3. Conclusion

Several circuit techniques to improve radiation tolerance, for both TID and SEUs have been demonstrated. Both improvements, the special phase detector with four levels and the bang-bang PD with low hysteresis, enable an extremely fast recovery time below 2 μs in combination with a small locked loop hysteresis of 400 fs.

The proposed TDC will be submitted for fabrication in May 2017. Therefore, the presented performance of the TDC is based on simulation results using parasitic extracted models. As soon as silicon is available, measurements will be compared to the simulated resolution and hysteresis. Concerning radiation robustness, TID as well as SEU tests will be performed to verify the stability over time and fast recovery of the DLL.

4. References

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