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Analysis of three-level converters with voltage balancing capability in bipolar DC distribution networks

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***Abstract*—The growing number of distributed energy resources, DC loads and energy storage systems drive the adoption of DC distribution networks. This paper in particular addresses three-wire bipolar DC distribution networks (b-DCDN), that provide two voltage levels to connect low- and high-power loads, while transferring twice the amount of power with less conduction losses as compared to the two-wire unipolar network configuration. To stabilize and control these two voltage levels, converters with voltage balancing capability are essential. Although dedicated voltage balancing converters that transfer power between both poles exist, this paper shows the extent to which certain three-level DC-DC converters can both interface DC devices such as battery energy storage systems and balance the pole-to-neutral voltages in the presence of unbalanced currents. More in particular, this paper identifies and analyzes the members of the non-isolated three-level converter family that feature a bipolar DC front-end in different unbalanced conditions, thereby explicitly deriving the operating area of these converters, based upon a decomposition in balanced and unbalanced components. Furthermore, the paper demonstrates the influence of the modulation scheme in unbalanced conditions on the current ripple and required inductance.**

I. Introduction

DC distribution networks (DCDN) have been proposed because they offer potential benefits over AC distribution networks (ACDN), specifically when considering an increasing number of distributed energy resources and loads that require DC along the power conversion chain [1]–[5]. The improved compatibility between DC devices and a DC power architecture may reduce and simplify the power conversion steps, thereby reducing the losses and increasing the device-level reliability. Apart from the improved compatibility, DCDN enable to transfer more power over the same conductor cross-section [3], [5] and comprise DC-DC point-of-load converters which are actively controllable contrary to diode rectifiers.

In the literature, a two-wire ($+$ and $-$) unipolar and a three-wire bipolar network configuration adopting an additional neutral wire (n), are typically distinguished [6]–[8]. Providing the same pole-to-neutral voltage, the bipolar DC distribution networks (b-DCDN) allow transferring more power with lower conduction losses. Furthermore, they provide two voltage levels, namely the pole-to-neutral voltage and the pole-to-pole voltage (twice the pole-to-neutral voltage), which allows connecting high- and low-power DC devices at a suited voltage level. b-DCDN can therefore be considered the counterpart of a three-phase AC distribution network (ACDN) as compared to a single-phase ACDN. Accordingly, it is possible to connect DC devices asymmetrically (either to the positive-neutral or negative-neutral conductor pair), which causes (1) voltage unbalance and (2) non-zero neutral conductor currents. To resolve the first issue, this paper addresses converters with voltage balancing capability (VB) to equalize the pole-to-neutral voltages. Besides, converters with current redistributing capability (CR) address the second issue [9].

In literature several converter topologies have been presented to solely balance the pole-to-neutral voltages [7], [10]–[12]. However, it may be desirable to incorporate the voltage balancing capability in DC-DC converters that are anyway present within b-DCDN, e.g. converters to interface energy storage systems. For instance, the step-down three-level converter (S-TLC) has been identified as a suitable topology capable of providing a balanced and regulated bipolar front-end [13]–[15].

The voltage balancing capability of the S-TLC opens perspectives to address the other members of the three-level DC-DC converter (TLC) family, which were originally proposed to halve the voltage stress of power semiconductor devices (PSD), to double the effective switching frequency and to reduce the size of the passive components [16]. This paper therefore analyzes the non-isolated three-level converter family comprising the step-down, full-bridge and half-bridge three-level converter topologies that feature a bipolar front-end. The analysis starts from a decomposition of the voltages and currents in balanced (B) and unbalanced (U) components [17] and the definition of two novel control inputs, named the balanced and unbalanced duty cycles. The result is a model that decouples the balanced and unbalanced dynamics of the three-level converter family. Because the balanced and unbalanced duty cycle depend on the original duty cycles, they are inherently limited depending on the converter topology. These limitations are analytically derived to anticipate which unbalance scenarios can be accommodated and need to be incorporated in the converter controller (e.g. integrator anti-windup).

The paper is structured as follows. The next section introduces the voltage unbalance issue and four possible unbalance scenarios that generally may occur at the terminals of a VB. Subsequently, the third section analyzes the TLC family in

unbalance conditions including the derivation of their operating area and the unifying converter model. The third section also proposes two possible modulation schemes and evaluates the influence of unbalance conditions on the inductor current ripple. The fourth section concludes this paper.

II. Voltage unbalance in bipolar DC distribution networks

A. Causes and consequences of voltage unbalance

Bipolar DC distribution networks (b-DCDN) apply a positive, neutral and negative conductor to transfer power between different nodes in the distribution network, as opposed to unipolar DC distribution networks that only require two active conductors. Therefore, b-DCDN provide two voltage levels at each node terminal, i.e. the pole-to-neutral voltage and the pole-to-pole voltage which equals twice the former one. Accordingly, devices that operate at higher voltage levels can be connected pole-to-pole, while low-power devices can be connected between the positive (or negative) pole and the neutral conductor, similar to three-phase and single-phase devices in AC distribution networks respectively.

Connecting devices asymmetrically between a pole and the neutral may cause intolerable voltage unbalance in the network as the neutral terminal voltage shifts, a problem that also exists in three-phase AC networks [18], [19]. As a result of voltage unbalance, network components may be overstressed triggering protection equipment that will shut down part of the network. Another potential consequence is that dc-dc converters in the network no longer function near nominal operating conditions with the highest conversion efficiencies. Therefore, it is important to reduce voltage unbalance.

To demonstrate the voltage unbalance issue more in depth, consider the simple bipolar network depicted in Fig. 1 which consists of two voltage sources representing power electronic converters that regulate the pole-to-neutral voltages and two current sources representing loads (positive currents) or generators (negative currents). The steady-state voltages at the load terminals are expressed as:

$$V_{pi} = V_p - RI_{pi} - R(I_{pi} - I_{ni}) \tag{1}$$
$$V_{ni} = V_n - RI_{ni} + R(I_{pi} - I_{ni}) \tag{2}$$

where V_{pi} and V_{ni} are the positive and negative pole voltage at the load terminals respectively, I_{pi} and I_{ni} represent the positive and negative pole current drawn by the load respectively and R is the line resistance, assumed equal for the different conductors.

Building on the approach in [17], voltages and currents can be decomposed in balanced (B) and unbalanced (U) components, which resembles the symmetrical component method in ACDN. As will be exemplified, the decomposition provides valuable insights by decoupling the unbalanced voltage from the balanced voltage. The B/U components are related to the positive and negative quantities as:

$$x_B \equiv \frac{x_p + x_n}{2} \tag{3}$$
$$x_U \equiv \frac{x_p - x_n}{2} \tag{4}$$

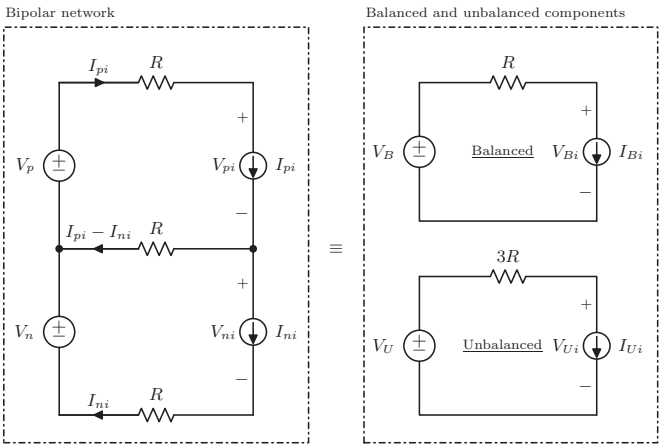


Fig. 1: Voltage unbalance example

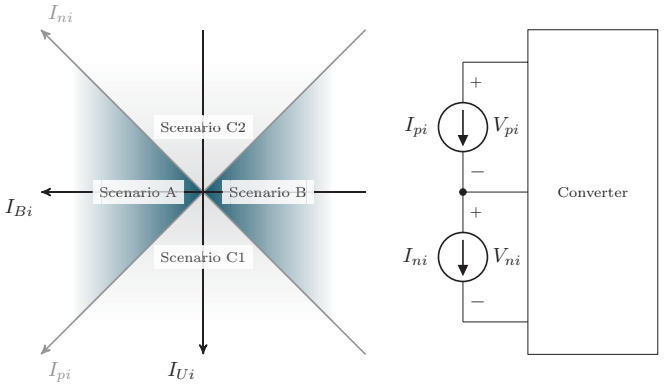


Fig. 2: Current unbalance scenarios

Applying the B/U decomposition to (1) and (2) results in following set of equations describing the network:

$$V_{Bi} \equiv \frac{V_{pi} + V_{ni}}{2} = V_B - RI_{Bi} \tag{5}$$
$$V_{Ui} \equiv \frac{V_{pi} - V_{ni}}{2} = V_U - 3RI_{Ui} \tag{6}$$

Where V_{Bi} and V_{Ui} are the balanced and unbalanced voltage at the load terminals respectively, and $I_{Bi} \equiv \frac{1}{2}(I_p + I_n)$ and $I_{Ui} \equiv \frac{1}{2}(I_p - I_n)$ represent the balanced and unbalanced current drawn by the load respectively. As can be observed from (5) and (6), the original bipolar network in Fig. 1 can be decomposed in a balanced and unbalanced network. In case the voltage sources are balanced ($V_p = V_n$), the unbalanced voltage V_U is zero and one can observe from (6) that $|RI_{1i}|$ should be zero to avoid voltage unbalance across the current sources with a balanced source ($V_p = V_n$). Note that voltage unbalance may also result from distributed generators or bidirectional energy storage systems in b-DCDN, causing negative I_{pi} and I_{ni} currents. Voltage unbalance thus stems from unbalanced currents (I_{Ui}) caused by the devices in the network and resulting resistive voltage drops (R) across the conductors.

Accordingly, four scenarios may occur, depending on the sign of I_{pi} and I_{ni}, as depicted in Fig. 2. Scenario A considers the case when unbalanced loads are connected to both poles, scenario B considers the case when unbalanced generation is connected to both poles, and scenario C1 and C2 consider a combination of unbalanced load and unbalanced generation. Note that scenario C1 and C2 may cause overcurrent in the neutral conductor, since I_{pi} and I_{ni} have opposite directions. Therefore it is concluded that scenario's C1 and C2 should be avoided or at least carefully considered when designing the architecture of a b-DCDN.

B. Solutions to reduce voltage unbalance

As the basic analysis has shown, voltage unbalance is in essence caused by current unbalance that leads to different voltage drops across the positive, neutral and negative conductor. A priori, unbalance currents should be avoided by connecting pole-to-neutral devices alternately positive-to-neutral and neutral-to-negative, possibly in an automated manner applying static load transfer switches [20]. However, voltage balancers (VB) should still govern the voltage balance in b-DCDN. In this work, a *voltage balancer* is defined as *a power electronic converter connected to a b-DCDN that is, amongst other optional functionalities, able to regulate the positive pole-to-neutral voltage equal to the negative pole-to-neutral voltage at the point of common-coupling with the network*. It will therefore withdraw or inject different currents in the positive and negative pole in order to equalize the pole-to-neutral voltages. Also note that each b-DCDN requires at least one VB to define the neutral point voltage.

The most basic VB in its kind is a resistive voltage divider, but it encounters intolerable quiescent power losses. Other converters with voltage balancing capability have been analyzed in [7], [11].

Other applications, like inverters with series-connected DC bus capacitors [21]–[23] and battery management systems [10], [24], [25], encounter similar unbalance issues due to leakage currents. However, since the leakage currents are orders of magnitude smaller than the unbalance currents encountered in b-DCDN, the proposed solutions are designed for low currents and consequently not applicable in b-DCDN.

The authors would like to point out that *current redistributors* (CR) have been proposed for b-DCDN [26], which are defined in this work as *power electronic converters connected to a b-DCDN that are, amongst other optional functionalities, able to transfer current from the positive to the negative pole and vice versa in order to reduce current in the neutral conductor*. Although both a VB and a CR will reduce voltage unbalance in b-DCDN, they serve a different purpose: the VB aims at directly regulating the unbalanced voltage V_U to zero, while the CR aims at regulating the unbalance current I_U to zero. They thus have different control objectives, but either directly or indirectly will have an influence on the voltage profile in the network. This paper focuses on the voltage balancing capabilities of the three-level converter family as will be elaborated in the next section.

III. Three-level converters in unbalance conditions

This section will analyze and discuss three members of the non-isolated three-level converter (TLC) family that possess two series-connected capacitors at the input and hence are able to connect to b-DCDN. These include the step-down TLC (S-TLC), the full-bridge TLC (FB-TLC) and the half-bridge TLC (HB-TLC) as depicted in Fig. 3. Although it features a bipolar front-end, the flyback three-level converter is not considered because it generally is used in the $0-500\,\mathrm{W}$ range [27] which is considered out of the scope of the present work. Each topology is analyzed in a similar manner: first the converter operation is introduced and key features are highlighted, subsequently the model equations are developed and finally the feasible operating area is determined.

A. Step-down three-level converter (S-TLC)

The S-TLC, depicted in Fig. 3a, contains two series-connected capacitors at the DC front-end, 4 power semiconductor devices (PSDs) with anti-parallel diodes and an inductor that enables regulating the current drawn from the DC back-end (the subsequent analysis presumes that $v_2 \geq 0$). As Fig. 3a shows, the four PSDs are stacked and the 2 pairs (d_p, d_p') and (d_n, d_n') are switched in a complementary manner. Hence two control inputs are available d_p and d_n that can be independently controlled using pulse-width modulation. When the output currents are balanced ($I_p = I_n$), the corresponding duty cycles d_p and d_n are equal. In unbalanced conditions however, the S-TLC is able to vary the amount of charge drawn from the positive and negative capacitors respectively by varying d_p and d_n and hence balance the pole-to-neutral voltages at the DC front-end.

Following averaged model governs the dynamics of the S-TLC:

$$L\frac{di_L}{dt} = d_p v_p + d_n v_n - v_2 \tag{7}$$

$$C\frac{dv_p}{dt} = -i_p - d_p i_L \tag{8}$$

$$C\frac{dv_n}{dt} = -i_n - d_n i_L \tag{9}$$

where i_L represents the inductor current, L is the inductance, v_p is the positive pole-to-neutral voltage, v_n is the neutral to negative pole voltage, v_2 is the back-end voltage and C is the pole-to-neutral capacitance.

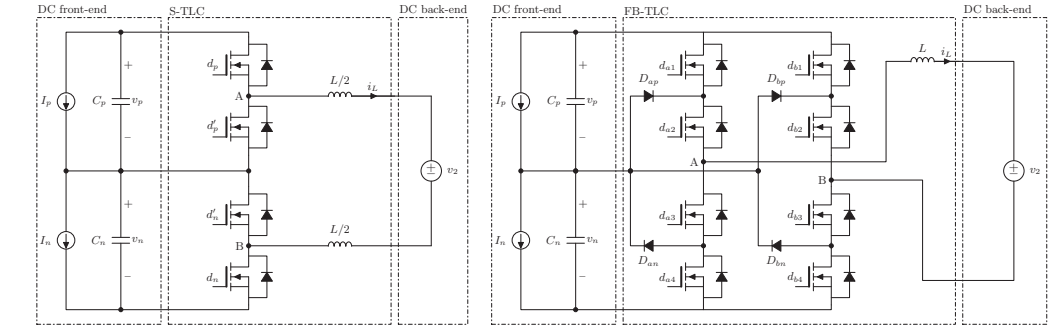
The averaged model can subsequently be decomposed in balanced and unbalanced components applying (3)-(4), resulting in:

$$L\frac{di_L}{dt} = 2d_B v_B + 2d_U v_U - v_2 \tag{10}$$

$$C\frac{dv_B}{dt} = -i_B - d_B i_L \tag{11}$$

$$C\frac{dv_U}{dt} = -i_U - d_U i_L \tag{12}$$

where v_B is the balanced voltage and v_U is the unbalanced voltage. $d_B = \frac{d_p+d_n}{2}$ and $d_U = \frac{d_p-d_n}{2}$ are two novel control inputs, referred to as the balanced and unbalanced duty cycle. The balanced duty cycle d_B governs i_L, while the unbalanced



(a) S-TLC (b) FB-TLC

(c) HB-TLC (neutral variant) (d) HB-TLC (positive variant) (e) HB-TLC (negative variant)

Fig. 3: Three-level converter topologies for b-DCDN

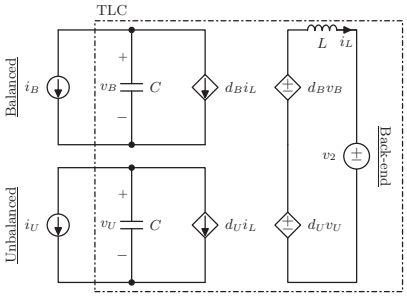


Fig. 4: Equivalent circuit of three-level converters

duty cycle d_U controls the unbalanced voltage v_U. Adding an additional outer-loop voltage controller that alters the current setpoint enables regulating the balanced voltage v_B. These model equations effectively decompose the converter model in a balanced and unbalanced operating mode, resulting in the equivalent averaged circuit depicted in Fig. 4.

The steady-state of the converter (steady-state variables are capitalised) in balanced conditions ($V_U = 0$) is described by:

$$D_B = \frac{V_2}{2V_B} \tag{13}$$

$$I_L = \frac{-I_B}{D_B} \tag{14}$$

$$D_U = \frac{-I_U}{I_L} \tag{15}$$

Equation (13) states that the balanced duty cycle D_B solely depends on the voltage ratio V_2/V_B and (15) relates the unbalanced duty cycle D_U to the unbalance current I_U and the inductor current I_L. The result is a relatively fixed balanced duty cycle D_B and an unbalanced duty cycle D_U that varies with the unbalance current I_U.

Because the duty cycles d_p and d_n should remain in the $[0;1]$ range, the S-TLC faces theoretical operating limits, given by (16)-(17) and expressed in B/U components in (18)-(19).

$$d_p = d_B + d_U \in [0;1] \tag{16}$$

$$d_n = d_B - d_U \in [0;1] \tag{17}$$

$$d_B \in [0;1] \tag{18}$$

$$|d_U| \leq \begin{cases} d_B & d_B \leq 0.5 \\ 1 - d_B & d_B > 0.5 \end{cases} \tag{19}$$

Fig. 5a graphically depicts the operating area of the S-TLC. Accordingly, in steady-state, the amount of unbalance current I_U in (15) is limited between $[-D_B I_L; D_B I_L]$ in case $D_B \in [0; 0.5]$ and $[-(1-D_B)I_L; (1-D_B)I_L]$ in case $D_B \in [0.5; 1]$. It can thus be concluded that the operating area of the S-TLC is theoretically limited and the amount of unbalance current I_U that can be supplied depends on the voltage ratio (related to D_B) and the inductor current I_L. The conclusion can also be physically interpreted as the inductor current I_L determines how much charge can be transferred from the positive and negative pole to the DC back-end during $D_p T_s$ and $D_n T_s$ (T_s is the switching period). Hence, the lower

TABLE I: Feasible switch configurations of the FB-TLC

Configuration	d_{a1}	d_{a4}	d_{b1}	d_{b4}	v_L
0	0	0	0	0	$-v_2$ (freewheeling)
1	1	0	0	0	$v_p - v_2$
2	0	0	1	0	$-v_p - v_2$
3	0	0	0	1	$v_n - v_2$
4	0	1	0	0	$-v_n - v_2$
5	1	0	0	1	$v_p + v_n - v_2$
6	0	1	1	0	$-v_p - v_n - v_2$

I_L, the lower the amount of charge that can be transferred in the respective ON time periods. Furthermore, operating closer to $D_B = 0.5$ enables a wider range of D_U values that can be attained. Finally, the operating limits of d_B and d_U can be conveniently be implemented in the converter controller, as opposed to limiting d_p and d_n.

Reconsidering the unbalance scenarios introduced in the previous section, the S-TLC can operate in scenarios A and B, but not in scenarios C1 and C2. Scenarios C1 and C2 require that the converter would be able to transfer power generated in one pole to the other pole during one switching cycle, which is impossible with the S-TLC. As explained in the previous paragraph, the amount of unbalance current I_U that can be compensated in scenarios A and B is theoretically limited.

B. Full-bridge three-level converter (FB-TLC)

The FB-TLC, depicted in Fig. 3b, contains two neutral point clamped legs (labeled A and B) each made up of four series-connected PSDs, including antiparallel diodes, an inductor L at the DC back-end and two series-connected capacitors that make up the DC front-end. Switches d_{a1} and d_{a3} of the A leg are switched in a complementary manner, as well as d_{a4} and d_{a2} [28]. d_{a1} and d_{a4} should never be on simultaneously, as it leaves the corresponding terminal voltage (terminal A) undefined. The same rules apply for the B leg.

Converter legs A and B enable to connect each terminal of the DC back-end to the positive, negative or neutral terminal of the DC front-end, which results in the 7 feasible switch configurations listed in Table I. Accordingly, 7 voltage levels (v_L) can be applied across the inductor L, including $-v_p - v_2$ and $-v_n - v_2$, which distinguishes the FB-TLC from the S-TLC. These switch configurations enable to transfer energy from one pole to the other within a single switching cycle. The ability to charge the inductor from one pole and discharge to the other pole implies that the FB-TLC can operate in scenario C1 and C2, which is a distinguishing feature of this topology.

By defining $d_p = d_{a1} - d_{b1}$ and $d_n = d_{b4} - d_{a4}$, the averaged converter model of the FB-TLC can also be described by the model and equivalent circuit derived for the S-TLC in (7)-(9) and Fig. 4. Decomposing the FB-TLC model in B/U components also leads to (10)-(12) and (13)-(15) in balanced steady-state conditions.

The difference with the S-TLC exists in the values that d_p and d_n can attain: $\{-1, 0, 1\}$, instead of $\{0, 1\}$. This is accomplished as follows: when $d_p > 0$, $d_{a1} = |d_p|$ and $d_{b1} = 0$ and vice versa when $d_p < 0$. The same rules apply for d_n: when $d_n > 0$, $d_{b4} = |d_n|$ and $d_{a4} = 0$ and vice versa when $d_n < 0$. Following the same definition of d_B and d_U, the model is transformed to balanced and unbalanced components.

TABLE II: HB-TLC model equations and limits

Variant	d_p	d_n	Limits
Neutral	d_{a1}	$-d_{a4}$	$d_p \in [0;1]$, $d_n \in [-1;0]$, $d_U \leq 0.5$
Positive	$d_{a1} - 1$	$-d_{a4}$	$d_p \in [-1;0]$, $d_n \in [-1;0]$, $d_U \leq 0$
Negative	d_{a1}	$1 - d_{a4}$	$d_p \in [0;1]$, $d_n \in [0;1]$, $d_U \leq 0$

The operating area of the FB-TLC is limited by the feasible values that the duty cycles d_p and d_n can attain, resulting in two operating limits:

1) As explained, the DC back-end can be connected to the neutral, positive or negative pole by leg A or B respectively and consequently d_p and d_n are limited between $[-1; 1]$.
2) The switches d_{a1} and d_{a4} cannot be in the on-state simultaneously, therefore $d_{a1} < 1 - d_{a4}$ and the same applies for switches d_{b1} and d_{b4}. Otherwise, the corresponding inductor terminal voltage would be undefined. That limitation constrains d_U, as expressed in (20) and (21).

$$\underbrace{d_{a1}}_{d_p} \leq 1 - \underbrace{d_{a4}}_{-d_n} \Rightarrow d_p \leq 1 + d_n \Rightarrow d_U \leq \frac{1}{2} \tag{20}$$

$$\underbrace{d_{b1}}_{-d_p} \leq 1 - \underbrace{d_{b4}}_{d_n} \Rightarrow -d_p \leq 1 - d_n \Rightarrow d_U \geq \frac{-1}{2} \tag{21}$$

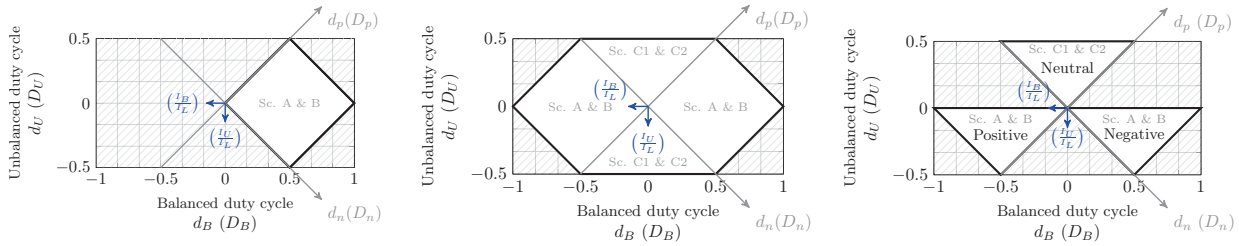
The resulting operating area that is theoretically achievable is depicted in Fig. 5b. The FB-TLC covers a wider operating area as compared to the S-TLC. The additional area that is covered relates to operating scenario C1 and C2 where power is transferred between both poles. And furthermore, the FB-TLC allows for negative V_2/V_B voltage ratios. If $|d_B| < 0.5$, d_U can vary between $[-0.5; 0.5]$ instead of $[-d_B, d_B]$ as with the S-TLC. In case $D_B > 0.5$, the operating area of the FB-TLC and S-TLC coincide.

C. Half-bridge three-level converter (HB-TLC)

The HB-TLC, depicted in Fig. 3c-3e, consists of one neutral-clamped leg, an inductor L at the DC back-end and two series-connected capacitors that make up the DC front-end, similar to the converter topologies discussed previously. Three variants exist as the inductor can be connected between the output terminal of the half-bridge and either the neutral point, positive pole or negative pole. Similar to the FB-TLC, (d_{a1},d_{a3}) and (d_{a4},d_{a2}) are complimentary switch pairs.

By defining d_p and d_n as included in Table II, the models of the three HB-TLC variants resemble the model and equivalent circuit of the TLC topologies discussed before. The model can in turn be transformed to balanced and unbalanced variables.

As d_p and d_n are defined differently, each HB-TLC variant covers a specific part of the operating area as depicted in Fig. 5c and included in Table II. As $d_{a1} \in [0; 1]$ and $d_{a4} \in$



(a) S-TLC (b) FB-TLC (c) HB-TLC

Fig. 5: Operating area of the S-TLC, FB-TLC and HB-TLC. The white regions represent the operating area. The operating area is valid during transients and in steady-state (steady-state quantities are capitalised and within brackets).

$[0;1]$, d_p and d_n are limited. Furthermore, d_{a1} and d_{a4} should never be on simultaneously (they may be off simultaneously), implying that $d_u < 0$ for the positive and negative variant and $d_u < 0.5$ for the neutral variant.

As Fig. 5c shows, the neutral variant can only operate at zero unbalance current $I_U = 0$ in case $D_B = 0$, which implies $V_2 = 0$. In that case, the neutral variant is the three-level version of the two-level half-bridge voltage balancer. Depending on the direction of I_L, positive and negative unbalance currents I_U can be supplied. On the contrary, the positive can operate at $V_2 < 0$ and negative variant at $V_2 > 0$.

D. Modulation and inductance selection

The filter inductor L is an essential design parameter of the TLC topologies discussed previously, as it determines the current ripple ΔI that is generally a design constraint. The adopted pulse-width modulation scheme that determines the relative phase of d_p versus d_n also influences the current ripple. Two modulation schemes are considered in this analysis. The first modulation scheme is generally proposed for three-level converters [16], while the second modulation scheme is proposed here as an alternative. In modulation scheme 1, as shown in Fig. 6a, the switching signals referred to by the duty cycles d_p and d_n, start at the beginning and at half of the switching cycle. In case d_n exceeds 0.5, the corresponding switching signal extends into the beginning of each switching cycle. An alternative modulation scheme 2 is depicted in Fig. 6b, where d_p and d_n are applied at the beginning and the end of the switching cycle.

As the TLC topologies all obey the same model by defining d_p and d_n, the expressions for the current ripple do match. The normalized current ripple in steady-state $\Delta I_n = \left(V_B^{-1} L f_s\right) \Delta I$ is expressed by (22) and (23) and depicted in Fig. 6 as a function of the balanced and unbalanced duty cycle D_B and D_U in case the unbalanced voltage is regulated to zero ($V_U = 0$).

$$\Delta I_n = \begin{cases} (|D_B| + |D_U|)\,|(1 - 2|D_B|) & |D_B| \in [0; 0.25] \\ (0.5 - |D_B| + |D_U|)\,(-2|D_B|) & |D_B| \in [0.25; 0.5] \wedge |D_U| \leq 0.25 \\ (1 - |D_B| - |D_U|)\,(-2|D_B|) & |D_B| \in [0.25; 0.5] \wedge |D_U| > 0.25 \\ (|D_B| + |D_U| - 0.5)\,(2 - 2|D_B|) & |D_B| \in [0.5; 0.75] \wedge |D_U| \leq 0.25 \\ (|D_B| - |D_U|)\,(2 - 2|D_B|) & |D_B| \in [0.5; 0.75] \wedge |D_U| > 0.25 \\ (1 - |D_B| + |D_U|)\,(1 - 2|D_B|) & |D_B| \in [0.75; 1] \end{cases} \tag{22}$$

$$\Delta I_n = \begin{cases} (|D_B| + |D_U|)(1 - 2|D_B|) & |D_B| \leq 0.5 \wedge |D_B| - |D_U| \leq 0 \\ (1 - 2|D_B|)(2|D_B|) & |D_B| \leq 0.5 \wedge |D_B| - |D_U| > 0 \\ (2|D_B| - 1)(2 - 2|D_B|) & |D_B| > 0.5 \end{cases} \tag{23}$$

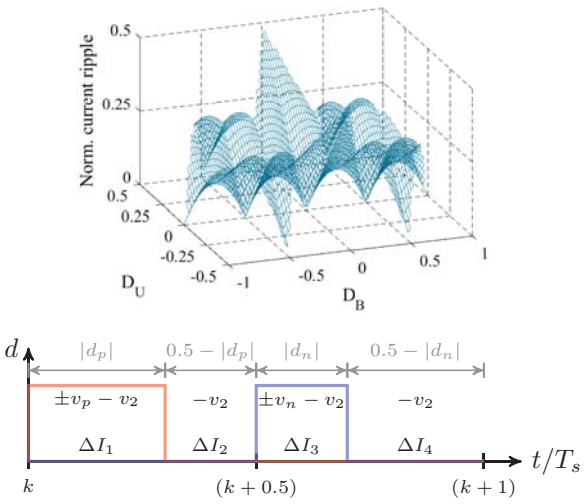
These expressions are valid for all TLC topologies in their respective feasible operating area. As the previous analysis has proven, D_B is related to the input-output voltage ratio and D_U to the level of unbalance current I_U, and hence Fig. 6 shows that the current ripple is different in unbalance conditions in case $I_U \neq 0$. Also note that the normalized current ripple in the absence of unbalance current ($D_U = 0$) matches with the results presented in [16].

Fig. 6 shows that both modulation schemes result into comparable current ripple values. However, as depicted in Fig. 7, modulation 1 outperforms modulation 2 in certain regions of the operating area and vice versa. The figure also indicates regions where modulation 1 is not applicable, corresponding to the operating area of the FB-TLC and the HB-TLC (neutral variant). Modulation scheme 1 is not applicable in those particular regions because the switching signals d_{a1} and d_{a4} should never overlap, as described in the analysis of the respective topologies. Consider for example the case $D_B = 0.25$ and $D_U = 0.3$, located in that particular region. That translates into $d_p = d_{a1} = 0.55$ and $d_n = -d_{a4} = -0.05$ and as $d_p > 0.5$, both switching signals will overlap, which is not allowed. On the contrary, modulation 2 is applicable as d_p and d_n do not overlap.

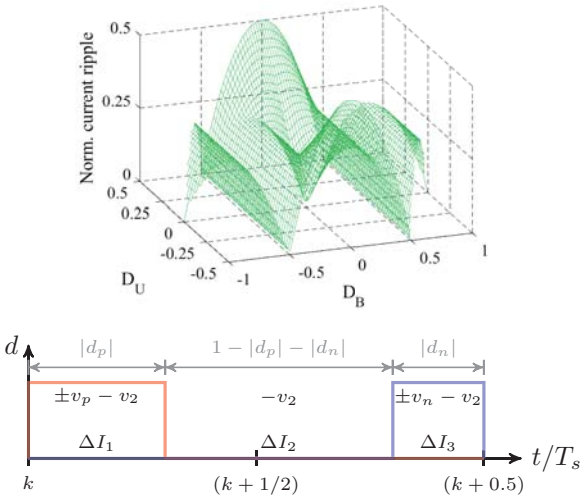
Finally, Fig. 6 shows that the highest normalized current ripple ($\Delta I_n = 0.5$) for both modulation schemes occurs in the region where D_p and D_n have opposite signs, i.e. the region of unbalance scenario C1 and C2. Hence, if those scenarios need to be handled by the FB-TLC or HB-TLC, it requires a significantly higher inductance as compared to the other unbalance scenarios. Outside that region, the highest ΔI_n equals 0.28125 and 0.25 for modulation scheme 1 and 2 respectively. The current ripple of modulation scheme 2 does not depend on D_U.

E. Discussion

The preceding analysis shows that the S-TLC, FB-TLC and the HB-TLC all feature a DC back-end voltage which is lower



(a) Modulation 1



(b) Modulation 2

Fig. 6: Modulation and normalized peak-peak current ripple (ΔI_n) ($\Delta I = \Delta I_n V_B (L f_s)^{-1}$)

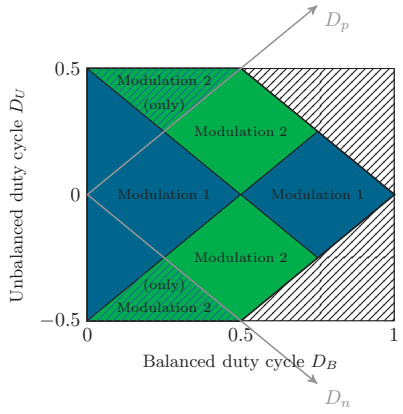


Fig. 7: Applicability of modulation scheme 1 and 2 in different parts of the operating area

than the pole-to-pole voltage and are capable at balancing the pole-to-neutral voltages in case the inductor current is non-zero. The analysis resulted in the averaged converter model (10)-(12), governing the dynamics of all three-level converters that are considered. Alternatively, the model equations can be represented by the equivalent circuit in Fig. 4, which applies to all TLC topologies and clearly demonstrates the decoupling between the balanced and unbalanced network. As the same equivalent circuit applies, the same controller can be adopted for the different three-level topologies.

Nonetheless, the converter topologies fundamentally differ in terms of the applicable limits of the balanced (d_B) and unbalanced (d_U) duty cycles, resulting in a specific operating area for each topology as depicted in Fig. 5. These operating limits should be incorporated in the controller, e.g. in anti-windup settings. The FB-TLC covers the largest operating area, followed by the S-TLC and the HB-TLC. The FB-TLC is capable of transferring current between both poles in a single switching cycle and therefore may operate in scenario C1 or C2, at the expense of a high part count as compared to the other two. In case $V_2 > V_B$, the operating area of the FB-TLC and S-TLC coincide. The FB-TLC is expected to encounter higher power losses as compared to the S-TLC and HB-TLC, because of higher conduction losses occurring in the PSDs. The smallest operating area is covered by the HB-TLC and as it requires additional clamping diodes as compared to the S-TLC, it is considered less advantageous.

IV. Conclusion

The analysis conducted in this paper showed that the S-TLC, FB-TLC and HB-TLC are able to interface DC devices such as energy storage systems with b-DCDN and simultaneously provide voltage balancing capability.

The analysis demonstrated that not only voltages and currents can be effectively decoupled to study the unbalanced and balanced operating mode of the three-level converters, but also the duty cycles. The analysis resulted in a unifying model and equivalent averaged circuit that describes all considered three-level converter topologies. The model furthermore includes two novel control inputs, i.e. the balanced and unbalanced duty cycle, that are limited and specific for each three-level converter topology. Consequently, the voltage balancing capability and operating area of each topology is limited and different. The FB-TLC covers the largest operating area at the expense of additional power semiconductor devices, while the S-TLC shows to be a good compromise between operating area and part count. The three variants of the HB-TLC cover only a limited part of the operating area while requiring more parts than the S-TLC.

The paper showed that a higher inductance should be selected in certain unbalance conditions, as unbalanced operation increases the current ripple in certain parts of the operating area, depending on the adopted modulation scheme.

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REFERENCES

[1] K. Engelen, E. L. Shun, P. Vermeyen, I. Pardon, R. D'hulst, J. Driesen, and R. Belmans, "The feasibility of small-scale residential DC distribution systems," in *Proc. 32nd Annual Conference on IEEE Industrial Electronics (IECON)*, Nov. 2006, pp. 2618–2623.

[2] M. E. Baran and N. R. Mahajan, "DC distribution for industrial systems: opportunities and challenges," *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1596–1601, Nov. 2003.

[3] A. Agustoni, E. Borioli, M. Brenna, G. Simioli, E. Tironi, and G. Ubezio, "LV DC distribution network with distributed energy resources: Analysis of possible structures," in *Proc. 18th International Conference and Exhibition on Electricity Distribution (CIRED)*, Jun. 2005, 5 pages.

[4] J. J. Justo, F. Mwasilu, J. Lee, and J.-W. Jung, "AC-microgrids versus DC-microgrids with distributed energy resources: A review," *Renewable and Sustainable Energy Reviews*, vol. 24, pp. 387–405, Aug. 2013.

[5] D. K. Elektrotechnik, "Deutsche Normungs-Roadmap Gleichstrom im Niederspannungsbereich Version 1," Verband Der Elektrotechnik, Tech. Rep., 2016, 138 pages.

[6] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type DC microgrid for super high quality distribution," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066–3075, Dec. 2010.

[7] J. Lago, J. Moia, and M. L. Heldwein, "Evaluation of power converters to implement bipolar DC active distribution networks DC-DC converters," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2011, pp. 985–990.

[8] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids - part II: A review of power architectures, applications, and standardization issues," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[9] J. Lago and M. Heldwein, "Operation and control-oriented modeling of a power converter for current balancing and stability improvement of DC active distribution networks," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 877–885, Mar. 2011.

[10] A. V. Jouanne, S. D. S. Dai, and H. Z. H. Zhang, "A Simple Method for Balancing The DC-link Voltage of Three-Level Inverters," in *Proc. IEEE 32nd Annual Power Electronics Specialists Conference*, vol. 3. IEEE, 2001, pp. 1341–1345.

[11] H. Kakigano, Y. Miura, T. Ise, and R. Uchida, "DC Voltage Control of the DC Micro-grid for Super High Quality Distribution," in *Proc. Power Conversion Conference*, Nagoya, Japan, April 2007, pp. 518–525.

[12] J. Rekola and H. Tuusa, "Comparison of line and load converter topologies in a bipolar LVDC distribution," in *Proc. 14th European Conference on Power Electronics and Applications*, Aug. 2011, 10 pages.

[13] L. Tan, B. Wu, V. Yaramasu, S. Rivera, and X. Guo, "Effective Voltage Balance Control for Bipolar-DC-Bus-Fed EV Charging Station With Three-Level DCDC Fast Charger," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4031–4041, Jul. 2016.

[14] L. Tan, B. Wu, S. Rivera, and V. Yaramasu, "Comprehensive DC Power Balance Management in High-Power Three-Level DC-DC Converter for Electric Vehicle Fast Charging," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 89–100, Jan. 2016.

[15] C. Jiang, G. Zeng, X. Wu, and J. Yang, "Droop control of current-source converters in bipolar-type DC microgrid," in *Proc. IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, vol. 3. IEEE, Nov. 2015, 5 pages.

[16] X. Xinbo Ruan, B. Bin Li, Q. Qianhong Chen, S.-C. Siew-Chong Tan, and C. Tse, "Fundamental Considerations of Three-Level DCDC Converters: Topologies, Analyses, and Control," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.

[17] Y. Gu, W. Li, and X. He, "Analysis and control of bipolar LVDC grid with DC symmetrical component method," *IEEE Transactions on Power Systems*, vol. 31, no. 1, pp. 685–694, Jan. 2016.

[18] L. Sainz, J. Pedra, and J. Mesas, "Study of neutral conductor current in three-phase networks with single-phase converters," *IEEE Transactions on Power Delivery*, vol. 21, no. 3, pp. 1466–1476, Jul. 2006.

[19] L. Degroote, B. Renders, B. Meersman, and L. Vandevelde, "Neutral-point shifting and voltage unbalance due to single-phase DG units in low voltage distribution networks," in *Proc. IEEE Bucharest PowerTech*, Jun. 2009, 8 pages.

[20] G.-H. Gwon, C.-H. Kim, Y.-S. Oh, C.-H. Noh, T.-H. Jung, and J. Han, "Mitigation of voltage unbalance by using static load transfer switch in bipolar low voltage DC distribution system," *International Journal of Electrical Power & Energy Systems*, vol. 90, pp. 158–167, 2017.

[21] H. Ertl, T. Wiesinger, and J. Kolar, "Active voltage balancing of DC-link electrolytic capacitors," *IET Power Electronics*, vol. 1, no. 4, pp. 488–496, 2008.

[22] P. Grbovic, "Loss-Free Balancing Circuit for Series Connection of Electrolytic Capacitors Using an Auxiliary Switch-Mode Power Supply," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 221–231, Jan. 2009.

[23] M. Makoschitz, M. Hartmann, H. Ertl, and R. Fehringer, "DC voltage balancing of flying converter cell active rectifier," in *Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2014, pp. 4071–4078.

[24] D. O. Boillat and J. W. Kolar, "Integrated isolation and voltage balancing link of 3-phase 3-level pwm rectifier and inverter systems," in *Proc. International Power Electronics Conference (IPEC)*, Hiroshima, Japan, May 2014, pp. 1073–1080.

[25] M. Daowd, N. Omar, P. Van Den Bossche, and J. Van Mierlo, "Passive and active battery balancing comparison based on matlab simulation," in *Proc. IEEE Vehicle Power and Propulsion Conference*, Sep. 2011, 7 pages.

[26] J. Lago and M. L. Heldwein, "Operation and Control-Oriented Modeling of a Power Converter for Current Balancing and Stability Improvement of DC Active Distribution Networks," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 877–885, Mar. 2011.

[27] F. Forest, E. Laboure, T. A. Meynard, and J.-J. Huselstein, "Multicell Interleaved Flyback Using Intercell Transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1662–1671, Sep. 2007.

[28] F. Deng and Z. Chen, "Control of Improved Full-Bridge Three-Level DC/DC Converter for Wind Turbines in a DC Grid," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 314–324, Jan. 2013.