The Tunnel Field-Effect Transistor

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I. INTRODUCTION

The tunnel field-effect transistor (TFET) is a semiconductor device aimed at low-power logic applications that employs band-to-band tunneling (BTBT) as a carrier injection mechanism to obtain a subthermionic subthreshold swing (SS). In particular, it relies on the energetic filtering of the tail of the electron Fermi-Dirac distribution to go below the fundamental 60 mV/dec SS limit at room temperature of a metal-oxide-semiconductor FET (MOSFET). The goal is to combine a low leakage current with a low SS to allow the TFET to be more energy efficient than a MOSFET.

Research in TFET has been driven by the fundamental power issues encountered by MOSFET as device scaling continues along the path of Moore's law. This law, in its most common formulation today, states that the number of electronic components per chip resulting in a minimum component cost, doubles approximately every two years[1,2]. Also, the rise of mobile applications and the Internet of Things, which contain a plethora of always-on sensor nodes, has increased the demand for devices with low supply voltage (V_{DD}) and low-leakage operation[3,4]. The TFET aims to fulfill this demand by exploiting the quantum mechanical phenomenon of tunneling. Although it is a leakage mechanism for MOSFET in today's scaled architectures, tunneling enables the TFET to go beyond the inherent ON-current ($\mathrm{I_{ON}}$) - OFF-current ($\mathrm{I_{OFF}}$) trade-off that hampers the low-power performance of the MOSFET. Several challenges still remain, however, before TFET can be implemented as a low-power replacement for MOSFET.

Several excellent overview works exist which summarize the TFET state-of-the-art or go into more detail on specific TFET topics[5–8]. This article aims to give a broad overview of the TFET field, with a distinct focus on device physics and architecture options. For more details, the reader is invited to consult the references which are included in each section. The article is structured as follows. First, the power issue of the MOSFET, which the TFET seeks to solve, is outlined in Section II. Next, the basic operation of the TFET is explained in Section III, along with the two main types of tunneling in Section IV. This is followed by an overview of different approaches to model the TFET operation in Section V. The main performance challenges for TFET are then presented in Section VI. In Section VII, different material options for TFET are considered. The subsequent sections are devoted to various implementation options that are being researched to improve the TFET performance, such as dopant pockets (Section VIII), specific gate configurations (Section IX) and strain (Section X). Section XI discusses attention points upon using the TFET in a circuit. Finally, Section XII gives a brief update on experimental work in literature. Section XIII concludes the article and provides a future outlook.

II. MOSFET POWER ISSUE

The inherent trade-off between $\mathrm{I_{ON}}$ and $\mathrm{I_{OFF}}$ for decreasing V_{DD} lies at the heart of the power density issue of MOSFET-based logic. This can be understood by looking at the total dissipated power of a circuit of MOSFET-based logic gates, which consists of a static and a dynamic component[9]:

$$P_{\mathrm{tot}} = P_{\mathrm{static}} + P_{\mathrm{dynamic}} = N_{\mathrm{g}} I_{\mathrm{OFF}} V_{\mathrm{DD}} + \alpha C_{\mathrm{tot}} V_{\mathrm{DD}}^2 f \quad (1)$$

with $\mathrm{N_g}$ the amount of gates, α the fraction of active gates, $\mathrm{C_{tot}}$ the total load capacitance of all gates and f the switching frequency. Based on Eq. (1), a key element in the so-called Dennard scaling of MOSFET, proposed in 1974[10], is the reduction of V_{DD} as the physical transistor dimensions are decreased with every new generation in order to maintain a constant power density (note that although $\mathrm{C_{tot}}$ decreases, the V_{DD} reduction also results in an increase of f). The threshold voltage ($\mathrm{V_{th}}$) is decreased accordingly to maintain sufficient $\mathrm{I_{ON}}$, which is proportional to $(\mathrm{V_{DD}} - \mathrm{V_{th}})^x$. The Dennard scaling paradigm has enabled the continuation of Moore's law until the end of the 20th century. However, Dennard scaling eventually leads to an untenable increase in the static power component, as the OFF-state leakage is exponentially dependent on $\mathrm{V_{th}}$[5]:

$$I_{\mathrm{OFF}} \sim e^{\frac{-V_{\mathrm{th}}}{nkT/q}} \quad (2)$$

where kT/q is the thermal voltage with k the Boltzmann constant, T the temperature and q the elementary charge, and where n is the body factor, equal to $\left(1 + \frac{C_d}{C_{\mathrm{ox}}}\right)$ with C_d and $\mathrm{C_{ox}}$ respectively the depletion and oxide capacitance of a planar MOSFET. Around the year 2002, the path of Dennard scaling was therefore abandoned, with the scaling of V_{DD} slowing down

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with respect to the scaling of the physical transistor dimensions. As a result, power density has been increasing as more and more transistors are included on a chip, with each transistor consuming roughly the same power as the previous generation. Notably, a significant portion of this power is consumed in the OFF-state. The rising power density leads to issues with cooling and reliability.

The origin of the exponential dependence in Eq. (2) is the Fermi-Dirac distribution of the charge carriers in the source region. In the subthreshold regime, also called weak inversion, a potential energy barrier in the MOSFET channel region prevents low energy carriers in the source from flowing to the drain contact. However, the high energy carriers in the exponential tail of the distribution can still diffuse over the barrier in a process called thermionic emission. This leads to an exponential dependence of the drain-source current I_{DS} on the gate-source voltage V_{GS}[11]:

$$I_{\mathrm{DS}} \approx I_{D0} e^{\frac{V_{\mathrm{GS}}-V_{\mathrm{th}}}{nkT/q}} \quad \text{for } \mathrm{V_{GS}} < \mathrm{V_{th}} \tag{3}$$

with I_{D0} the current at $V_{GS} = V_{th}$.

The inverse of the slope of Eq. (3) determines the trade-off between I_{ON} and I_{OFF}. It is called the subthreshold swing (SS) and is used as a metric for the switching steepness of the device. SS is defined as the increase in V_{GS} that is required to increase I_{DS} with one order of magnitude[5,10], and can be expressed as:

$$SS = \frac{V_{\mathrm{GS}}}{\log_{10} \mathrm{I_{DS}}} \approx \left(1 + \frac{C_d}{C_{\mathrm{ox}}}\right) \frac{kT}{q} \ln(10). \tag{4}$$

At room temperature (T = 300 K), the SS of a MOSFET is therefore theoretically limited to about 60 mV/dec. In actual implementations, non-idealities result in SS values which can be significantly higher. Fig. 1 illustrates graphically that the value of the SS determines the intersection with the V_{GS} = 0 V axis, which corresponds to I_{OFF}. I_{OFF} increases exponentially as V_{th} is decreased and the curve shifts leftwards. As I_{OFF} becomes unacceptably high, it prevents further concurrent scaling of V_{DD} and V_{th} and hence leads to aforementioned power density issues in highly scaled technologies. The underlimit on the SS makes this a fundamental trade-off.

Several new transistor concepts have been proposed to break the I_{ON}-I_{OFF} trade-off by having a SS lower than the MOSFET limit. Examples include concepts which use negative capacitance[12], impact-ionization[13] and mechanical switches[14]. However, these concepts give rise to hysteretic behavior and typically require a high operating voltage (> 1 V) at one of the transistor contacts.

The TFET is a new transistor concept, compatible with CMOS technology, that has been proposed for being capable of having a SS lower than the MOSFET limit. This is possible because the TFET relies on quantum mechanical BTBT instead of thermionic emission as the carrier injection mechanism. The basic TFET structure was first proposed in 1978 as a 'surface channel tunnel junction', aimed at investigating subband splitting and many-body effects in quasi-2D systems[15]. However, it was not until 1987 that BTBT was suggested as the working principle of a transistor in a DRAM trench transistor cell[16]. Major research efforts started after 2004, when a carbon nanotube TFET was demonstrated with a sub-60 mV/dec SS at room temperature[17] and the use of heterostructures was conceptually introduced[18]. Since then, significant research efforts have been invested worldwide in improving the TFET performance by optimization of the device architecture and material system.

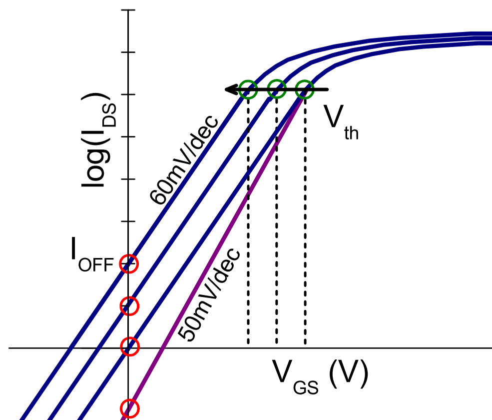

FIG. 1. Schematic transfer characteristics of a MOSFET with an ideal SS and a steep slope device with a sub-60 mV/dec SS, illustrating that the SS determines I_{OFF}. Scaling of the threshold voltage V_{th} increases the OFF-current I_{OFF} exponentially.

III. TFET BASICS

A. Basic structure and operating principle

The basic TFET structure is similar to that of a MOSFET: it contains two contact regions and an intrinsic or lowly doped channel region, covered by a gate dielectric and a gate contact (see Fig. 2(a)). In contrast to a MOSFET, however, the TFET contact regions have an opposite doping polarity, resulting in a p-i-n profile. In an nTFET, the p-type region acts as the source region, while in a pTFET, the n-type region acts as the source. Many variations on the basic configuration are possible, with different gate overlaps or doping profiles. These will be discussed in Sections VIII to X. First, the working principle will be explained for a basic p-i-n nTFET in a semiclassical picture. In this discussion, it is assumed that the doping is such that the Fermi-level in the source is aligned with the valence band edge.

The TFET operates by enabling and preventing BTBT between the source and the channel region by modulation of the electrostatic potential in these regions with

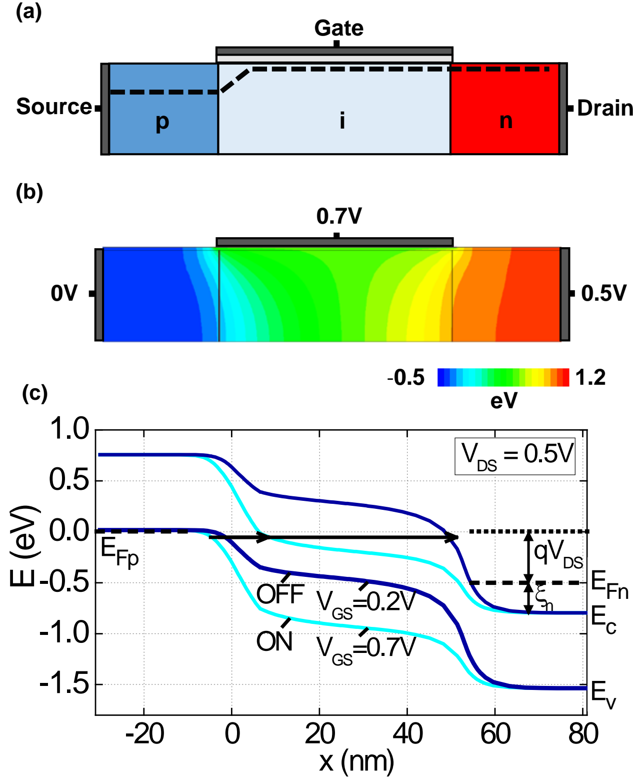

FIG. 2. (a) Basic p-i-n TFET configuration. (b) 2D electrostatic profile of a p-i-n $In_{0.53}Ga_{0.47}As$ TFET in the ON-state. (c) Energy band diagram along the cutline in (a) in the OFF (dark lines) and ON-state (light lines). The black arrows illustrate the shortening of the available tunnel paths. The quasi-Fermi level for the holes in the source (E_{Fp}) coincides with the valence band edge, while at the drain side, there is a degeneracy ξ_n.

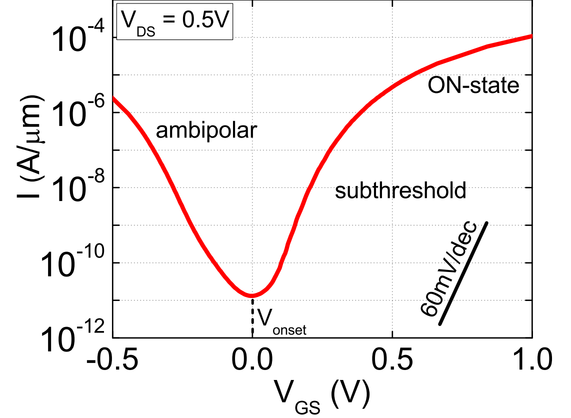

FIG. 3. Semiclassical (SC) simulated transfer characteristics of an $In_{0.53}Ga_{0.47}As$ p-i-n TFET as shown in Fig. 2(a). The TFET body thickness is 20 nm with a source doping of $5\text{x}10^{19}\text{cm}^{-3}$ and an EOT of 0.6 nm.

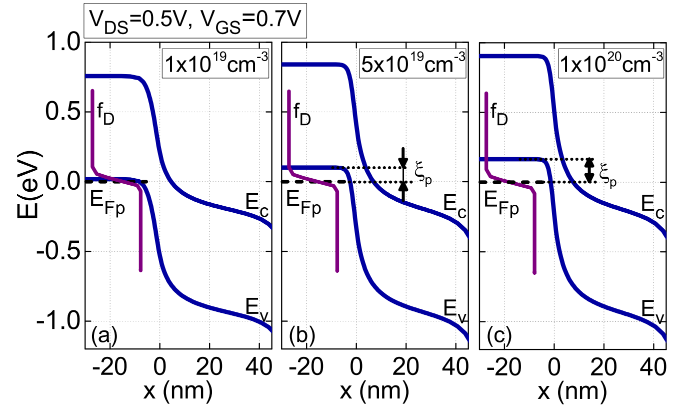

FIG. 4. Energy band diagram of the p-i-n $In_{0.53}Ga_{0.47}As$ TFET of Fig. 2 with different degrees of source doping degeneracy ξ_p, ranging from (a) no degeneracy to (b) medium degeneracy to (c) high source degeneracy. As the source degeneracy increases, less of the exponential tail of the Fermi-Dirac distribution f_D is filtered by the source bandgap. For the ease of extraction, a cross-section parallel to the gate has been used.

the gate contact (see Figs. 2(b) and (c)). The source and drain contacts are biased such that the p-i-n diode is in reverse bias. In the OFF-state, the only current that flows is the reverse leakage current of the p-i-n diode. This leakage current is typically caused by minority carrier diffusion currents and by defect-assisted processes, such as Shockley-Read-Hall (SRH) generation and trap-assisted-tunneling (TAT) (see Section VI C). As V_{GS} is increased, the source is depleted and the electric field at the tunnel junction rises. This corresponds to an increasing band bending at the source-channel junction. At a given V_{GS}, called the onset voltage (V_{onset}), the conduction band in the channel crosses over with the valence band in the source, such that tunneling transitions between these two bands become available. These transitions can be direct, between the maximum of the valence band and the minimum of the conduction band at the Γ-point, or indirect, between the maximum of the valence band and the minimum of one of the conduction band valleys. In the indirect case, the transition is assisted by a phonon. The tunneling transitions, whether direct or indirect, form the current generating process of the TFET.

B. Transfer characteristics

Fig. 3 plots an example of typical TFET transfer characteristics, I_{DS} as a function of V_{GS}, showing the different operating regimes. The tunneling current rises as V_{GS} is increased above V_{onset}, since the length of the available tunnel paths decreases and the electron tunneling probability is exponentially dependent on the tunneling distance. At V_{GS} equal to V_{DD}, the transistor is in the ON-state, and I_{DS} at this point is I_{ON}. The transition

from the OFF to the ON-state is, in analogy to the MOSFET, called the subthreshold swing (SS), although there is no fixed-swing subthreshold regime as in a MOSFET (see Section VI B), and hence also no V_{th}. The I-V curve in Fig. 3 shows a SS lower than the 60 mV/dec MOSFET limit.

The low SS of the TFET originates from the energetic filtering effect of BTBT carrier injection. Fig. 4(a) illustrates how the bandgap of the source material cuts off a significant part of the exponential tail of the Fermi-Dirac distribution. This band-pass filter action effectively cools the carrier distribution. The origin of the SS-limit in a MOSFET, which was discussed in Section II, is thus removed. The TFET is therefore able to obtain a SS lower than 60 mV/dec at room temperature. When the Fermi-level in the source is no longer aligned with the valence band in the case of a highly doped source, the SS can be degraded if the source degeneracy is too large. Figs. 4(b) and (c) show that a part of the exponential tail is then no longer filtered. If this part of the tail results in observable current, it deteriorates the SS. On the other hand, Figs. 4(b) and (c) also show that a higher source doping increases the electric field at the tunnel junction, which leads to a higher I_{ON}. This SS-I_{ON} trade-off, along with other parameters influencing SS, is discussed further in Section VI B.

The TFET is an ambipolar device, meaning that an nTFET operates as a pTFET when a negative V_{GS} is applied. In this case, the depletion occurs in the n-type drain region as the electric field rises at the channel-drain junction. After cross-over of the valence band in the channel with the conduction band in the drain, a hole tunneling current is injected into the channel and the current increases with decreasing V_{GS} (see Fig. 3). The ambipolar behavior can be both an advantage and a disadvantage, and will be further discussed in Section XI A.

C. Output characteristics

The source doping, drain doping and V_{DS} determine the energetic window available for tunneling (see Fig. 2(b)). V_{DS} fixes the hole quasi-Fermi level E_{Fp} in the source relative to the electron quasi-Fermi level in the drain E_{Fn}. The total tunneling window, the energetic distance between the valence band in the source and the conduction band in the drain, is then the sum of (E_{Fp}-E_{Fn}) and any doping degeneracies in source ξ_p and drain ξ_n (see Fig. 4). For a constant V_{GS} and starting at a V_{DS} of 0 V, an increase in V_{DS} enlarges the tunneling window and increases I_{DS} (see Fig. 5). The increase of I_{DS} with V_{DS} continues until the conduction band edge in the drain falls below the conduction band edge in the channel. Beyond this V_{DS}, called $V_{DS,SAT}$, I_{DS} saturates, since an increase in V_{DS} no longer has an impact on the tunneling window. Since the conduction band edge in the channel is determined by V_{GS}, $V_{DS,SAT}$ increases with increasing V_{GS}, just like in a MOSFET.

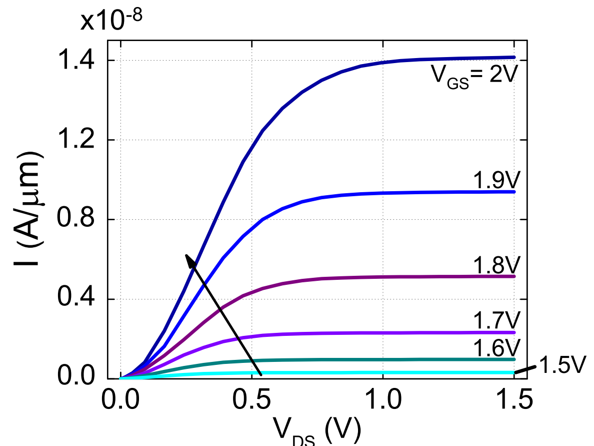

FIG. 5. SC simulated output characteristics of a Si p-i-n TFET as shown in Fig. 2(a) for varying V_{GS}. The TFET body thickness is 20 nm with a source doping of 5x10^{19}cm^{-3} and an EOT of 0.6 nm.

Fig. 5 also shows that in contrast to the MOSFET, the onset of the TFET output characteristics can be superlinear. This occurs when the BTBT is inefficient for small V_{DS}, e.g. as a result of a large tunnel path caused by a large effective oxide thickness (EOT), a low source doping or as a result of very low carrier density available for BTBT[19–21] (see also Section VI A). In the superlinear regime, the output current is small. This is unwanted, since it increases the settling time of a TFET inverter. Further circuit implications of this superlinear onset will be discussed in Section XI D.

IV. POINT VERSUS LINE TUNNELING

After introducing the basic operating principle in the previous section, a first major distinction in tunneling types can now be made. Based on the alignment of the electric field induced by the gate with the dominant tunnel paths, two types of tunneling can be defined in a TFET: point tunneling (Section IV A) and line tunneling (Section IV B), which can both be present in the same device (Section IV C).

A. Point tunneling

Point tunneling is the dominant type in a standard p-i-n/n-i-p TFET as depicted in Fig. 2(a) or Fig. 6(a), with the gate predominantly covering the channel. This configuration is also called a pointTFET. The term 'point tunneling' originates from the assumption that the tunnel paths curve around a central point at the interface between gate metal and gate dielectric, right above the tunnel junction. In this approximate semiclassical view, the tunnel paths are assumed to lie on circles formed

by the electric field lines between source and gate, starting at the tunnel junction and ending at the interface between gate-dielectric and channel[20]. Note that the circular form of the field lines is based on the assumption of infinitely high source doping. At onset, only the longest tunnel paths are available, which then gradually shorten as V_{GS} is increased toward the ON-state. In Fig. 2(a), these circular lines have been replaced with a straight line indicating the shortest allowed tunnel path, with roughly same start and end point as the circular lines.

The pointTFET performance is influenced by field-induced quantum confinement (FIQC), which is present in the triangular well formed by the conduction band edge in the channel and the dielectric barrier[22] (see Fig. 7, although for a lineTFET, the shape of the well is similar). In this well, subbands are formed. The onset of BTBT is thereby shifted to a higher V_{GS}, since the band edge determining the allowed tunnel path inside the well is defined by the first subband level, which is higher in energy than the bulk value of the band edge. As V_{GS} is increased and the triangular well deepens, the first subband level shifts down at a slower pace than the bulk band edge. Hence, the tunneling window increases more slowly than it would in the absence of FIQC. This has a stretching effect on the transfer characteristics, and hence negatively impacts SS. The degree of this confinement is determined by the effective mass of the band structure valley to which the tunneling transition is taking place and therefore depends on the material choice for the channel. The impact of FIQC can be alleviated with the introduction of a doping pocket at the source-channel interface, which forces the tunnel paths more parallel to the gate (see Section VIII A).

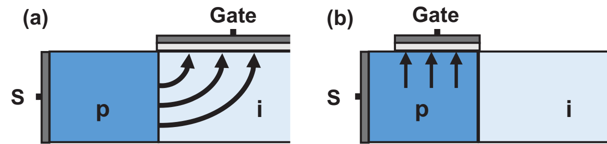

FIG. 6. Source-channel region of a (a) point tunneling and (b) line tunneling TFET configuration. The arrows schematically indicate the tunneling paths.

B. Line tunneling

Line tunneling can be induced with a large overlap of the gate over the source (see Fig. 6(b)). Such a configuration is also called a lineTFET. In contrast to point tunneling, the tunnel paths are equally long parallel straight lines perpendicular to the gate dielectric in the ideal case of no parasitic paths. For an increasing V_{GS}, the energy bands bend toward the gate dielectric until cross-over occurs between the conduction band edge at the gate dielectric and the valence band edge in the bulk, such that BTBT becomes possible (see Fig. 7). In the idealized case of a uniform field underneath the gate dielectric, implying that also the drain voltage impact on the source region is completely neglected, the onset is more abrupt than for point tunneling. All tunnel paths underneath the gate-source overlap become available at the same amount of band bending, after which they shorten uniformly for increasing V_{GS}. The tunneling is also located closer to the gate than in a pointTFET, while the electric field is in line with the tunnel paths. This means a smaller increase in V_{GS} is required to achieve a given amount of band bending. Additionally, in the ON-state, the band bending is stronger, resulting in shorter tunnel paths. Important to note is that I_{ON} is proportional to the gate-source overlap.

The lineTFET's performance is more heavily impacted by FIQC than the pointTFET, since the triangular well underneath the gate is more pronounced. The stretching effect due to the slower increase in the tunneling window, also seen in the pointTFET, can therefore have a negative impact on the SS. Additionally, due to the strong FIQC, several distinct subband energy ladders can appear in the well, since the degree of confinement depends on the effective masses of the different band structure valleys. E.g. in a Si nTFET, those conduction band valleys which have a heavy longitudinal effective mass in the direction of confinement, are shifted in energy less than those for which the lower transverse mass determines the confinement. This leads to two ladders of quantized energy levels, as shown in Fig. 7(b). As a consequence, the tunneling currents to the different valleys see a relative shift, which is visible in the transfer characteristics as a kink in the SS[23]. This relative shift also affects the pTFET, in which the light hole band is shifted more by the confinement than the heavy hole band. Tunneling between conduction band and heavy hole band is not as efficient as to the light hole band: because of symmetry reasons, there is no direct coupling, so any tunneling transition must be assisted by a phonon. In the absence of confinement, this inefficient tunneling current is masked by the higher light hole-conduction band current. In the presence of FIQC, however, the relative shift results in the heavy hole-conduction band current forming an undesired tail to the transfer characteristics[24].

C. Point and line tunneling combined

Point and line tunneling current components can be present together in the same configuration. This is certainly true if the gate overlaps both the source and the channel region, but can also be induced by the fringing field of the gate, even if no gate-channel overlap is present. Because the line tunneling is more impacted by FIQC, V_{onset} for the point tunneling component is lower, meaning the gradual onset of the point tunneling can degrade the abrupt line tunneling onset. On the other hand, however, a gate-channel overlap removes the potential barrier between the source and the ungated channel, which can impede carriers from flowing to the drain

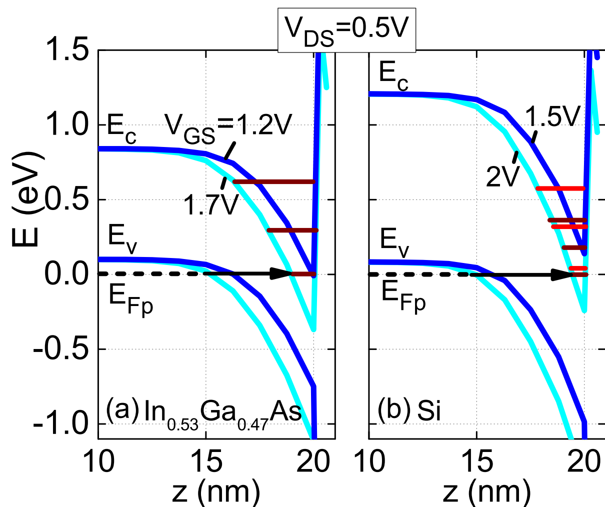

FIG. 7. Energy band diagrams of a lineTFET in the OFF (dark lines) and ON-state (light lines) along a vertical cutline through the center of the gate in the [100] crystal direction. (a) An $In_{0.53}Ga_{0.47}As$ configuration for a V_{GS} of 1.2 V and 1.7 V and (b) a Si configuration for a V_{GS} of 1.5 V and 2 V. Indicated schematically in brown and red are estimations of the first three quantized energy levels for the highest V_{GS}, corresponding to different valley effective masses inside the potential well. The dashed line represents the quasi Fermi level for the holes in the source (E_{Fp}).

and hence can decrease I_{ON}[25]. This introduces a trade-off between SS and I_{ON} and makes the alignment of the gate to the source-channel junction an important potential source for device variability in a lineTFET. However, the unwanted lateral tunneling component and the associated variability can be removed with the introduction of a counterdoped pocket, as discussed in Section VIII B.

V. MODELING

To acquire more physical insight into TFET operation and assess different architecture options, several models have been established. Since tunneling is a quantum mechanical phenomenon, all of these models rely on the solution of some form of the Schrödinger equation. Even so, the different solution approaches can be categorized as either semiclassical (Section V A) or fully quantum mechanical (Section V B). In semiclassical models, the Schrödinger equation is not solved directly. Rather, the tunneling probability is calculated based on the integral of a position dependent imaginary wave vector along a well-defined tunnel path. This implies the classical assumption that wave vector and position of the electron are known at the same time, violating the Heisenberg uncertainty principle. In fully quantum mechanical approaches, on the other hand, the electron is described entirely by its wave function, which is obtained from a solution of the Schrödinger equation projected on a chosen basis. Tunneling then arises as a consequence of the wave-like character of the electron. Here, the most common examples of both approaches are discussed, without being exhaustive.

A. Semiclassical

A common semiclassical approach to the solution of the time-independent Schrödinger equation is the Wentzel-Kramers-Brillouin (WKB) approximation. The reasoning behind WKB starts from the one-electron wave function ψ in zero electric field, which corresponds to a constant potential energy. Assuming the electric field to be zero in the tunneling direction x, and disregarding the other directions for now, ψ takes the form of a plane wave[26]:

$$\psi(x) = A\exp\left(\pm \mathrm{ik_x x}\right) \tag{5}$$

with i the imaginary number, x the tunneling direction, k_x the wave number and A the amplitude. The plus (minus) sign corresponds to a right (left) moving wave. The approximation then lies in assuming that the wave function in the presence of a small and smoothly varying non-zero field, can be described by introducing a position dependence for k_x. It can be shown that the phase $\phi(x)$ of the wave function can be obtained from the integral of $k_x(x)$ over the given domain[26]:

$$\psi(x) \equiv A(x)\exp(\mathrm{i}\phi(\mathrm{x})) \approx \frac{\mathrm{C}}{\sqrt{|\mathrm{k_x(x)}|}}\exp\left(\pm\mathrm{i}\int \mathrm{k_x(x)dx}\right) \tag{6}$$

with C a real constant. In a forbidden energy region, like the bandgap, k_x is imaginary ($k_x = i\kappa_x$), which results in an exponential decay of the wave function. This corresponds to a tunneling process. By comparing the probability density at each side of the tunneling barrier, an expression for the transmission probability can be derived. This expression typically ignores the prefactors of the exponentials and therefore solely consists of a contour integral of the imaginary k_x along the tunnel path through the forbidden region:

$$T_{\mathrm{WKB}} = \exp\left(2\int_{x_1}^{x_2} \kappa_x(x)dx\right) \tag{7}$$

with x_1 and x_2 respectively the start and end point of the tunnel path, also known as the classical turning points[26–28]. The tunnel path starts at the valence band edge and ends at the conduction band edge for a particular set of perpendicular wave numbers k_y and k_z. For zero perpendicular momentum ($k_y = k_z = 0$ and $\kappa_x = \kappa_{x0}$), the application of Eq. (7) is illustrated in Fig. 8. For non-zero k_y and k_z, the effective tunnel gap increases, making transmission less probable. This effect can be

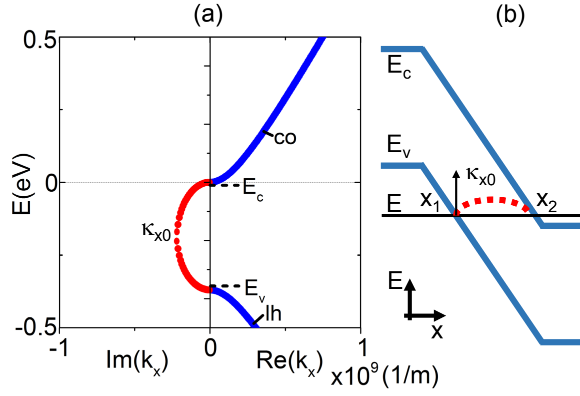

FIG. 8. (a) Real and imaginary 2-band $\mathbf{k}\cdot\mathbf{p}$ band structure of bulk InAs for zero perpendicular momentum ($k_y = k_z = 0$). Indicated are the conduction (co) and light hole (lh) bands. (b) Energy band diagram, superimposed with the imaginary band structure at a given energy E. The WKB transmission probability is calculated from an integral of this imaginary dispersion.

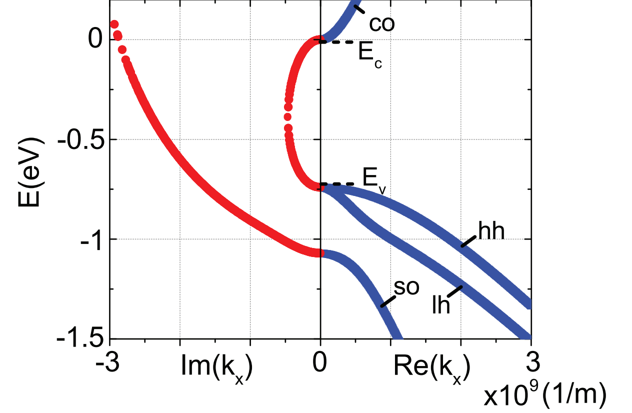

FIG. 9. Real and imaginary 30-band $\mathbf{k}\cdot\mathbf{p}$ band structure of bulk $In_{0.53}Ga_{0.47}As$. Indicated are the conduction (co), light hole (lh), heavy hole (hh) and split-off (so) bands.

made explicit by rewriting Eq. (7) as:

$$T_{\mathrm{WKB}}(k_y,k_z) = \exp\left(2\int_{x_1}^{x_2}\kappa_{x0}(x)dx\right) \times \exp\left(-|\mathrm{k_y^2}+\mathrm{k_z^2}|\int_{\mathrm{x_1}}^{\mathrm{x_2}}\frac{\mathrm{dx}}{\kappa_{\mathrm{x0}}(\mathrm{x})}\right) \quad (8)$$

where the assumption has been made that $k_y^2 + k_z^2 << k_{\mathrm{tot}}^2$ [28]. It is now clear that the second exponential factor of Eq. (8) reduces the transmission for non-zero perpendicular momentum[27,28]. In the case of direct BTBT, κ_{x0} can be extracted from the complex band structure of the material under study (see Fig. 8(a) and Fig. 9 for example band structures). Although the WKB method can describe quantum phenomena like tunneling, it is still a semiclassical approach, because Eq. (8) requires that both position and momentum (expressed by the wave vector) are known at the same time. This is possible in a classical approach, but violates the quantum mechanical Heisenberg uncertainty principle. From the WKB transmission probability in Eq. (7), the BTBT current can be calculated. This is discussed later in this section.

Another commonly used semiclassical model to calculate the transmission probability is Kane's model[29]. Originally, the Kane formula for BTBT probability was derived for a uniform electric field in a perturbative approach, using Fermi's golden rule and assuming a 2-band $\mathbf{k}\cdot\mathbf{p}$-model. An equivalent result can be obtained by starting from the WKB method and assuming the electric field F to be constant over the tunnel path length, while taking a two band $\mathbf{k}\cdot\mathbf{p}$ model to describe the complex wave vector dispersion. The transmission probability in a direct bandgap material can then be written as:

$$T_{\mathrm{Kane}}(k_y,k_z) = \exp\left(-\frac{\pi \mathrm{E_G^{3/2}m_R^{1/2}}}{2\mathrm{q}\hbar\mathrm{F}}\right)\exp\left(-2\frac{\mathrm{E}_\perp}{\overline{\mathrm{E}}}\right) \quad (9)$$

where $\mathrm{E_G}$ is the effective bandgap at the tunnel junction and m_R is the reduced effective mass, defined as $m_R = \frac{m_e m_{lh}}{m_e+m_{lh}}$, with m_e and m_{lh} the effective masses of respectively the conduction band and the light hole band. In the second exponential factor, $\mathrm{E}_\perp = \hbar^2(k_y^2+k_z^2)/(2m_R)$ and $\overline{\mathrm{E}} = 2q\hbar F/\left(\pi(m_R)^{1/2}E_G^{1/2}\right)$. A factor $\frac{\pi^2}{9}$, present in the original Kane derivation, was shown later to be incorrect and has been removed[30]. Because of the assumption of a constant electric field, the Kane model can deviate significantly from the WKB approach in cases where the field is strongly non-uniform[30,31].

From the transmission probabilities in Eq. (7) and Eq. (9), the BTBT current can be calculated in two ways. The first is based on the ballistic Landauer formalism and entails a direct integration of the transmission probabilities, weighted with the distribution functions in the contacts. This is called the Tsu-Esaki formula[32], which gives the BTBT current density as:

$$J_{DS} = \frac{2q}{h}\int_{k_x,k_y,k_z} T(k_y,k_z)(f_{\mathrm{S}}(E)-f_{\mathrm{D}}(E))\frac{dk_x}{2\pi}\frac{dk_y}{2\pi}\frac{dk_z}{2\pi} \quad (10)$$

where T is the transmission probability and $\mathrm{f_S}(E)$ and $\mathrm{f_D}(E)$ are the Fermi-Dirac distributions in the source and drain contacts respectively. The energy E is a function of k_x, k_y and k_z. Eq. (10) illustrates that the BTBT current is determined by both the transmission probability and the occupation probabilities at both sides of the tunnel junction.

A second way with stronger simplifications is to calculate the BTBT current is to determine a generation rate

per unit volume, which is then integrated over the full device volume. In this approach, device simulators search for tunnel paths which connect points of sufficient potential difference to allow for tunneling. Carriers are generated by the BTBT process at the endpoints of the tunnel paths. An expression for the generation rate can be derived from Eq. (10) by assuming the distribution functions for the carriers to be step functions, corresponding to a temperature of 0 K. This effectively decouples the carrier distribution functions from the transition rates. For the Kane model, the following generation rate formula is commonly used:

$$G_{\text{Kane}} = A\left(\frac{F}{F_0}\right)^D \exp\left(\frac{-\text{B}}{\text{F}}\right) \tag{11}$$

where F is the electric field, F_0 is 1 V/cm, D is a parameter that is taken 2 for direct bandgap materials and A and B are parameters defined as:

$$A_{\text{direct}} = \frac{g m_R^{1/2}(qF_0)^2}{\pi h^2 (E_G)^{1/2}} \tag{12}$$

$$B_{\text{direct}} = \frac{\pi^2 m_R^{1/2}(E_G)^{3/2}}{qh} \tag{13}$$

where g is a factor for the spin and valley degeneracies. Corrections that reintroduce the non-zero temperature distribution functions afterwards have been developed[33]. Extensions of Kane's model have been made to describe indirect phonon-assisted transitions as well[27]. For indirect BTBT, D in Eq. (11) is 2.5 and A and B are modified to[25]:

$$A_{\text{indirect}} = \frac{g(m_c m_v)^{3/2}(1+2N_{\text{PH}})D_{PH}^2(qF_0)^{5/2}}{2^{21/4}h^{5/2}m_R^{5/4}\rho\epsilon_{\text{PH}}E_G^{7/4}} \tag{14}$$

$$B_{\text{indirect}} = \frac{2^{7/2}\pi m_R^{1/2}E_G^{3/2}}{3qh} \tag{15}$$

where m_v (m_c) is the valence (conduction) band density of states effective mass, $\text{N}_{\text{PH}} = 1/\left[\exp(\epsilon_{\text{PH}}/\text{kT}) - 1\right]$, D_{PH} and ϵ_{PH} are respectively the occupation number, the deformation potential and the energy of the relevant phonons and ρ is the mass density. To obtain the BTBT current, the generation rate of Eq. (11) is integrated over the device volume:

$$I_{\text{DS}} = q\int G dV \tag{16}$$

with dV an elementary volume. The same approach can be followed for the WKB approximation[33].

The disadvantage of semiclassical methods is that they neglect certain quantum phenomena which result from the wave-like character of the electron, since they do not directly solve the Schrödinger equation in the full device region. Important examples for TFET include field or size-induced confinement effects, which can effectively increase the bandgap, and resonances and reflections in regions of high field, which respectively increase or decrease the transmission probability[34,35].

B. Quantum mechanical

A fully quantum mechanical simulation approach entails the solution of the Schrödinger equation in some form. In TFET modeling, the most commonly used is the time independent one-electron form:

$$\hat{H}\psi(\mathbf{r}) = \left[\frac{-\hbar^2}{2m_{\text{e}}}\nabla^2 + V_e(\mathbf{r}) + V_c(\mathbf{r})\right]\psi(\mathbf{r}) = E\psi(\mathbf{r}) \tag{17}$$

with m_e the free electron mass, E the total energy, $V_e(\mathbf{r})$ the external applied potential energy and $V_c(\mathbf{r})$ the crystal potential energy of the lattice. The solution of Eq. (17) generally occurs in two steps. First, the wave function is decomposed onto a reduced basis. This is because the complicated nature of $V_c(\mathbf{r})$ prevents the direct solution of Eq. (17) for ψ. The choice of basis corresponds to a particular band structure model. For TFET, the most commonly used models are the $\mathbf{k}\cdot\mathbf{p}$-based envelope function method and the orbital-based tight-binding method. Once the Hamiltonian has been written in the chosen basis, the second step is to construct a linear system or an eigenvalue problem, the solutions of which can be used to extract desired quantities like currents and carrier densities. The two main approaches for this step are the wave function method and the non-equilibrium Green's function (NEGF) method.

A first band structure model is the envelope function method, which expands the wave function on the solutions of the Schrödinger equation in bulk[36]:

$$\psi(\mathbf{r}) = \sum_n F_n(\mathbf{r})U_n(\mathbf{r}), \tag{18}$$

where the $U_n(\mathbf{r})$ form a complete set of orthonormal basis functions with the periodicity of the lattice and $F_n(\mathbf{r})$ are slowly varying envelope functions, which contain only Fourier components in the first Brillouin zone. The index n runs over all bands considered in the description. Inserting the expansion of Eq. (18) into Eq. (17) and using the properties of the set $U_n(\mathbf{r})$, namely orthonormality and completeness, the following system of equations results (a detailed derivation can be found in the work of Burt[36] and Van de Put *et al.*[34]):

$$\frac{-\hbar^2}{2m_{\text{e}}}\nabla^2 F_n(\mathbf{r}) - \frac{i\hbar}{m_{\text{e}}}\sum_m \mathbf{p}_{nm}\cdot\nabla F_m(\mathbf{r}) + \sum_m H_{nm}(\mathbf{r})F_m(\mathbf{r}) + V_e(\mathbf{r})F_n(\mathbf{r}) = EF_n(\mathbf{r}) \tag{19}$$

where the external potential V_e is assumed to vary slowly on the scale of a unit cell, like the envelope functions. The $\mathbf{p}_{nm}$ are known bulk $\mathbf{k}\cdot\mathbf{p}$ interband momentum matrix elements. They describe the coupling strength, and hence BTBT, between bands n and m. H_{nm} are the bulk Hamiltonian matrix elements, which correspond to known bulk band edge energies. The main advantage of Eq. (19), compared to Eq. (17) is therefore that the crystal potential $V_c(\mathbf{r})$ has been replaced with known material parameters.

An alternative band structure description, called the tight-binding method, consists of expanding the wave function on Bloch sums of localized atomic orbital-like functions, instead of on extended bulk solutions[37–39]:

$$\begin{aligned}\psi(\mathbf{r}) &= N^{-\frac{1}{2}} \sum_n C_n \sum_i \exp(\mathrm{i}\mathbf{k}\cdot\mathbf{R}_\mathrm{i})\phi_\mathrm{n}(\mathrm{r}-\mathbf{R}_\mathrm{i}) \\ &= N^{-\frac{1}{2}} \sum_{n,i} C_{n,i}\phi_n(r-\mathbf{R}_i)\end{aligned} \tag{20}$$

where ϕ_n is a Löwdin orbital with quantum number n, located on the atom at position $\mathbf{R}_i$. N is the number of primitive unit cells in the crystal and serves as a normalization constant. $C_{n,i} = C_n\exp(\mathrm{i}\mathbf{k}\cdot\mathbf{R}_\mathrm{i})$ are the expansion coefficients, which serve a similar purpose as the envelope functions F_n of Eq. (18). Inserting the expansion of Eq. (20) into the Schrödinger equation Eq. (17), multiplying from the left with the Bloch sum $\sum_j \exp(-\mathrm{i}\mathbf{k}\cdot\mathbf{R}_\mathrm{j})\phi^*_\mathrm{m}(\mathbf{r}-\mathbf{R}_\mathrm{j})$ and integrating over the full crystal, the following system of equations is obtained:

$$\sum_{\mathrm{i,j}} \mathrm{C_{n,i-j}} \int \phi^*_\mathrm{m}(\mathrm{r}-\mathbf{R}_\mathrm{j})\hat{\mathrm{H}}\phi_\mathrm{n}(\mathrm{r}-\mathbf{R}_\mathrm{i})\mathrm{d}\mathbf{r} = \sum_{\mathrm{i,j}} \mathrm{C_{n,i-j}E} \tag{21}$$

with $C_\mathrm{n,i-j} = C_\mathrm{n}\exp(\mathrm{i}\mathbf{k}\cdot(\mathbf{R}_\mathrm{j}-\mathbf{R}_\mathrm{i}))$. The integrals in Eq. (21) can be replaced by parameters available in literature, similar to the $\mathbf{p}_{nm}$ elements in the envelope function approach.

For both the envelope function method and the tight-binding method, the inclusion of more basis functions results in a more accurate band structure that can capture a larger part of the first Brillouin zone. If enough bands are included such that the full first Brillouin zone is captured, the model is called a full-zone model. For the envelope function method, this corresponds to a 30-band basis[40,41], for the tight binding method to the $\mathrm{sp^3d^5s^*}$ basis set[42]. With more basis functions, also the coupling between the different bands is captured more accurately (compare e.g. Fig. 8 with Fig. 9).

To solve Eq. (19) or Eq. (21) for an actual device in which current enters and leaves through the source and drain contacts, open boundary conditions are required. For TFET simulations, the quantum transmitting boundary method (QTBM) is often used[43]. QTBM imposes that the electric field is zero in the contacts in the transport direction. The wave function is then known to take the form of a plane wave in that direction. It is this form which is imposed as a boundary condition on the system.

With the appropriate boundary conditions, Eqs. (19) and (21) can be discretized and solved for the envelope functions and tight binding coefficients respectively. This direct solution approach is called the wave function method. Available numerical techniques include finite difference methods[44], finite element methods[45], spectral methods[46] and others. The envelope functions and the tight binding coefficients can be used to calculate important device characteristics such as carrier densities, transmission probabilities and currents. Similar to the semiclassical case, the current can be calculated from the transmission probabilities directly with Eq. (10), or more approximated by first converting to a generation rate and using Eq. (16). To include the effect of the carrier concentration on the potential energy profile, the calculated carrier densities can be used to calculate a new potential energy profile with the Poisson equation, which in its turn can be used to calculate a new carrier density. This loop is then repeated until self-consistency is reached.

Instead of solving Eqs. (19) and (21) directly as in the wave function method, an alternative is to calculate the non-equilibrium Green's function (NEGF)[38,47]. In an NEGF approach, Eq. (17) is rewritten as:

$$(EI - \hat{H} - \hat{\Sigma}_{S/D})G = I \tag{22}$$

with G the Green's function, $\hat{H}$ the Hamiltonian in the chosen basis and $\hat{\Sigma}_{S/D}$ the self-energies of the source and drain contacts. The self-energy terms are added to include the open boundary conditions. Just like the wave function, G contains all relevant device information. The advantage of the NEGF approach is that other interactions can be included in a rather straightforward manner by adding the corresponding self-energy term. E.g. for electron-phonon interactions:

$$(EI - \hat{H} - \hat{\Sigma}_{S/D} - \hat{\Sigma}_{el-ph})G = I \tag{23}$$

with $\hat{\Sigma}_{el-ph}$ the self-energy for the electron-phonon interaction[38]. In this way, rethermalization, phonon-assisted tunneling and other scattering processes can be described. To avoid having to calculate the inverse of a large matrix $(EI - \hat{H} - \hat{\Sigma}_{S/D} - \hat{\Sigma}_{el-ph})$, methods have been developed that calculate only the relevant entries in the Green's function matrix, such as the contact block reduction (CBR) method[48] and the recursive Green's function (RGF) method[38].

A separate quantum-mechanical framework based on wave functions has also been established for phonon-assisted tunneling[23]. It was shown that the current can be determined from solving Eq. (19) for each band separately. Two distinct sets of wave functions are then obtained for the conduction band and the valence band. The transmission probability is calculated based on the overlap of the wave functions of the two bands, combined with the interaction probability with a phonon of the appropriate momentum.

C. Semiclassical versus quantum mechanical

Compared to semiclassical approaches, quantum mechanical models are typically computationally more expensive, but include the effects of the wave-like nature of the electron, such as confinement and reflections in regions of high field or at a heterojunction. Quantum simulations should therefore be preferred in cases where confinement is expected to be strong, e.g. for TFETs with

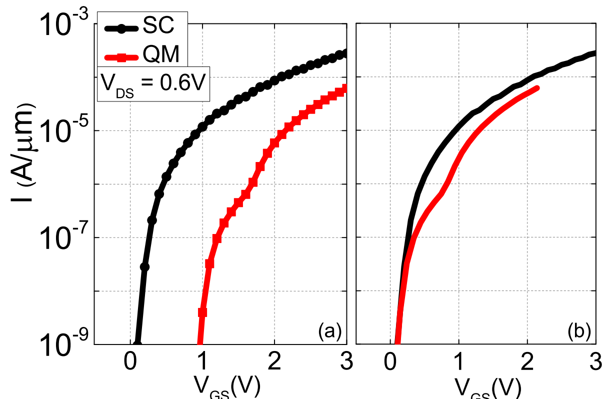

FIG. 10. Transfer characteristics of a Si lineTFET simulated with a semiclassical (SC) approach based on the WKB method and a quantum mechanical (QM) approach based on wave function overlap. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1\text{x}10^{-9}\text{A}/\mu\text{m}$ coincides.

a body thickness below the Bohr radius of the material, or when the tunneling is oriented toward the quantum well underneath the gate dielectric. Other cases include TFETs with a heterojunction[49] or configurations that rely on resonant tunneling[50].

To illustrate the differences that can exist between semiclassical and quantum mechanical approaches, Fig. 10 compares the simulated transfer characteristics of a Si lineTFET, whereby the last described quantum mechanical approach for phonon-assisted tunneling is used. Since the tunneling is oriented towards the gate, a strong impact of FIQC is expected. The effect of FIQC is visible for the quantum simulation as a shift in V_{onset} compared to the semiclassical prediction and a kink due to different subband ladders (see also Section IV B).

VI. CHALLENGES

Having a basic understanding of TFET and methods to model the tunneling current, the main challenges for TFET implementation are now discussed in more detail. Although the operating principle of the TFET is promising for low power applications, several important challenges remain. They can be summarized as reaching a high I_{ON} (Section VI A), combined with a low SS over several decades of current (Section VI B), while maintaining a low I_{OFF} (Section VI C). These three device characteristics are discussed with the appropriate metrics and the parameters which have an influence on them.

A. I_{ON}

The TFET I_{ON} is typically lower than that of a MOSFET. This is due to the tunneling barrier, which all charge carriers have to overcome before they can drift and diffuse toward the drain. This barrier is present even in the ON-state of the device. In contrast, in a MOSFET, the carriers with an energy higher than the source-channel barrier can drift and diffuse from source to drain unimpeded. The lack of sufficient drive current negatively impacts the intrinsic delay of a TFET inverter configuration, expressed as:

$$\tau_d = \frac{C_{ox} V_{\mathrm{DD}}}{I_{\mathrm{ON}}} \tag{24}$$

From Eq. (24), it is clear that to keep the delay small in low-V_{DD} operation, I_{ON} should be sufficiently high. In order to compete with MOSFET, it is generally accepted that I_{ON} should be in the range of several hundreds of μA/μm for V_{DD} smaller than 0.5 V[4].

To identify the parameters that increase I_{ON}, the Kane model can be used, although it is strictly speaking only valid for uniform fields. The exponential factors in Eqs. (11)-(15) show that the BTBT generation rate, and hence I_{ON}, is largest for a high electric field at the tunnel junction, a small bandgap and a small reduced effective mass. A high F and small E_G correspond physically to short tunnel paths, while the low m_R signifies a small attenuation along the path, as it is correlated with the imaginary dispersion in the bandgap. A short tunnel path and a small attenuation result in a high probability for the charge carriers to tunnel into the channel and contribute to the current. A high F can be obtained with sharp doping profiles and a large doping level at the tunnel junction, by increasing the source doping and/or with the introduction of a counterdoped pocket (see Section VIII). Additionally, F can be improved by enhancing control of the gate over the tunnel junction, e.g. by thinning the device body, by adding gates to obtain a multi-gate (MuG) configuration or by modifying the device structure to a line tunneling set-up (see Sections IV and IX). The small E_G and reduced m_R, on the other hand, are the result of a proper material choice, with III-V materials proving promising candidates, either in a homostructure (one material) or in a heterostructure (multiple materials) configuration (see Section VII).

B. SS

In addition to a high I_{ON}, a TFET should obtain a low, sub-60 mV/dec SS over a large current range of interest. The SS of a TFET at a specific V_{GS} can be approximated as:

$$SS = \frac{\mathrm{dV_{GS}}}{\mathrm{dlog_{10}I_{DS}}} = \ln(10)\left[\frac{1}{\mathrm{V_R}}\frac{\mathrm{dV_R}}{\mathrm{dV_{GS}}} + \frac{\mathrm{F+B}}{\mathrm{F^2}}\frac{\mathrm{dF}}{\mathrm{dV_{GS}}}\right]^{-1} \tag{25}$$

TABLE I. Examples of recent experimental values for I_{60} in literature, rounded to order of magnitude. Target value for I_{60} is 10 μA/μm or larger.

nTFET	I_{60} [μA/μm]	pTFET	I_{60} [μA/μm]
Tomioka et al.[53]	10^{-3}	Mayer et al.[54]	10^{-6}
Dewey et al.[55]	10^{-3}	Morita et al.[56]	10^{-5}
Sarkar et al.[57]	10^{-4}		
Huang et al.[58]	$<10^{-6}$		
Kim et al.[59]	$<10^{-6}$		

which is derived from an approximation of the tunnel junction as a degenerately doped p-n junction with a constant electric field[51]. V_R is then the reverse bias of the tunnel junction (E_{Fp}-E_{Fn}) and B is the exponential parameter of the Kane formalism (see Eq. (13) and Eq. (15)). Comparing Eq. (25) to Eq. (4) shows that in contrast to the MOSFET, the SS of a TFET is indeed not limited by $\frac{kT}{q}\ln(10)$. However, Eq. (25) also shows that the TFET SS is not constant with V_{GS}. It is therefore possible that the sub-60 mV/dec SS regime is only limited to very small levels of I_{DS}. In this case, reducing the supply voltage is still not feasible, as the majority of the SS is above the thermionic limit. The minimum value of the SS as described in Eq. (25) at a particular V_{GS}-point, also called the minimum point-SS, is therefore not a good metric to assess TFET performance. More relevant is to look at the average SS over the full operating voltage range, as shown in Fig. 11:

$$SS_{\mathrm{avg}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{OFF}}}{\log\left(\frac{I_{\mathrm{ON}}}{I_{\mathrm{OFF}}}\right)} \tag{26}$$

where V_{OFF} is the V_{GS} corresponding to the defined I_{OFF}. SS_{avg} still depends, however, on the choice of I_{OFF} and V_{DD}, which can vary depending on the targeted application. Therefore, another metric called I_{60} has been proposed[52]. I_{60} is defined as the point on the I_{DS}-V_{GS} curve where the SS transitions from sub-60 mV/dec to super-60 mV/dec (also indicated in Fig. 11). Hence, it is the largest current for which the corresponding TFET outperforms a theoretically optimal MOSFET. I_{60} is independent of the choice of I_{OFF}, V_{DD} or the gate workfunction, so it can be used to compare various TFET configurations presented in literature. To be competitive with MOSFET, I_{60} should be at least above 10 μA/μm[4,52]. As an example, Table I lists some experimental values obtained in literature. See also Section XII for more experimental results. These examples show that there is still a large gap with the SS goal.

From Eqs. (25) and (26), it is clear that SS can be minimized by increasing $\frac{dV_R}{dV_{GS}}$ and $\frac{dF_{\max}}{dV_{GS}}$, which represent the gate control over the tunnel junction, and by increasing the ratio I_{ON}/I_{OFF}. Physically, these requirements correspond to the capability of the gate to induce an abrupt transition from an OFF-state with a low tunneling probability to an ON-state with a very high tunneling

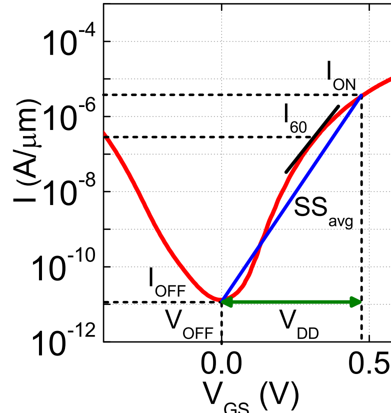

FIG. 11. SC simulated transfer characteristics of an $In_{0.53}Ga_{0.47}As$ p-i-n TFET as shown in Fig. 3, illustrating various metrics used to characterize TFET performance.

probability. This means the optimization of SS and I_{ON} are intertwined, with one generally benefiting from the improvement of the other. This is not true, however, for very high source doping levels. A large source doping improves I_{ON}, but can degrade the SS if the source degeneracy becomes too high, as was mentioned in Section III. For a given doping level, the source degeneracy is determined by the density of states (DOS) in the valence band (for an nTFET) or the conduction band (for a pTFET) of the source material. A large DOS allows for a high source doping while keeping the source degeneracy, and hence the SS degradation, small. As the conduction band for most common bulk materials has a lower DOS than the valence band, the pTFET has a more limiting trade-off between I_{ON} and SS. This puts the pTFET at an inherent disadvantage compared to the nTFET. This imbalance can be alleviated using dopant pockets, discussed in Section VIII.

The SS can be negatively impacted by parasitic current mechanisms which occur in addition to the desired BTBT process, such as trap-assisted tunneling (TAT)[60–62]. TAT is a process in which trap levels in the bandgap are used by the charge carriers as stepping stones between conduction and valence band (see Fig. 12(a)). These levels are localized energy states resulting from defects in the material, such as vacancies, impurities and dangling bonds in the bulk or at interfaces. The TAT transition itself consists of at least one ballistic tunneling step and a phonon-assisted thermal step to and from the trap level. This means TAT has both a field and a temperature dependence. TAT degrades the SS, as it can turn on at lower V_{GS} and add a thermal tail to the transfer characteristics. The impact of TAT can be reduced by improving the material quality, such that the trap density is low, or by enhancing the desired BTBT current, such that it better masks the current component caused by TAT. The amount of TAT present in the transfer characteristics can

be characterized by V_{TAT}@I_{OFF}, the increase in V_{onset} at 300 K at the specified I_{OFF} compared to the V_{onset} value at 77 K[63].

C. I_{OFF}

To obtain a low leakage power, I_{OFF} should be sufficiently small. I_{OFF} is composed of the reverse leakage current of a p-i-n diode, consisting mainly of SRH processes, minority carrier diffusion, and possibly some TAT if the other two mechanisms are sufficiently small. Additionally, parasitic TFET mechanisms such as ambipolar current and direct source-drain tunneling can increase I_{OFF}. For low-power applications, the ITRS roadmap sets the target for I_{OFF} at 10 pA/μm, with $\frac{I_{ON}}{I_{OFF}} > 10^5$.

SRH, similar to TAT, is a trap-assisted process in which carriers are generated via localized trap levels through phonon-assisted thermal steps when the electron and hole densities are out of equilibrium (see Fig. 12(b)). In contrast to TAT, SRH has a weak field dependence and so does not impact the SS. However, if the trap density is sufficiently high, it can increase I_{OFF}. Similar to TAT, the remedy is to decrease the trap density.

The ambipolar current is determined by the efficiency of BTBT at the channel-drain junction. This means it can be reduced by taking opposite measures as those suggested in Section VI A to increase I_{ON}, viz. a reduction of F and E_G and an increase in m_R at the channel-drain tunnel junction. F can be reduced by lowering the drain doping, at the expense of increasing the resistance. E_G and m_R depend on the material choice and cannot be varied independently from the source in a homostructure, but they can be in a heterostructure (see Section VII C). Another option is to introduce a gate-drain underlap region, which decreases the influence of the gate on the channel-drain junction[64] (see Section IX B). Using a combination of these techniques, the ambipolar current can be kept to acceptable levels.

Direct source-drain tunneling occurs when charge carriers can tunnel from source to drain, even when the device is in the OFF-state. This occurs when the tunnel paths in the OFF-state are too short or provide insufficient attenuation to suppress the carrier tunneling probability. Direct tunneling is particularly important in materials with a small E_G and m_R and in configurations with a short channel. In vertical architectures, increasing the channel length is a straightforward way to reduce the source-drain tunneling. In planar configurations, however, a longer channel length also increases the device footprint.

VII. MATERIAL CHOICE

To overcome the challenges outlined in the previous section, different material options are being considered for TFET. Of particular interest are materials from group

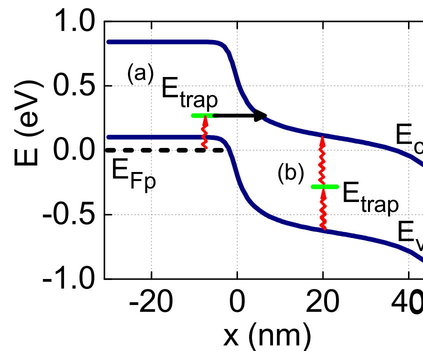

FIG. 12. Energy band diagrams of the tunnel junction of an $In_{0.53}Ga_{0.47}As$ TFET showing (a) TAT and (b) SRH processes, which contribute to the TFET I_{OFF}. The green lines represent localized trap energy levels, the red wavy lines are thermal steps and the black solid line corresponds to a tunneling step.

IV (Section VII A) and compounds from group III and V of the periodic system of elements (Section VII B). Multiple of these materials can be combined in a heterostructure (Section VII C). 2D materials are a new class of materials, which is also gaining interest for TFET applications (Section VII D).

A. Group IV materials

Silicon is the most prevalent material in today's MOSFETs for logic applications, and has therefore also been extensively studied for TFET. Si has the distinct advantage of being a well-known, abundant material that can be obtained with a very low density of defects in the bulk of the material as well as at the gate dielectric interface. Established fabrication infrastructure and processes exist in industry for a wide variety of process steps. This includes high quality oxide growth and high concentration doping. Si is also interesting for TFET because of its large conduction band DOS, which limits the source doping degeneracy in pTFETs (the importance of which is discussed in Section VI B).

However, Si is a relatively poor material for BTBT and consequently, Si TFETs typically have a small I_{ON}. A first cause is the relatively large E_G of 1.12 eV, which results in a low tunneling probability (see Section VI A). Although beneficial for I_{OFF}, the low tunneling rate is detrimental for I_{ON}. Secondly, Si is an indirect bandgap material, which reduces the overall efficiency of BTBT. The smallest E_G is measured between the valence band maximum at the Γ-point and the conduction band valley minimum along the Δ-direction[40]. These two points in the E-k diagram are not at the same k-value, which means they correspond to a different crystal momentum $\hbar$k. A tunneling transition between these two points requires a phonon to provide the necessary crystal momen-

tum. This makes it less probable for a given energetic separation than a direct transition, in which the start and end points of the tunneling process are at the same k-value, therefore requiring no phonon. In Si, the indirect transitions are dominant, since the bandgap at the Γ-point is much larger at 3.4 eV, making direct transitions very improbable[25].

As an alternative to Si in group IV of the periodic system of elements, Ge is more suited for BTBT. It has a smaller indirect bandgap than Si of 0.66 eV. Unlike Si, the direct bandgap at the Γ-point is only slightly larger at 0.8 eV. Consequently, once the band bending is such that direct transitions are allowed, they will dominate over the indirect transitions and improve I_{ON}[25,65]. However, as discussed in Section VI C, a smaller bandgap facilitates ambipolar tunneling at the channel-drain junction, which is an important leakage mechanism in TFET. I_{OFF} will therefore generally be larger than for Si implementations, but it is expected that acceptable levels of I_{OFF} can be reached.

Since it belongs to the same group as Si, Ge can also be used in an alloy with Si, forming Si_xGe_{1-x}, with x the Si mole fraction. x determines the band structure, including the bandgap and the relative importance of the indirect and direct processes. A rather abrupt transition occurs from Ge-like to Si-like behavior above x=0.2[25]. The control over the band structure through x can be used to find a compromise between improving I_{ON}, and reducing I_{OFF}.

B. Group III-V materials

Beyond group IV, a host of materials suited for TFET can be found in the group of III-V materials, which are compounds of elements from group III and group V. They are actively researched as future channel materials for MOSFET, because they can exhibit high electron mobilities compared to Si[66]. III-V materials show a wide variety of band structures, with bandgaps varying from 0.17 eV for InSb up to 3.28 eV for GaN[67]. The same variety can be found in the effective masses. The possibility of a small bandgap and small effective mass, combined with the direct nature of most III-V materials, makes them interesting candidates for improving the TFET I_{ON}. Important examples which have been studied for TFET applications are binary compounds like InAs, GaSb, InP and ternary compounds like $In_xGa_{1-x}As$ and $GaAs_xSb_{1-x}$[7].

Nevertheless, III-V materials also present significant challenges. Firstly, they are much less known than Si, so it is challenging to obtain high-quality materials and gate dielectrics with a low defect density[66]. Secondly, the material properties that allow for a high I_{ON} also raise I_{OFF} undesirably. A small bandgap combined with a low effective mass facilitates both ambipolar and direct source-drain tunneling. This issue can be alleviated with the use of a heterostructure as discussed in Section VII C. Thirdly, a low electron effective mass means a low DOS in the conduction band compared to Si. This exacerbates the I_{ON}-SS trade-off for pTFET for increasing source doping, discussed in Section VI B. Solutions exist in the form of dopant pockets, as discussed in Section VIII.

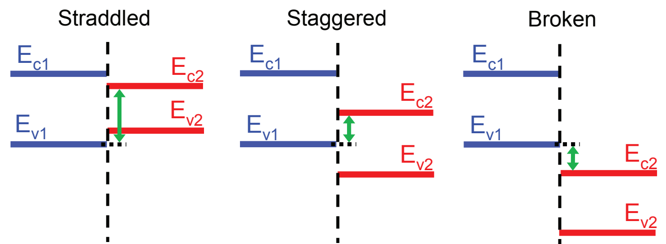

FIG. 13. Types of band edge alignments at a heterostructure tunnel junction. In a straddled alignment, $E_{c1} > E_{c2}$ and $E_{v1} < E_{v2}$. In a staggered alignment, $E_{c1} > E_{c2}$ and $E_{v1} > E_{v2}$. In a broken alignment, $E_{v1} > E_{c2}$. The green arrows indicate the effective bandgap at the tunnel junction. For the broken configuration, the effective bandgap is negative.

C. Heterostructures

The material options discussed so far assume that the active region of the device consists of only one material. For such a configuration, an important issue in the material choice is the link between I_{ON} and I_{OFF}, with the desired improvement of the former also inducing an unwanted increase in the latter. A way to decouple the two is to combine two materials in a heterostructure, such that the material in the source is different from the material in the channel and the drain.

A heterostructure configuration has an extra degree of freedom: the band edge alignment at the tunnel junction. The alignment is determined to a first approximation by the electron affinity of the two constituent materials, and is classified as straddled, staggered or broken, as shown in Fig. 13. The effective bandgap which determines the tunnel path lengths at the tunnel junction is determined by the alignment and not by the bandgaps of the individual materials. A hetero-TFET can therefore combine a very small effective bandgap at the source-channel junction, enabling a high I_{ON}, with a large bandgap at the channel-drain junction, maintaining a low I_{OFF}. Fig. 14 illustrates the performance improvement for a staggered heterojunction compared to a homojunction. The material of the source can also be chosen to have a large DOS, associated with a large bandgap, to limit the source doping degeneracy. This can be done without increasing the effective bandgap at the tunnel junction, so long as the band alignment remains favorable[68].

In the special case of a broken band alignment, there is no forbidden region through which the carrier has to tunnel. This enables a high transmission probability and is hence beneficial for I_{ON}. It is still unclear, however,

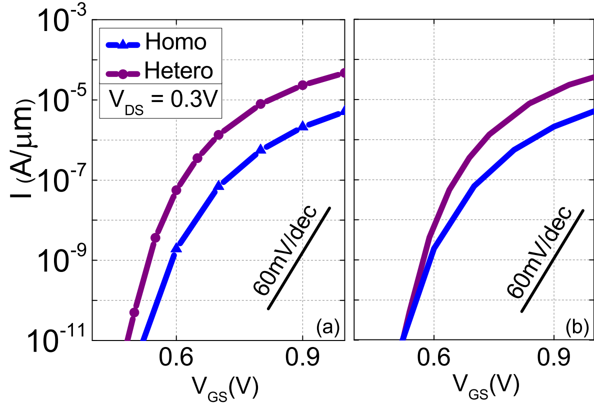

FIG. 14. QM simulated transfer characteristics for a $In_{0.53}Ga_{0.47}As$ (bandgap of 0.73 eV) homostructure TFET and a $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterostructure TFET. The heterostructure is lattice matched and has a staggered band alignment with an effective bandgap of 0.29 eV. The TFET is a double gate configuration with an EOT of 0.6 nm, a body thickness of 10 nm and a source doping of $5x10^{19}cm^{-3}$. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1x10^{-11}A/\mu m$ coincides. This shift can be accomplished by a proper choice of gate workfunction.

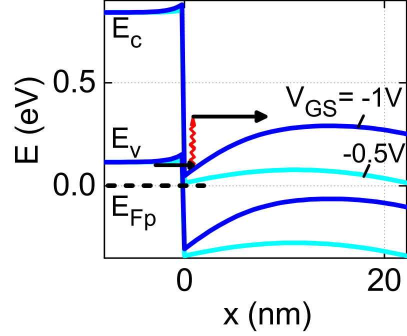

FIG. 15. Energy band diagram at the tunnel junction of a GaSb/InAs heterostructure TFET with a broken band alignment in the OFF (dark lines) and ON-state (light lines). V_{GS} is -1 V and -0.5 V respectively. Indicated is a leakage path in the OFF-state. The red wavy line represents a thermal step. The dashed line represents the quasi Fermi level for the holes in the source (E_{Fp}). The source doping is $5x10^{19}cm^{-3}$.

whether a broken gap alignment will allow for a sufficiently low I_{OFF}, since phonon-assisted leakage paths exist in the OFF-state[69,70]. This is indicated in Fig. 15: after transitioning from source to channel, a rethermalization step can enable the electron to pass over the potential barrier in the channel, resulting in an increased I_{OFF}. The importance of this leakage current is influenced by the quantization in the triangular wells at the junction and the interaction strength with the available phonons.

Depending on the choice of materials, heterostructures can be either lattice-matched or lattice-mismatched. In the first case, both materials have the same lattice constant. The materials can be grown epitaxially without any stress at the heterojunction. Notable examples include $In_{0.53}Ga_{0.47}As/InP$ (straddled) and $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ (staggered). In the second case, the mismatch of lattice constants results in a non-uniform stress profile arond the tunnel junction, as in the case of GaSb/InAs (broken). The stress has an impact on the local band structure (see Section X). The build-up of stress can also result in interfacial defects at the junction if relaxation sets in[71].

D. 2D materials

2D materials are an alternative to the bulk semiconductors described in the previous sections, and are being investigated for both MOSFET and TFET applications[72]. 2D materials are atomically thin, enabling excellent gate control. In addition, it is expected that low defect densities can be obtained with no dangling bonds or roughness at the surface.

The most studied 2D-material is graphene, but since it is a semi-metal, it does not have a bandgap and is therefore not suited for TFET as such. However, a bandgap can be introduced by symmetry-breaking operations such as patterning the graphene into nanoribbons, or by stacking two layers and applying an electric field[73]. This allows the bandgap to be tuned, either by controlling the size of the ribbon or the strength of the electric field.

Transition metal dichalcogenides (TMD) form an alternative to graphene in 2D TFET applications. TMDs are a class of 2D materials with chemical formula MX_2, with M a transition metal and X a chalcogenide. In contrast to graphene, TMDs do exhibit a variety of relatively large bandgaps. They can be used as the channel material of an atomically thin TFET[74–76] (see Fig. 16(a)), or layers of different TMDs can be stacked as a heterostructure, bonded by Van der Waals interactions. Tunneling then occurs in the overlap region of the layers, perpendicular to the gate (see Fig. 16(b)). Such 2D heterostructure TFETs are predicted to combine high I_{ON} and low I_{OFF} in the same way as bulk heterostructures[77]. TMDs can also be combined with a bulk semiconductor, such as MoS_2 on Ge[57] (see Fig. 16(c)). Challenges that remain for 2D materials are the development of large area defect-free production, good ohmic contacts and techniques to obtain high doping levels[72,78]. As a result of these challenges, only few experimental 2D TFETs with sub-60 mV/dec SS have been realized (see Fig. 30).

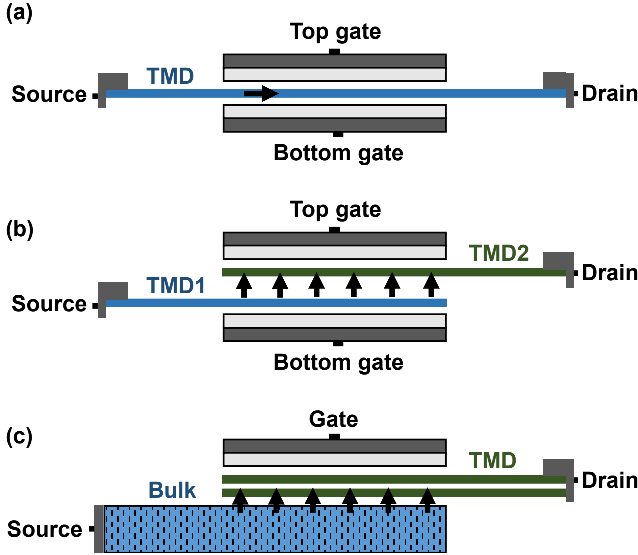

FIG. 16. TMD TFET configurations. (a) homojunction TMD TFET[74–76], (b) 2D heterojunction TMD TFET, also called a Thin-TFET[77] and (c) 3D-2D heterojunction bilayer TMD TFET, also called ATLAS-TFET[57]. The arrows indicate the direction of the tunneling paths.

VIII. DOPANT POCKETS

To improve SS and/or I_{ON}, another design option is to use dopant pockets. A dopant pocket is a localized region of doping, which locally modifies the device electrostatics. In a TFET, they can be used both in point tunneling (Section VIII A) and line tunneling (Section VIII B) configurations.

A. Pocketed pointTFET

In a pocketed pointTFET, a counterdoped pocket is added at the interface between source and channel to improve both I_{ON} and SS (see Fig. 17(a)). This forms a p-n-i-n doping profile in an nTFET, and a n-p-i-p profile for a pTFET. Compared to a p-i junction, the built-in field at a p-n junction is larger, corresponding to a stronger built-in band bending and hence an onset at lower V_{GS} and the potential for a higher I_{ON}[79–82]. As shown in the band diagrams of Fig. 18, for a properly designed pocket, the enhanced band bending induces an abrupt transition from long to very short tunnel paths at tunneling onset, compared to more gradual shortening seen in a standard p-i-n/n-i-p configuration. In the transfer characteristics this results in an improvement of SS, as shown in Fig. 19.

An additional effect of the pocket is that it reduces the impact of FIQC on the pointTFET performance. The strong built-in electric field at the tunnel junction forces the tunnel paths in a direction more parallel to the gate and induces tunneling before a strong band bending towards the gate, causing FIQC, is induced. The result is a shift of the BTBT onset to lower V_{GS} and a reduction of the stretching effect on the SS, discussed in Section IV A.

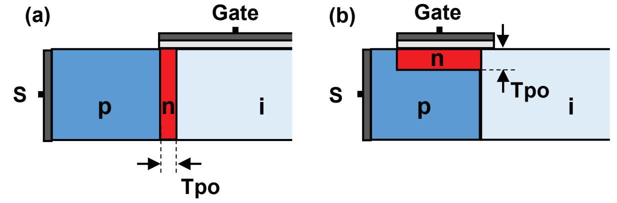

FIG. 17. Source-channel region of a pocketed (a) point tunneling and (b) line tunneling TFET configuration.

An optimum exists for the pocket thickness (T_{po}, see Fig. 17(a)). The strength of the built-in field, and consequently the improvement in I_{ON}, increases with T_{po} (see Fig. 20(a)). However, if the pocket is so thick that the concentration of free carriers in the pocket becomes large (close to the doping level in the source) and is larger than the concentration in the channel at the onset of tunneling, the abrupt onset is deteriorated by a potential barrier in the channel[82] (see Fig. 20(b)). At the first moment of cross-over between valence and conduction band, a dip is present in the energy bands at the tunnel junction, followed by a bump in the channel. For such a configuration, a further increase in V_{GS} only marginally goes toward increasing the band bending at the tunnel junction, but is consumed largely by a further increase of the carrier concentration in the pocket. The structure is then effectively a p-n diode in series with an n-i-n MOSFET. A good estimate for the optimal T_{po} is the depletion width at the tunnel junction[79,82]. Note that for configurations with a large body thickness, a thick pocket can cause an uncontrolled tunneling current through the body of the device.

A pocket can also be used to mitigate the deteriorating effects of a large source doping degeneracy on the SS. The doping in the source is kept low, except for a pocket at the source side of the source-channel junction. This pocket retains the built-in electric field, while the lower doping in the rest of the source reduces the degeneracy[83]. SS is consequently improved, while I_{ON} is maintained. The source pocket can be combined with a counterdoped pocket at the channel side, resulting in a $p^-p^+n^+$in configuration. This approach is particularly useful for III-V pTFET in which the source consists of a material with a low conduction band DOS, as discussed in Section VI B.

B. Pocketed lineTFET

In a pocketed lineTFET, a pocket is introduced to mitigate the impact of FIQC and to reduce the sensitivity to the gate-channel overlap (see Section IV B). The pocket is located in the source region, underneath the gate-source overlap and adjacent to the source-channel junction (see Fig. 17(b)). Similar to the pocketed point TFET, the doping type of the pocket is opposite to that

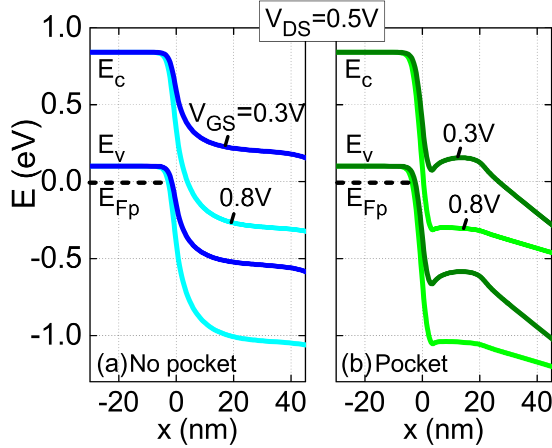

FIG. 18. Energy band diagrams of a $In_{0.53}Ga_{0.47}As$ TFET in the OFF (dark lines) and ON-state (light lines). V_{GS} is respectively 0.3 V and 0.8 V. (a) A no-pocket configuration and (b) a configuration with a 4 nm thick pocket at the source-channel junction as in Fig. 17(a). The source and pocket doping is $5x10^{19}cm^{-3}$. The EOT is 0.6 nm, with a body thickness of 20 nm. The dashed line represents the quasi Fermi level for the holes in the source (E_{Fp}).

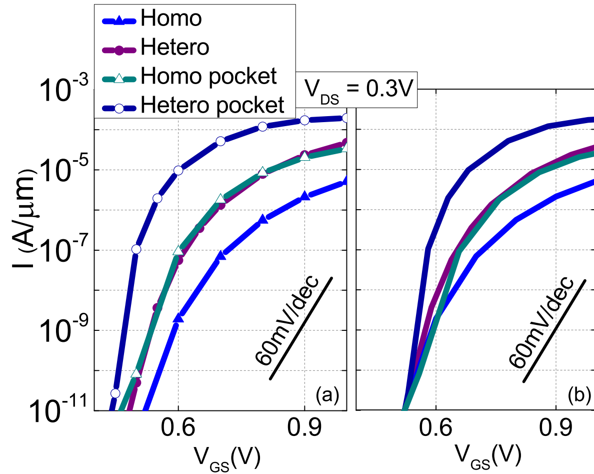

FIG. 19. QM simulated transfer characteristics of Fig. 14 compared to the transfer characteristics of the same configurations with a counterdoped pocket of 3 nm. The TFET is a double gate configuration with an EOT of 0.6 nm, a body thickness of 10 nm and a source and pocket doping of $5x10^{19}cm^{-3}$. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1x10^{-11}A/\mu m$ coincides. This shift can be accomplished by a proper choice of gate workfunction.

of the source.

The effect on the FIQC underneath the gate dielectric is shown by the energy bands of Fig. 21: the triangular well is rounded off and becomes wider for increasing T_{po}. The rounding reduces the FIQC, such that the subband quantization levels decrease in energy. The onset of vertical BTBT, determined by the first quantized level,

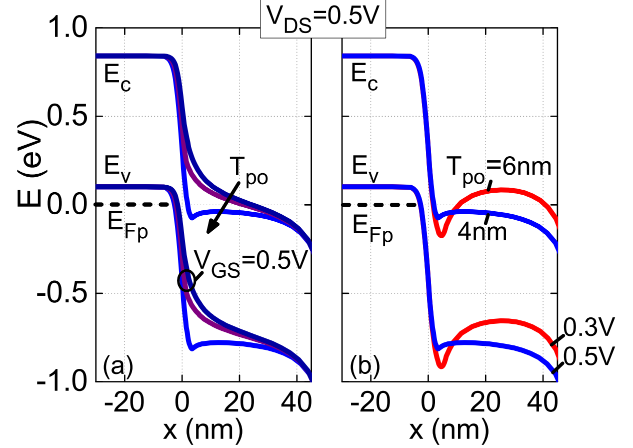

FIG. 20. Energy band diagrams of an $In_{0.53}Ga_{0.47}As$ TFET around onset of BTBT. The source and pocket doping is $5x10^{19}cm^{-3}$. The EOT is 0.6 nm, with a body thickness of 20 nm. (a) Impact of increasing T_{po} (0 nm, 2 nm and 4 nm) for a constant V_{GS} of 0.5 V, showing an increasing electric field at the tunnel junction. (b) Comparison of an optimal T_{po} of 4 nm to a larger T_{po} of 6 nm at onset, with the latter showing a potential bump in the channel. V_{GS} is respectively 0.5 V and 0.3 V. The dashed line represents the quasi Fermi level for the holes in the source (E_{Fp}).

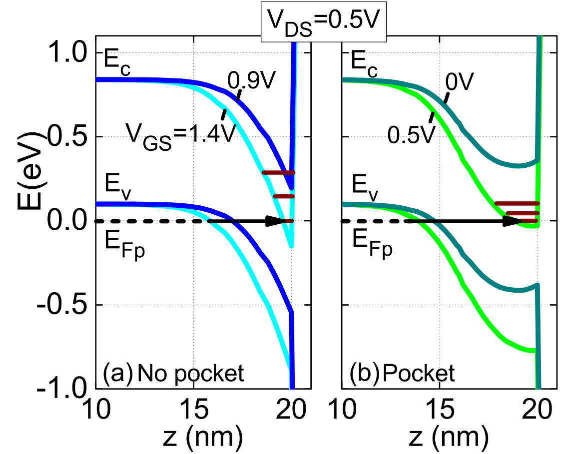

FIG. 21. Energy band diagrams of a $In_{0.53}Ga_{0.47}As$ lineTFET in the OFF (dark lines) and ON-state (light lines) along a vertical cutline through the center of the gate. The source and pocket doping is $5x10^{19}cm^{-3}$. The EOT is 0.6 nm, with a body thickness of 20 nm. (a) A no-pocket configuration for a V_{GS} of 0.9 V and 1.4 V and (b) a configuration with a 4 nm thick pocket underneath the gate as in Fig. 17(b) for a V_{GS} of 0 V and 0.5 V. Indicated in brown are estimations of the first three quantized energy levels inside the potential well for the highest V_{GS}. The dashed line represents the quasi Fermi level for the holes in the source (E_{Fp}).

therefore shifts to a lower V_{GS}. The resulting onset voltage V_{onset} can be calculated analytically as[84]:

$$V_{\text{onset}} = \frac{WF - \chi_e + E_{\text{sub}}}{q} - \frac{q(N_{\text{po}} + N_s)T_{\text{po}}}{C_{\text{ox}}} + \frac{1}{C_{\text{ox}}}\ldots \times \sqrt{2q\epsilon_s N_s \left[\frac{E_g + E_{\text{sub}}}{q} + \frac{q(N_{\text{po}} + 2N_s)T_{\text{po}}^2}{2\epsilon_s}\right] - q^2 N_s^2 T_{\text{po}}^2} \tag{27}$$

provided the pocket is fully depleted, with WF the work function of the gate, χ_e the semiconductor electron affinity, N_{po} and N_s respectively the doping level of the pocket and the source and E_{sub} the energy level of the first subband in the potential well underneath the gate, which can be solved from a 1D Schrödinger equation. Eq. (27) shows that by adjusting the thickness and doping of the pocket for a given WF of the gate, the FIQC-induced shift in V_{onset} seen in the no-pocket case can be removed. Note that for materials which are more prone to FIQC, i.e. those with a small effective mass and hence a large E_{sub}, the required T_{po} or N_{po} to compensate for the FIQC shift are larger.

In materials like Si, which have two distinct subband ladders in the well underneath the gate, the decreased FIQC has the added benefit of reducing the relative shift between the subband levels. The corresponding kink in the SS which was discussed in Section IV B is thereby also reduced, as shown in Fig. 22, where two pocketed lineTFETs are compared to a pocketed pointTFET configuration. For a thicker pocket, V_{onset} is reduced, while the relative shift of the two current components is decreased. The kink is not present in a III-V configuration with an isotropic conduction band effective mass, as shown in Fig. 23.

The presence of the counterdoped pocket also reduces the unwanted lateral point tunneling component by blocking the shortest lateral tunneling paths closest to the gate, since the source-channel p-i junction is locally replaced by a n-i junction. Combined with the earlier onset of vertical BTBT, the overall impact of the lateral component on the transfer characteristics is thus diminished, removing also the variability to the gate alignment.

The comparison of transfer characteristics in Fig. 22 and Fig. 23 shows that although the pocketed lineTFET outperforms the pocketed pointTFET in a Si configuration in terms of I_{ON} and SS, the difference becomes smaller for materials with a smaller bandgap, like $In_{0.53}Ga_{0.47}As$[82,85].

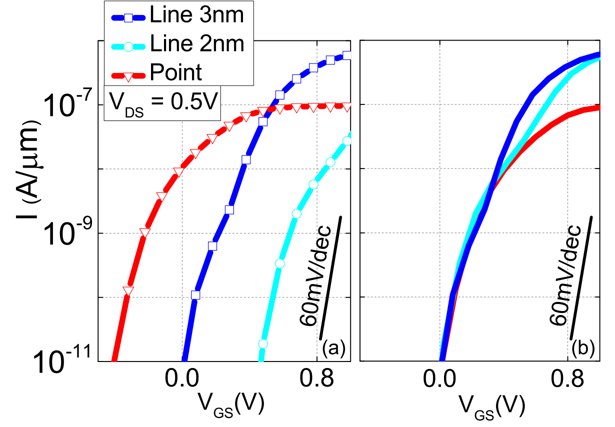

FIG. 22. QM simulated transfer characteristics of a Si pocketed pointTFET with a T_{po} of 4 nm and pocketed lineTFET with two different T_{po}. The TFETs are double gate configurations with an EOT of 0.6 nm, a body thickness of 20 nm and a source doping of $1\text{x}10^{20}\text{cm}^{-3}$. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1\text{x}10^{-11}\text{A}/\mu\text{m}$ coincides. This shift can be accomplished by a proper choice of gate workfunction.

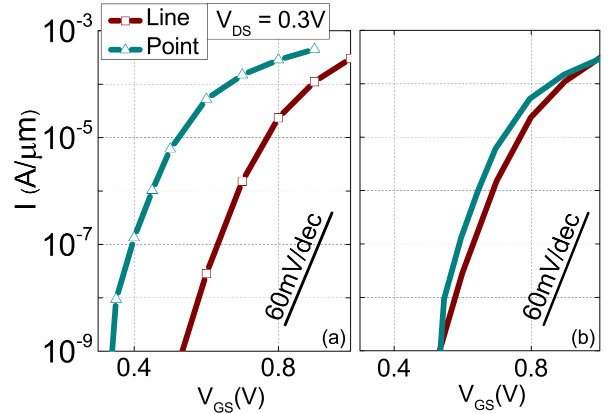

FIG. 23. QM simulated transfer characteristics of an $In_{0.53}Ga_{0.47}As$ pocketed pointTFET with a T_{po} of 3 nm and a pocketed lineTFET with a T_{po} of 6 nm. The TFETs are double gate configurations with an EOT of 0.6 nm, a body thickness of 10 nm for the pointTFET and 40 nm for the lineTFET and a source and pocket doping of $5\text{x}10^{19}\text{cm}^{-3}$. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1\text{x}10^{-11}\text{A}/\mu\text{m}$ coincides. This shift can be accomplished by a proper choice of gate workfunction.

IX. GATE STACK CONFIGURATION

As discussed in Section VI, the gate control is an essential factor in the BTBT efficiency. Gate control is characterized by two aspects. The first aspect is the portion of the gate voltage observable in the semiconductor, after the voltage drop over the oxide. This is directly related to the EOT. A second aspect is the degree in which a given variation in gate voltage moves the equipotential lines in the device closer together and hence increases the electric field locally. By tuning both aspects, the gate control at a tunnel junction can be enhanced or decreased.

To improve TFET performance for conventional logic applications, it is advantageous to enhance the gate con-

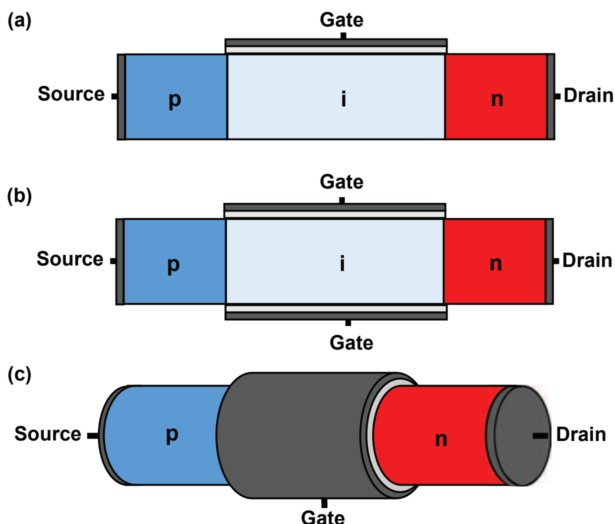

FIG. 24. (a) Single gate, (b) double gate and (c) gate-all-around TFET configuration.

trol at the source-channel tunnel junction (Section IX A), and to decrease it at the channel-drain junction (Section IX B). The former improves the TFET SS and I_{ON}, while the latter reduces the ambipolar current and C_{GD}. In this section, gate configurations addressing both requirements are discussed.

A. Improving source-channel BTBT

A first way to improve the gate control at the source-channel junction is to decrease the EOT, which increases the electrostatic potential drop in the semiconductor. Like a MOSFET, the TFET performance therefore benefits from the introduction of high-k materials as the gate dielectric[86–88].

A second way to improve the gate control at the source-channel junction is to go from a single-gate (SG) to a multi-gate (MuG) to a gate-all-around (GAA) configuration[89,90] (see Fig. 24), an approach which is also applied to MOSFET. This requires a transition from a planar to a protruding structure. A multi-gate configuration can be implemented as a finFET, where the gate covers three sides of the device body. Going further, the TFET body can be realized as a horizontal or vertical nanowire (NW), with the gate wrapped around.

The tighter gate control can be seen when comparing the electrostatic profile of a single gate to that of a double gate configuration[89] (see Fig. 25). When a second gate is added, the equipotential lines are curved more strongly. A consequence is that the electric field close to the source region is enhanced and hence the tunnel path lengths are reduced, improving I_{ON}. The electric field is now increasing towards the source region. Therefore, a given increase in V_{GS} results in a larger increase in electric field than in the single-gate configuration, because the electric field now increases both due to a larger total voltage drop between source and gate, and because the tunneling moves closer to the source where the equipotential lines are more closely spaced, and the electric field is higher. The result is a beneficial impact on the SS. This effect is enhanced further for a MuG or GAA structure as illustrated in Fig. 26(a).

Further scaling of the body thickness has an additional beneficial impact on the gate control. As the gates move closer together, the curvature of the equipotential lines becomes more pronounced, and the electric field hence increases. As explained in the previous paragraph, this benefits the SS of a pointTFET as illustrated in Fig. 27 for a pocketed point TFET. For a double gate lineTFET, the body scaling does not benefit performance above a certain minimum body thickness, as the gate depletes the source locally underneath the gate and tunneling starts from close to the undepleted source region (see Fig. 21), which is at source voltage. Hence, the two depleted source regions underneath the two gates are disconnected in the lineTFET.

Although body scaling can improve performance, size-induced quantum confinement (SIQC) effects become more important as the body thickness is scaled to dimensions comparable to the exciton Bohr radius of the material[91,92]. SIQC results in a global increase of the material bandgap, and hence an increase in tunnel path lengths. As discussed in Section VI, this can be detrimental for I_{ON} and can consequently undo some of the advantage that comes with improved gate control. In particular, a GAA structure is more affected by SIQC than a MuG or SG configuration as it is confined in two directions. Fig. 26(a) shows this can even result in a smaller I_{ON} for the GAA configuration than for the DG configuration. Similar to the case of FIQC, materials with small effective masses are more affected by SIQC.

Specific care must be taken when scaling the body thickness of lineTFET or pointTFET configurations, to prevent excessive depletion of the source region[82,93]. Underneath the gate-source overlap, a depletion region extends into the source, with a maximal extent in the ON-state (as explained in Section III A). If the body of the device is too thin, the depletion regions of different gates touch even before the device reaches the ON-state, resulting in depletion of the source over the full body thickness. For a lineTFET, this means no more tunnel paths perpendicular to the gate are available. Only much longer non-orthogonal tunnel paths are available and the current drops accordingly (see Fig. 27). Since the lineTFET operation depends on the gate-source overlap, the body thickness can therefore not be scaled below a certain critical thickness. This thickness is determined by the sum of the depletion lengths underneath the gate-source overlaps in the ON-state. The depletion lengths themselves are determined by the doping level of the source and of the pockets, if present. In a pointTFET, depletion over the full body thickness increases the tunnel path lengths, resulting in a drop in current for high V_{GS}. In this case,

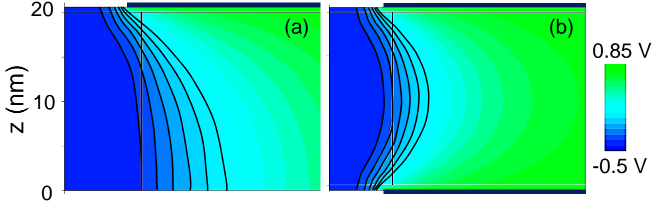

FIG. 25. Electrostatic potential profiles at the source-channel junction for a (a) single gate and (b) double gate $In_{0.53}Ga_{0.47}As$ p-i-n TFET at a V_{GS} of 1 V and a V_{DS} of 0.5 V. Six contour lines have been highlighted in each configuration.

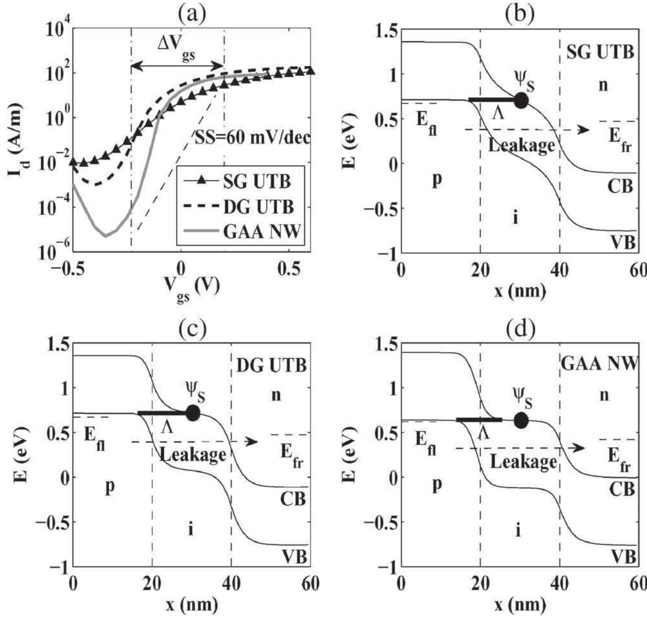

FIG. 26. (a) QM simulated transfer characteristics at V_{DS} = 0.2 V of InAs (line with triangles) SG ultra thin body (UTB), (dashed line) DG UTB, and (gray line) GAA NW devices. Body thickness or diameter is 6 nm. The NW current is normalized with its diameter. The OFF-to-ON gate voltage swing Δ-V_{GS} is indicated. (b) CB and VB edges along the transport direction x of the 6 nm p-i-n SG UTB device at the onset gate voltage. Λ indicates the tunneling barrier width, ψ_S is the electrostatic potential in the middle of the gate, and E_{fl} and E_{fr} denote the source and drain Fermi levels, respectively. (c) Same as (b) for the 6 nm DG UTB device. (d) Same as (b) and (c) for the 6 nm GAA NW device. Current leakage paths are indicated by dashed arrows in (b), (c), and (d) ©2009 IEEE. Reprinted, with permission, from *IEEE Elec. Dev. Lett.* vol. 30, no. 6, pp. 602604, 2009.

full depletion of the source can be avoided by reducing or removing the gate-source overlap for thin body thicknesses.

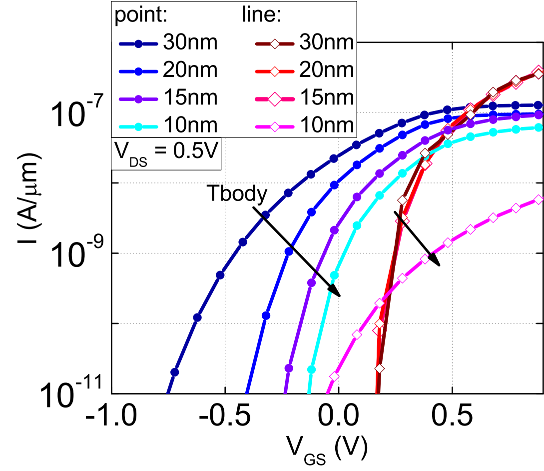

FIG. 27. QM simulated transfer characteristics of Si pocketed point and lineTFETs for varying body thickness. The configurations are as shown in Fig. 17, but have a double gate. The gate-source overlap for the 10 nm body pointTFET configuration is removed. For the lineTFET, the length of the gate-source overlap and the pocket are 20 nm. The EOT is 0.6 nm. Source and pocket doping are $1x10^{20}cm^{-3}$.

B. Reducing channel-drain BTBT and C_{GD}

The ambipolar current can be reduced by introducing a gate-drain underlap[64] (see Fig. 28(a)). The underlap decreases the gate control on the channel-drain junction. Since the desired BTBT takes place locally at the source-channel junction, the gate does not have to cover the full channel as in a MOSFET to enforce a particular band bending and hence tunnel path length at the source-channel junction. The underlap increases the distance between the gate and the channel drain-junction and consequently reduces the BTBT efficiency at the drain. The short gate has the added benefit of reducing C_{GD}, which is responsible for the Miller effect (see Section XI C). Shortening of the gate can proceed down to the length at which it loses control over the source-channel junction (typically lengths of 10 nm and below). Care has to be taken as well that the resistance in the ungated channel region does not surpass the resistance of the tunnel barrier, to avoid an observable reduction in the desired TFET current.

Instead of removing part of the gate, an alternative is to make the gate heterogeneous, for instance by introducing two different metals, each with a different work function[94] (see Fig. 28(b)). This is also called a dual material gate TFET. Although both metals are biased at the same V_{GS}, the work function at each of the tunnel junctions (source-channel and channel-drain) determines the amount of local band bending and hence the local tunnel barrier. The two work functions can be optimized separately: at the source-channel junction for a minimal tunnel barrier in the ON-state and at the channel-drain

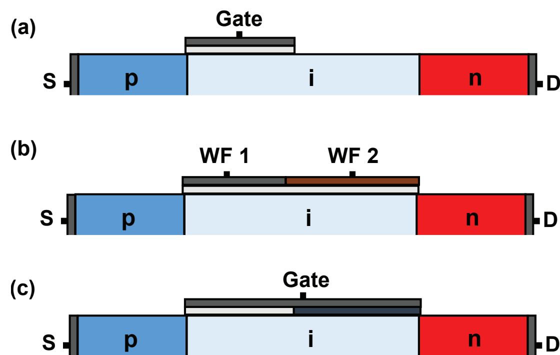

FIG. 28. Gate stack configurations for a p-i-n TFET aimed at reducing ambipolar behavior. (a) Short gate, (b) dual metal work functions and (c) dual EOT dielectric.

junction for a maximal tunnel barrier in the OFF-state.

The same can be achieved by reducing the EOT only at the source-channel junction, while retaining a large EOT at the channel-drain interface[95] (see Fig. 28(c)). This can be implemented with different physical oxide thicknesses, or with a high-k dielectric at the source side and a low-k dielectric at the drain.

X. STRAIN

Similar to a MOSFET, mechanical strain impacts TFET performance. This is a result of the effect strain has on the band structure (Section X A), an effect which can be incorporated in TFET models (Section X B). Strain can be externally applied as a performance booster, and is also intrinsically present at a lattice-mismatched heterojunction (Section X C).

A. Impact of strain on the band structure

Mechanical strain can have an important effect on the band structure of a semiconductor, since it alters the bond lengths and changes the crystal symmetry[96]. Firstly, strain warps the curvature of the energy bands, and hence influences the effective masses. This effect is exploited in MOSFETs to increase carrier mobility, by choosing a strain configuration such that the effective masses in the transport direction are decreased[97]. Secondly, strain shifts the relative positions of valley edges, such that the bandgap changes. Thirdly, as a result of broken symmetries, strain lifts certain energy band degeneracies, which modifies the DOS. Most notably, strain can lift the degeneracy between the heavy and light hole valence band.

B. Strain modeling

A common approximate model to study the effect of strain on the band structure is the deformation potential model[98]. The strain due to the deformation is assumed to be small and gradually varying, such that the effect on the energy band edges can be treated as if it were a small applied electrostatic potential. The shift in the band edges then varies linearly with the strain components:

$$\Delta E_n = \sum_{ij} \Xi_{ij} \varepsilon_{ij} \tag{28}$$

with E_n the band edge of band n, ε_{ij} the elements of the strain tensor and Ξ_{ij} the so-called deformation potential constants, available in literature. The deformation potential model can be directly applied in semiclassical effective mass-based simulators as a correction on the band edges.

Strain can be introduced into more complex band structure models as well. In the **k·p**-model, strain can be incorporated by the addition of a strain interaction term as proposed by Pikus and Bir[99], which includes the deformation potential constants of Eq. (28). In the tight-binding approach, the integrals of Eq. (21) are adjusted based on the strain-induced change in bond lengths and angles[100]. The introduction of strain in these models accounts for both the shift in band edge energies and the change in effective masses. Strained band structure models can be used in fully quantum mechanical simulations, but are also useful to extract band edge energies and effective masses, which serve as inputs to semiclassical models[101].

C. Strain in TFET

Since TFET operation depends heavily on the band structure, strain affects the TFET performance. Strain can be induced intentionally like in a MOSFET, e.g. by external stressors, to improve I_{ON} by reducing E_G and m_R[102] (see Section VI A). Similarly, the shifting of the band edges due to strain can induce a more favorable band alignment at a heterojunction[103] (see Section VII C). Specifically in indirect materials, the relative shift of conduction band valleys can render the material direct[104]. This is of particular interest in Ge, where the difference between the indirect and direct bandgaps is small.

Under uniaxial or biaxial strain conditions, however, the valence band DOS is reduced due to the splitting of heavy and light hole bands. This is a result of a reduction of crystal symmetry. The smaller valence band DOS increases the source doping degeneracy and can hence result in an SS degradation (see Section VI B). The degradation can be prevented with a lowly doped source region in combination with a highly doped pocket at the tunnel junction, as discussed in Section VIII A. Fig. 29 illustrates using **k·p**-based quantum mechanical simulations

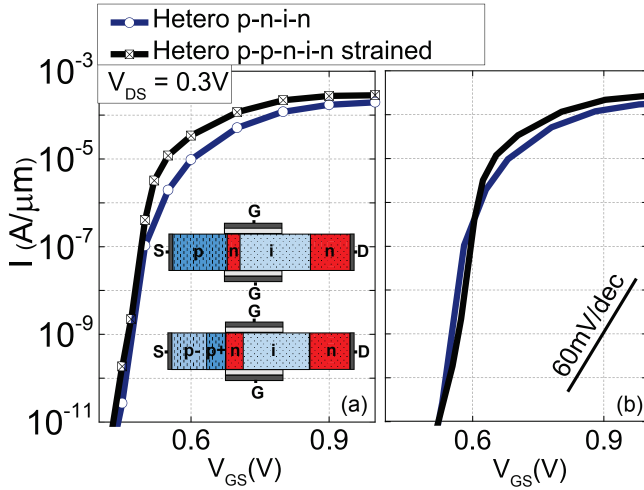

FIG. 29. QM simulated transfer characteristics of the unstrained pocketed $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ pointTFET of Fig. 19 compared with a $p^-p^+n^+$in version of this TFET (inset). The latter TFET is under a uniform tensile biaxial strain of 500 MPa and has a p-type pocket of 4 nm and and an n-type pocket of 3 nm, both with a doping of $5x10^{19}cm^{-3}$. The source doping is $5x10^{18}cm^{-3}$. The TFET is a double gate configuration with an EOT of 0.6 nm and a body thickness of 10 nm. The strain was included in the quantum mechanical simulations using a **k·p**-based model. (a) Unshifted and (b) shifted characteristics such that the V_{GS} at which I_{OFF} is $1x10^{-11}A/\mu m$ coincides. This shift can be accomplished by a proper choice of gate workfunction.

that with this approach uniform strain can be used to further improve performance[103].

Strain can also be inherently present in a TFET, e.g. at the heterojunction of two lattice mismatched materials. The strain profile in this case is very non-uniform, making it difficult to predict the exact impact on the TFET performance.

XI. CIRCUIT CONSIDERATIONS

Certain TFET features require additional care when designing circuits. The most important are the ambipolar effect (Section XI A), the asymmetrical structure (Section XI B), the Miller capacitance (Section XI C) and the superlinear onset in the output characteristics (Section XI D).

A. Ambipolar effect

The TFET ambipolarity can result in an increased switching leakage in a TFET inverter, but can just as well be used to design more compact digital and analog circuits if the positive and negative switching of the gate voltage to turn on the tunneling current is exploited[105,106]. For good ambipolar behavior in these applications, both the source-channel and channel-drain junction have to be optimized to obtain similar I_{ON} and SS. This stands in contrast to conventional logic applications, in which the channel-drain tunneling is suppressed (Section IX B). In digital circuits, the ambipolarity can be used to create more complex logic gates with fewer components[105]. These ambipolar gates have control inputs that determine the bias point, and hence the polarity of the devices. In analog applications, an ambipolar amplifier for example, exhibits both positive and negative small-signal gain, depending on the bias point[106]. This allows it to function as both a common-source and common-drain amplifier, without changing the physical implementation.

B. Asymmetrical structure

Unlike a MOSFET, the TFET has an asymmetrical source and drain doping and therefore behaves significantly different for a positive or negative V_{DS} polarity[107]. As the p-i-n diode is reverse biased in normal TFET operation, the sign of V_{DS} is fixed to positive for nTFET and negative for pTFET. When properly designed, the dominant current is BTBT-based with leakage mechanisms as described in Section VI C. Reversing the sign of V_{DS} brings the p-i-n diode in forward bias. At small forward bias, the current is typically negligible compared to the current at similar reverse bias, except for designs with sufficiently high source doping such that (Esaki-) tunneling becomes significant[108]. Even then, a drop in current is typically present upon increasing V_{DS} as the tunneling decreases, before the forward bias diode diffusion current reaches sufficiently high values to become dominant.

The asymmetrical TFET conduction can be a concern for Static Random Access Memory (SRAM) circuits. In standard 6-transistor (6T) SRAM cells, the two access transistors are required to conduct current in two directions. The asymmetrical conduction leads to unacceptable read and write static noise margins and hence instability of the SRAM cell[109]. Alternative SRAM cell designs with increased number of transistors have been proposed to circumvent this issue[109,110].

Weak conduction in one direction also prevents the discharging of transient noise signals that appear on a circuit node through capacitive coupling[111]. These signals can at times become very large and significantly surpass V_{DD} and therefore be detrimental to device reliability. Also the circuit timing suffers from these excessive noise signals. To alleviate this issue, the forward Esaki tunneling current present at low V_{DS} can be used to evacuate the excess charge. This requires a sufficiently high degeneracy in the source.

Several other logic circuits, like the basic inverter, are mostly unaffected by the asymmetry. It is even possible for specific basic circuits to exploit the unidirectionality to redesign the circuit with fewer transistors than in conventional CMOS, e.g. the pass-gate multiplexor[111].

C. Miller capacitance

A high C_{GD} creates an enhanced Miller effect, which results in over-and undershoots in the transient behavior of an inverter. The peak voltages V_P of the over- and undershoots can be expressed as[112]:

$$V_P = \frac{C_M}{C_M + C_L} V_{DD} \tag{29}$$

with C_L the load capacitance of the inverter and with C_M comprising the C_{GD} of both nTFET and pTFET of the inverter. It is possible to decrease V_P by increasing C_L, but this has the downside of also increasing the inverter fall time delay. Care must therefore be taken in the device design to keep C_{GD} low in the first place.

The gate capacitance division in gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} is different from the MOSFET-case, because charge injection from the source requires a tunneling event, while charge injection from the drain is via thermal injection, similar to the MOSFET-case. Therefore, when the tunneling efficiency at the source side is comparatively low, and in the absence of a strong SRH process, the carriers in the channel are supplied by the drain and the full channel determines C_{GD}. C_{GS} is then determined by the depletion of the highly-doped source region, hence resulting in a decreasing capacitance with increasing V_{GS} (nTFET). The channel charge is determined by the position of the drain Fermi level and the conduction band in the channel (nTFET). A channel material with a lower DOS in the conduction band (nTFET) hence results in a smaller charge build-up in the channel and the corresponding C_{GD} is also smaller[112]. Despite the fact that $C_g \approx C_{GD}$ if the tunneling efficiency at the source is low, the C_{GD} can hence be limited if the TFET is properly designed. Also a gate-drain underlap can help to reduce the Miller effect[113].

In cases where the tunneling efficiency is high and the device is fully in the ON-state, a significant amount of charge in the channel is supplied by the source. Like a MOSFET, the TFET then exhibits a linear region, in which charge is contributed equally by source and drain, and a saturation (pinch-off) regime, in which charge is uniquely supplied by the source. The gate capacitance is divided accordingly between the contacts. Improving the source tunneling efficiency is therefore also beneficial in reducing the Miller effect.

D. Superlinear onset

As discussed in Section III C, the TFET output characteristics can have a superlinear onset[19–21]. The small current at low V_{DS} delays the last part of the charging or discharging of the load capacitance in a TFET inverter. This increases the inverter rise and fall times and hence increases the total circuit delay. Additionally, recovery from transient noise signals is less efficient when the output characteristics are superlinear[114]. As suggested in Section III C, the superlinear onset can be reduced by improving the BTBT efficiency at small V_{DS}.

XII. EXPERIMENTAL STATUS

After describing the device physics and architecture options in previous sections, this section is intended to give an overview of experimental realizations. The current status of experimental TFET transfer characteristics is summarized in Fig. 30[17,53,55–58,81,115–129]. The curves have been selected to have a point-SS lower than 70 mV/dec, which means they are either close to or below the ideal MOSFET limit of 60 mV/dec for a given voltage range. A variety of experimental techniques is used to fabricate these structures[8]. Some configurations can be seen to obtain a sub-60 mV/dec SS, demonstrating the steep switching potential of TFET. None of the displayed curves, however, attains all requirements for SS, I_{ON}, I_{OFF} and I_{60} as specified in Section VI, and which are required to be a viable replacement for MOSFET. The comparison between nTFET and pTFET shows that fewer experimental realizations of pTFET exist, with a performance generally inferior to nTFET. The reasons behind this discrepancy are discussed in Section VI B. It is clear from Fig. 30 that a gap still needs to be closed between the promising theoretical predictions and actual experiment. Note, however, that some configurations which are promising in simulations, confined III-V heterostructure NW, are challenging to fabricate, and have not yet been experimentally realized.

XIII. CONCLUSIONS AND OUTLOOK

In this article, the TFET was discussed from the perspective of device physics. The basic operating principle based on BTBT enables the TFET to obtain a sub-60 mV/dec SS at room temperature. This makes it a promising candidate to circumvent the increasing power issues in scaled MOSFET technologies. The main challenges for TFET are to obtain a low average SS, a high I_{ON} and low I_{OFF}, or stated differently: a high I_{60}, and this for both nTFET and pTFET. Accurate predictive models are required to meet these challenges, with quan-

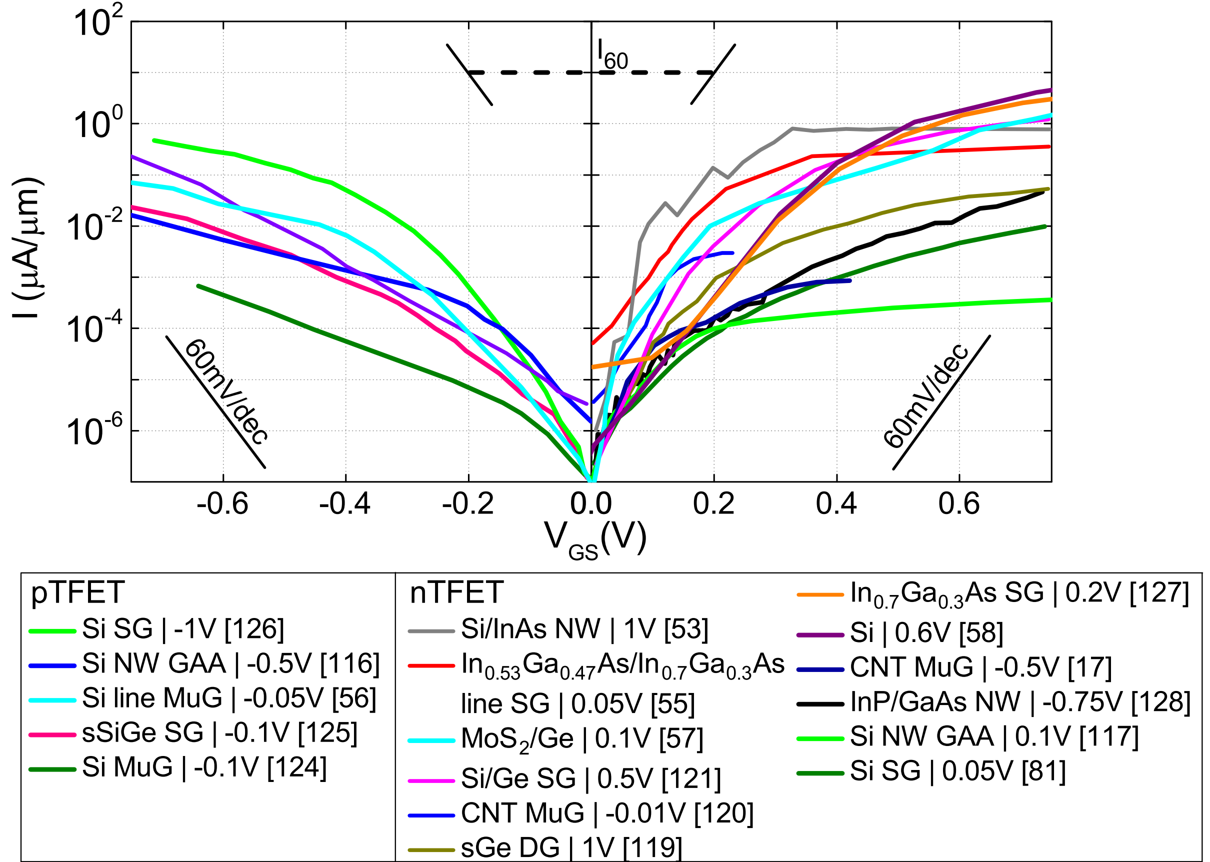

FIG. 30. Experimental transfer characteristics in literature of nTFET and pTFET. Only curves with an SS lower than 70 mV/dec have been included. The legend includes the material system (s-prefix stands for strained), gate configuration and V_{DS}. The legend entries are ordered according to the intersection of the corresponding curves at a V_{GS} of -0.2 V and 0.2 V. Also indicated is the target value for I_{60} mentioned in Section VI B. This figure is an updated version of Fig. 2 of Lu *et al*[7].

tum mechanical simulators complementing more and more the semiclassical models typically used for MOSFET. These models can help in choosing the optimal material system, with alternative group IV materials, III-V materials and 2D materials proving interesting alternatives for Si. Combining materials in a heterostructure provides an additional degree of freedom in the device design. Other performance improvements can be gained from dopant pockets or from an optimization of the gate stack configuration. The presence of strain can have a beneficial effect on the device performance. Finally, several specific characteristics of the TFET operation at a device level also have consequences for its use in circuits, suggesting the need for co-optimization of device and circuit. The gap between theoretical predictions and experimental realizations today shows that many challenges are still to be overcome, before the TFET's appearance in low-power products.

XIV. LIST OF ABBREVIATIONS

BGN: BandGap Narrowing
BTBT: Band-To-Band-Tunneling
CMOS: Complementary Metal-Oxide-Semiconductor
DG: Double Gate
DOS: Density Of States
EF: Envelope Function
EOT: Effective Oxide Thickness
FIQC: Field-Induced Quantum Confinement
GAA: Gate-All-Around
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
MuG: Multi-Gate
NEGF: Non-Equilibrium Green's Function
NW: NanoWire
QM: Quantum Mechanical
QTBM: Quantum Transmitting Boundary Method
SS: SemiClassical
SIQC: Size-Induced Quantum Confinement

SG: Single Gate
SRAM: Static Random Access Memory
SRH: Shockley-Read-Hall
SS: Subthreshold Swing
TAT: Trap-Assisted Tunneling
TFET: Tunnel Field-Effect Transistor
TMD: Transition Metal Dichalcogenide
WF: Work Function
WKB: Wentzel-Kramers-Brillouin

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