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Cu passivation for integration of gap-filling ultralow-k dielectrics

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For Cu/low-k interconnects, the reversed damascene is an alternative integration approach where the metal wires are patterned first and then the spacing filled with a flowable dielectric. In this paper, the replacement of a sacrificial template by gap-filling ultralow-k dielectrics is studied, focusing on yield and transport performance (“replacement dielectric” scheme). On non-passivated copper, the low-k curing processes induce severe damage to the metal lines, leading to the degraded electrical properties. This is confirmed by chemical inspection on the blanket Cu films and morphological inspection on patterned structures. In order to avoid Cu oxidation and out-diffusion at elevated temperature, Cu passivation by plasma-enhanced chemical vapor deposition SiCN is proposed and studied in detail. The inter-metal dielectric properties of replacement low-k are evaluated by resistance-capacitance and IV measurements using a Meander-Fork structure. By tuning the passivation layer thickness and ultraviolet curing time, high electrical yield is obtained with integrated porous low-k showing promising effective k-values (k_{eff}) and breakdown voltages (E_{bd}), confirming the interest of this specific integration scheme. *Published by AIP Publishing.*
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In advanced semiconductor manufacturing, interconnects require low dielectric constant (low-k) materials¹ in order to reduce power dissipation, cross-talk noise and resistance-capacitance (RC) signal delay. Among the variety of low-k materials, porous organosilicate glass (p-OSG) materials are currently the most successful candidates.^{2,3} Using chemical-vapor co-deposition of matrix and porogen precursors, continuous k value reduction is achieved by increasing the porogen/matrix ratio so as to generate higher open porosity. However, larger porosity is generally accompanied by an increased pore size,⁴ leading to poor mechanical integrity and poor resistance to plasma induced damage,⁵ lowered chemical resistance (wet clean),⁶ deep metal penetration during barrier deposition^{7,8} and enhanced slurry residues after Cu chemical mechanical polishing.^{9,10} As a result, the “effective” k-values for integrated inter-metal dielectrics are significantly higher than those of pristine materials.

Integrated k-value scaling for p-OSGs has attracted the attention of many research groups. Many potential solutions have been put forward in order to reduce the plasma induced damage, including low damage plasma chemistry,¹¹ post etch low-k restoration,¹² late porogen removal¹³ and pore protection by sacrificial polymers.^{14,15} However, all those solutions show either insufficient improvement or limited compatibility with the interconnect fabrication processes. In addition, the metallization of this porous substrates is also becoming more and more challenging: the penetration of metal-based species during physical-vapor or chemical-vapor deposition of the metal diffusion barrier causes issues of barrier continuity, too high leakage and high effective

dielectric constant.¹⁶ In order to ensure barrier continuity, in the presence of >1 nm pore radius, thicker barriers are required, which have such high resistivity that after Cu filling, the target line resistance cannot be achieved. Several “pore sealing” approaches^{17–19} have been explored so as to enable the deposition of continuous nanometer-scale thin metal diffusion barrier. Pore protection approaches can also potentially reduce the barrier penetration by using post CMP polymer burnout.²⁰ However, the temperatures required for complete removal of porogen residues or sacrificial polymers exceed 400 °C, which is considered to be too high for Cu metallization. In the recent studies, the porogen residues or sacrificial polymers were burnt out after low-k etching to avoid negative impact on metallization structures.^{21,22} In summary, the integration of ultra-porous low-k dielectrics by conventional damascene technology meets huge challenges and k-value scaling is far below expectation.

Given the increasing difficulty of integrating advanced porous low-k, it makes sense to reconsider the subtractive approach, where the metal structure is defined first, followed by a dielectric deposition. In spite of many research efforts on Cu direct etch and gap fill dielectrics,^{23–25} there has been limited success in providing satisfactory morphological profile and electrical performance in the technology-relevant dimensions. The present work investigates a “replacement” integration approach²⁶ that essentially relies on metal patterning by using a sacrificial template, which is afterwards replaced by a gap-filling ultralow-k dielectric. Fig. 1(a) shows a simplified Cu/low-k integration flow using this so-called “Replacement Dielectric Approach.” Trench/via is formed first by the conventional patterning of a sacrificial C-based high thermal stability material. A satisfactory morphological profile is obtained, as shown in Fig. 1(b). After

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FIG. 1. (a) Simplified Cu/low-k interconnect process flow using low-k replacement approach. Cross-sectional scanning electron microscopy (SEM) images of (b) template patterning with amorphous carbon, (c) metal lines after template removal, and (d) low-k gap-filling.

subsequent metallization, including barrier deposition, Cu plating and CMP, the sacrificial template is removed. In this way, a well-shaped Cu trench or via can be formed with continuous thin TaN/Ta barrier coated on the sidewall (Fig. 1(c)). Finally, a gap-filling porous low-k dielectric is spin-coated, followed by porogen removal, so as to encapsulate the metal gap structure (Fig. 1(d)). The proposed approach eliminates plasma-induced low-k damage, as well as barrier penetration and Cu CMP issues. If successful, inter-metal dielectric with pristine low-k properties is therefore achievable. However, the low-k gap-filling process requires a high temperature curing step in order to burn out the porogen, which may damage the Cu wires. As feature sizes shrink, the degradation of copper wires is becoming detrimental to the yield and dielectric performance. This paper aims to understand the impact of the gap-filling low-k deposition and cure on the metallization structures, Cu passivation and its relation to dielectric performance are studied.

For the gap-filling purposes, a liquid phase self-assembly low-k dielectric (SBA-2.2, from SBA Materials Inc.) is deposited by spin-coating. Driven by capillary forces, due to its low viscosity, the sol is capable to fill the narrow trench without void formation. A soft bake at 150 °C is then applied to evaporate the solvent. Finally, the expected dielectric properties are obtained upon the complete removal of the porogen. This is realized by a thermal anneal followed by a short ultraviolet (UV) cure. The FTIR spectra in Fig. 2(a)

show the removal of the porogen ($-\text{CH}_x$ groups in the range of 2800–2950 cm^{-1}) in the low-k films, as a function of time and conditions. As can be seen, a 400 °C thermal anneal burns out most of the porogen and increases the open porosity. In a previous study,²⁶ most of the porogen get easily desorbed within 30 minutes, leading to an open porosity around 32% and k -value = 2.53 at 100 kHz. However, the residue-free removal of porogen is rather difficult in this way, requiring treatments of several hours. A common solution is to add a short time UV cure in which the sample is exposed to broadband UV at high temperature.²⁷ Fig. 2(a) shows that further extraction of $-\text{CH}_x$ is facilitated by 120 s UV cure after 120 min thermal anneal. With this combination, the open porosity reaches 38% and the measured k -value get as low as 2.28 (100 kHz). It is also reported that UV curing can strengthen the matrix, leading to better mechanical properties.²⁸

The low-k sol is spun on patterned wafers using the same coating and curing conditions, as optimized on blanket substrates. SEM cross section images in Fig. 2 show the evolution of patterned Cu lines with the gap-filling process. The defect-free Cu lines are observed after template stripping by an H_2 based remote plasma, as shown in Fig. 2(b). However, after the low-k gap-filling and thermal anneal, void-like defects are observed in the metal trenches (Fig. 2(c)). The situation is even worse in case of an additional UV curing, i.e., Cu is extracted out of the trenches defined by the low-k and the diffusion barrier (Fig. 2(d)). The out-diffusion of Cu

FIG. 2. (a) FTIR spectra showing the removal of porogen in low-k films by thermal anneal (400 °C in N_2 for 2–120 min) and additional UV curing (385 °C in N_2 for 120 s). SEM cross section showing (b) metal lines only without gap-filling, (c) low-k curing with thermal anneal for 120 min, and (d) low-k curing with thermal anneal and additional UV curing.

FIG. 3. (a) AES Cu LMM spectra showing the surface composition of Cu with and without SiCN passivation: both samples are annealed at 400 °C for 120 min. TEM cross-sectional views of (b) gap-filling without SiCN passivation, cured by 400 °C anneal for 120 min. (c) Gap-filling with 3 nm SiCN passivation, low-k cured by 400 °C anneal for 120 min and additional UV curing for 120 s. The thickness of SiCN is measured on bare Si surface for calibration.

induces extensive voiding and subsequent failure in Cu meander lines. The failure mechanism is attributed to Cu migration, which is thermally activated.²⁹ The Cu migration is accelerated by the Rayleigh instability³⁰ and Cu oxidation.³¹ Oxidizing species, for instance oxygen leakage in atmosphere-controlled ovens and/or oxidizing by-products that are released from porogen decomposition, may increase dramatically the degree of damage.

Unlike their sidewalls, which are covered by a Ta/TaN diffusion barrier, the top part of the Cu lines is directly exposed to the low-k precursor. Therefore, it is necessary to passivate the open Cu surface in order to avoid oxidation. A non-conformal silicon carbon nitride (SiCN) cap layer is deposited over the Cu surface by the PECVD method. Auger electron spectroscopy (AES) is used to distinguish between metallic Cu, CuO and Cu₂O. Fig. 3(a) shows the Cu LMM spectra measured on blanket Cu surface after thermal annealing in N₂ at 400 °C. The extra peak at 916.5 eV indicates the presence of Cu₂O.³² With 3 nm SiCN passivation, there is no oxide observed, which indicates that such thin SiCN layer is able to stop the oxidation reaction on the Cu surface. Comparable tests can be performed on patterned wafers. Fig. 3(b) shows a TEM cross-sectional image of metal lines after low-k gap-filling without SiCN passivation. Voids are observed at the bottom of Cu line after thermal annealing. Copper migrates towards the top of the lines, where the diffusion barrier is absent. In contrast, Cu out-diffusion is not

observed in Fig. 3(c), since Cu has been passivated with SiCN prior to low-k gap-filling. The defect-free and well-shaped Cu lines are maintained after thermal annealing and additional UV curing, which is necessary to fully remove the porogen and porogen residues. It is worth mentioning that TEM images show light-colored area at the bottom of low-k, indicating the void formation in the trench. During the burn-out of solvent and porogen compositions, the low-k matrix shrinks and becomes solidified. As a result, the top of the trench is sealed by this non-flowable film, forming a confined space inside the trench. Along with further shrinkage at higher temperature, the stress build-up leads to the delamination of low-k from the trench bottom and sidewall. Further process optimization is therefore required to improve the gap-filling properties, for instance, surface modification to enhance the adhesion force, and multiple coating with thinner layer low-k precursors to reduce the stress build-up.

Functional circuits, in the form of Meander-Fork structures (Fig. 4(a)), are used to evaluate the electrical performance on the patterned wafers. Resistance is first measured on a 2 cm meander line directly after C template stripping. After gap-filling and thermal annealing at 400 °C, no yield is obtained for the wafer without SiCN passivation. The defects shown in Fig. 3(b) lead to an open resistance for the meander lines. On the contrary, there is no yield degradation for the wafers with 3 nm SiCN passivation. Since the SiCN film, deposited into the gap, has a k-value ~5.5, an increase in

FIG. 4. (a) Schematic of the Meander-Fork structure used for electrical measurement. The pitch is 90 nm, and the meander length is 2 cm. (b) Capacitance-resistance behavior of stand-alone Cu lines, with various SiCN thicknesses (3 and 6 nm) and with additional gap-fill low-k after annealing at 400 °C/120 min (fixed) with different UV cure times (30 and 120 s). (c) Cumulative probability plots of breakdown voltage for selected conditions.

structure's k_{eff} is expected. The SiCN has a similar composition as low- k dielectric; therefore, it is not distinguishable in the TEM inspection. The impact of SiCN layer on k_{eff} is studied by measuring the capacitance of metal lines prior to low- k gap-filling, as shown in Fig. 4(b). In comparison with the sample without passivation, 3 nm and 6 nm SiCN passivation increases the capacitance by 3% and 7%, respectively. The k_{eff} extracted by 2D simulation³³ is increased from 1.17 to 1.28 and 1.49. From that perspective, a minimal SiCN thickness and low conformity are preferred to minimize the deposition on the sidewall, provided it remains a good oxidation barrier.

After SiCN deposition, the low- k precursor is spin coated on the patterned wafers, followed by porogen removal by thermal annealing (400 °C, 120 min) and subsequent short UV cure. The resistance-capacitance (RC) curves for different passivation thicknesses and UV cure time are shown in Fig. 4(b). With 30 s UV curing, thicker SiCN passivation leads to higher capacitance; therefore, higher k_{eff} is expected. However, the impact of thicker SiCN disappears after 120 s UV cure, indicating the same k_{eff} as thin SiCN. Using a 2 dimension trench profile modeled from TEM image, the lowest value of $k_{\text{eff}} = 2.45$ is extracted for the wafer with 3 nm SiCN passivation and 120 s UV cure. TEM image is not available for the 6 nm passivated sample with 120 s UV cure; however, same k_{eff} can be expected by assuming a same trench profile, as shown in Fig. 3(c). Considering the contribution of the SiCN passivation layer, this value is close to the pristine value of 2.28 measured on the blanket wafers. It is also observed that the gap-filling wafers show the same range of meander resistance, as compared with the stand-alone metal lines. The Cu lines seem to be well protected even with 3 nm SiCN passivation.

The breakdown behavior is studied by the IV measurements on the same integration vehicle, as shown in Fig. 4(c). For wafers with 3 nm SiCN passivation, longer UV curing leads to degraded breakdown voltage. Together with the more scattered RC distribution, it is concluded that the protection by 3 nm SiCN is insufficient. Cu still oxidizes and diffuses into the porous low- k .³⁴ It leads to shallow energy levels in the bandgap of low- k dielectrics, facilitating the Poole-Frenkel type conduction.³⁵ The use of a thicker SiCN (6 nm) passivation allows to achieve the best RC and IV performances. In this case, the long UV cure significantly improves the breakdown voltage, linked to the UV-induced removal of graphitized-carbon residues.^{36,37} Assuming that the spacing is 35 nm, as shown in Fig. 3(c), the cumulative probability of the calculated breakdown field E_{BD} is in a range of 5.7–8.6 MeV/cm. This value is in agreement with the reported values measured on pristine low- k film,³⁸ allowing to conclude that this integration scheme does not bring any low- k degradation.

It is notable that gapfill low- k can be implemented in a dual-damascene process, with similar integration scheme as air-gap technology.³⁹ For this purpose, the overburden low- k layer should be planarized for the formation of upper metal layers. This could be achieved by direct low- k CMP using an oxide slurry. The previous studies^{40,41} indicated that the surfactants present in the slurry penetrate into the porous structure, leading to a dielectric degradation. A post-CMP

cleaning step is therefore required to remove the slurry residues and restore the k value to pristine level.

In summary, the impact of a low- k gap-filling process on metallization structure is investigated. The low- k curing requires high temperature annealing to enable the target porosity and dielectric constant. However, when applied directly to fully exposed copper, this induces oxidation/migration of the open Cu leading to voids, indicating that the Cu surface should be well protected to survive such high temperature curing process. A PECVD-type SiCN passivation layer is demonstrated to provide a sufficient protection against Cu oxide formation. The evaluation of the electrical performance indicates that, coupled to a 6 nm SiCN passivation, the gap-filling ultralow- k shows close to pristine dielectric constant and breakdown voltage. The study of copper passivation has also significance for post metallization polymer protection and late porogen removal, where high temperature cure is also adopted in order to burn-out sacrificial polymer or porogen residues. In this case, copper wires need to be selectively protected against degradation.

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