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A 16.07pJ/cycle 31MHz Fully Differential Transmission Gate Logic ARM Cortex M0 core in 40nm CMOS

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Abstract—This paper presents a 16.07pJ/cycle 31MHz ARM Cortex M0 core in 40nm CMOS. The system was designed using differential transmission gates in an extended standard cell flow, taking into account variability, speed, energy and scalability. Extensive measurements over a range of 25 dies show it achieves sub-20pJ/cycle operation in a 330-500mV 10-48MHz range and is fully functional down to 190mV. Compared to state-of-the-art, a 40x speed and 4.8x EDP improvement is reported at the MEP. With low variation (σ/μ) on the clock frequency (3.5% at the MEP) and energy consumption (18.2% at the MEP), it combines the low variability, high speed and low energy of full custom work with the ease and design time of standard cell design.

Index Terms—CMOS digital integrated circuits, nearthreshold logic, ultra-low voltage, transmission gate, variation resilience, minimum energy point, standard cell, microcontroller.

I. INTRODUCTION

Innovations in the field of mobile devices and IoT applications are driven by mobility and battery capacity. At the heart of these applications often lies a microcontroller: capable of handling a decent amount of workload, it is one of the most energy-consuming blocks in such applications. This has turned energy efficiency into a vital design parameter for such devices, and for digital design in general. Operating the microcontroller at ultra-low voltage can help to meet these strict energy requirements, yet this strategy is plagued by 3 conflicting design challenges: 1) ensuring reliable low voltage operation under the increased variability of advanced nanometer CMOS technologies; 2) maintaining an operating speed >10MHz, necessary to cover a wide range of applications, under ultra-low voltage operation; 3) integrating low voltage variability robust design into a standard cell design flow, avoiding the need for full custom design. Current state-of-the-art low-voltage 32-bit microcontrollers fail to combine these 3 aspects, either suffering from sub-MHz operating speed [1]–[3] or needing full custom circuit design to ensure variation resiliency [4].

The aim of this work is to use the efficiency of standard cell design with the ultra-low power, high speed performance and variation resilience of full custom work and combine it in a generic design flow, suitable for commercially available tools. The proposed design flow was applied to create a 32-bit microcontroller system with an industry-adopted and well-

Fig. 1. Proposed digital design flow with ultra-low voltage differential transmission gate standard cells.

established core: an ARM[®] Cortex[®]-M0. This resulted in a 4.8x better than state-of-the-art energy-delay performance at >10MHz clock frequencies with variation resilient logic.

Section II discusses the differential transmission gate library and design flow in more detail. Section III handles the implemented microcontroller architecture, while section IV discusses the measurement results. Section V draws a conclusion.

II. DIFFERENTIAL TRANSMISSION GATE DESIGN FLOW

The proposed differential design flow is shown in Fig. 1. It uses a custom standard cell library of 241 different cells. All ultra-low voltage cells consist of a combination of transmission gates (TG) and nMOS stacked inverters (Fig. 2). The combination of nMOS and pMOS in TGs significantly improves sensitivity to variability (Fig. 3). Differential signaling further improves variation resilience and allows simultaneous control of both devices. The structure of a TG allows to create any logic function with the same generic scheme and layout, making it easy to create a library consisting of lots of cells with different functionalities. The benefits of stacking and differential TG logic (see [4]) more than outweigh their increased design complexity. Signal degradation due to a lack

Fig. 2. Ultra-low voltage differential transmission gate standard cell library. For simplicity, the complementary parts of the TGs are omitted.

of regeneration in TGs restricts extensive cascading of multiple gates. Adding an nMOS stacked inverter after each cascade of TGs once again improves variability, restores the logic levels and allows unambiguous characterization of multiple TGs as a single standard cell. Up to 3 cascaded levels of logic functions are incorporated into a single cell. This way, complex cells like AO(I), OA(I) or even A222O(I) and A33O(I) become feasible. Every gate can be inverted without overhead. Flipflops with master/slave latches built out of transmission gates and inverters are used like in any other synchronous design.

The cell library is characterized in a differential way. Since differential synthesis is not commercially adopted, the differential cell library is converted to a single-ended library with worst-case timing/power information from the differential cells. This library is used to synthesize a pseudo single-ended design. During synthesis, the tool favors more complex cells (more cascaded transmission gates) when speed is not stringent and functionality allows it. This originates in the inherently higher TG/inverter-ratio that complex cells have, resulting in slower, more energy efficient operation at constant V_{dd} . After single-ended synthesis, the design is converted back into a differential netlist using an in-house netlist parser. Place & route, timing/power analysis and other back-end operations can be done with the actual differential library, enabling true differential sign-off. In a design with multiple voltage domains, the differential logic can be considered as a separate voltage domain where single-ended to differential conversion and vice versa is facilitated with dedicated level shifters. This allows seamless integration of the used differential transmission gate logic in any digital design flow with any kind of libraries or macro's. The full design flow can be executed using commercially available front-end and back-end tools, making it possible to design any generic system with the proposed design flow, and eliminates additional complexity or overhead for the designer due to the use of differential transmission gates.

Fig. 3. Variability analysis of stacked inverter and TG vs. normal CMOS logic propagation delay.

Fig. 4. Block diagram of the ARM Cortex M0 system. Chip micrograph of the 40nm implementation. Active area is 0.82mm².

III. MICROCONTROLLER ARCHITECTURE

The proposed microcontroller system (see Fig. 4) consists of an ARM[®] Cortex[®]-M0 core, 256KB of SRAM memory, a UART-interface, 8 GPIO ports and a test/debug interface. All peripherals are memory-mapped to the AHB bus. The system is realized using the ultra-low power design flow proposed in section II. The M0 core is a competitive architecture for ultra-low power applications and enables high processing power due to its 32-bit instruction set. It uses 3 pipeline stages and is equipped with 16 hardware interrupts. The SRAM can be used to emulate part ROM, part instruction and data memory and can be allocated at startup. The core and peripherals are located in separate ULV power domains. Both domains are fully composed out of transmission gates and inverters. SRAM macro's and other interfacing lie in a separate power domain, accessed through level shifters also facilitating single-ended to differential conversion and vice versa. All building blocks share a common clock domain: a clock mesh is used to alleviate the large delay variation on the clock tree, inherent to ultra-low voltage clock buffering [5]. To reduce the impact of hold time buffers on power consumption, special flip-flops

Fig. 5. Chip micrograph of the 40nm CMOS implementation. Active area is 0.82mm^2 .

Fig. 6. Boxplot of the measured maximum operating frequency as function of V_{dd} (25 dies).

were inserted on hold time violating paths. These flipflops have additional delay (transmission gates) in the datapath, reducing their hold time. Such flipflops prevent large-scale buffer insertion on short paths, which would compromise energy consumption. The final synthesized core consists of 10693 logic gates and 1332 flip-flops. 5.8% of total logic gates are 3 level TGs (A222O, A33OI, ...), 36.7% are 2 level TGs (AND4, AOI, FA, ...), the rest are 1 level TG deep (AND2, NAND2, IAND2, MUX2, ...). Post-route analysis showed a mean routing length difference of 5% accross nets longer than $50\mu\text{m}$ and of 20% across all differential nets, providing more than acceptable routing for differential signals without dedicated differential routing.

IV. MEASUREMENTS

The test chip (Fig. 5) was fabricated in a 40nm CMOS process and occupies a total area of 2.55mm^2 . Active area is limited to 0.82mm^2 , a large portion of which is occupied by the SRAM macro. Measurements on 25 dies from 2 different wafers at 20°C were done running the Dhrystone benchmark C-code. Fig. 6 shows the speed performance of the core.

Fig. 7. Boxplot of the M0 core measured energy/cycle and mean leakage power as function of V_{dd} (25 dies).

Fig. 8. Histogram of the measured minimal functional supply voltage and MEP supply voltage (25 dies). Pie chart of the total energy consumption at the MEP.

Mean clock frequencies reach from 0.8MHz at 190mV to 48.2MHz at 500mV , and vary only slightly over different samples ($\sigma/\mu = 3.5\%$ at the MEP). Fig. 7 shows the core energy/cycle, as well as its leakage power. At the lowest supplies, energy is leakage dominated (98% at 190mV), while at higher supplies active energy consumption becomes more important (57% leakage at 500mV). This trade-off leads to a MEP of $16.07\text{pJ}/\text{cycle}$ at 31MHz with a 440mV supply. The MEP is quite flat: sub- 20pJ performance is achieved in a $10 - 48\text{MHz}$ range for $330 - 500\text{mV}$. The very low $V_{dd,min}$ showcases the variation resilience of the applied standard cell library. The high speed/low energy shows the proposed strategy achieves great results does not compromise in the form of speed nor energy. Fig. 8 displays histograms of the $V_{dd,min}$ and $V_{dd,MEP}$ distribution across 25 samples, and shows the energy distribution of the different blocks and their leakage at the MEP.

Fig. 9 shows a contour plot of the measured core E/cycle as function of V_{dd} and $0 - 70^\circ\text{C}$ temperature range from a single die. It clearly shows the energy/cycle increases with rising temperature, mainly due to increased leakage. The MEP-line shows the MEP varies about 20% with temperature. A 30MHz -line is drawn to show the achievable clock frequency varies only slightly accross the provided temperature range. As shown in [6], an even lower temperature would reduce the

TABLE I
PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON.

	This work	[1] ISSCC'15	[2] ISSCC'15	[3] ISSCC'12
Technology	40nm CMOS	65nm CMOS	180nm CMOS	65nm CMOS
Core	ARM Cortex M0	ARM Cortex M0+	ARM Cortex M0+	32b RISC
Die Area (core)	0.16mm ²	0.16mm ²	1.1mm ²	0.36mm ²
Die Area (total)	2.55mm ²	3.76mm ²	2.04mm ²	2.7mm ²
Memory	256KB SRAM @ 0.6V	2KB ROM, 8KB ULV SRAM, 16KB SRAM	256B	0.6KB ULV SRAM, 32KB SRAM
# dies measured	25	160	28	37
V _{dd,MEP}	0.44V	0.35V	0.55V	0.325V
V _{dd,min}	0.19V	0.25V	0.16V	0.20V
Speed @ MEP	31.2MHz	750kHz	7Hz	133kHz
Speed @ V _{dd,min}	0.8MHz	27kHz	16Hz	10kHz
Core E/cycle @ MEP	16.07pJ	/	/	9.94pJ
Core E/cycle @ V _{dd,min}	60.55pJ			20pJ*
Total E/cycle @ MEP	100.34pJ	11.7pJ	92.04pJ	/
Total E/cycle @ V _{dd,min}	2551pJ	32pJ	2275pJ*	
	CPU, Periph, 256KB	CPU, 4KB SRAM	CPU, 256B	
EDP [pJ/MHz]	0.5 (core) 3.2 (total)	/	/	74.4 (core) /

* = estimated

Fig. 9. Contour plot of measured core E/cycle as function of V_{dd} and temperature.

speed of any ultra-low voltage design significantly.

A detailed comparison between this work and 3 other recently published 32-bit microcontrollers [1]–[3] is shown in Table I. The differential nature of our library clearly does not compromise core area. At the same time, this work outperforms all designs more than 40x in speed at the MEP. Even though the M0+ architecture in [1], [2] is more optimized for low energy, and [3] has a severely reduced instruction set, our work still reaches comparable core energy/cycle at this higher speed. Combining speed and total energy consumption in the energy delay product (EDP), it outperforms other works by at least 4.8x despite the far (at least 64x) larger SRAM array.

V. CONCLUSION

This work presents an ARM Cortex M0 microcontroller system in 40nm CMOS. It was designed using differential

transmission gates, integrated in an extended standard cell design flow. The proposed design flow succeeds in creating an industry-proven microcontroller with commercially available tools and minimal design effort. The microcontroller system achieves significantly better than state-of-the-art speed performance, well in the MHz range, combined with low variability and very low energy consumption (sub-20pJ/cycle) in a large voltage range. It merges the fast design time from standard cell design with the variation-tolerance, speed and energy consumption achieved in full custom designs resulting in a state-of-the-art EDP, at least 4.8x better than similar referenced designs.

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REFERENCES

- [1] J. Myers, *et al.*, “An 80nW retention 11.7pJ/cycle active subthreshold ARM Cortex-M0+ subsystem in 65nm CMOS for WSN applications,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2015 *IEEE International*, Feb 2015, pp. 144–145.
- [2] W. Lim, I. Lee, D. Sylvester, and D. Blaauw, “Batteryless Sub-nW Cortex-M0+ processor with dynamic leakage-suppression logic,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2015 *IEEE International*, Feb 2015, pp. 146–147.
- [3] S. Luetkemeier, T. Jungeblut, M. Porrmann, and U. Rueckert, “A 200mV 32b subthreshold processor with adaptive supply voltage control,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012 *IEEE International*, Feb 2012, pp. 484–486.
- [4] N. Reynders and W. Dehaene, “A 210mV 5MHz variation-resilient near-threshold JPEG encoder in 40nm CMOS,” in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014 *IEEE International*, Feb 2014, pp. 456–457.
- [5] M. Seok, D. Blaauw, and D. Sylvester, “Clock network design for ultra-low power applications,” in *Low-Power Electronics and Design (ISLPED)*, 2010 *ACM/IEEE International Symposium on*, Aug 2010, pp. 271–276.
- [6] D. Bol, C. Hocquet, D. Flandre, and J. D. Legat, “The detrimental impact of negative Celsius temperature on ultra-low-voltage CMOS logic,” in *ESSIRC, 2010 Proceedings of the*, Sept 2010, pp. 522–525.