

Reliability of Au-Free AlGaIn/GaN-on-Silicon Schottky Barrier Diodes Under ON-State Stress

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Abstract—In this paper, we report the results of an experimental analysis of the degradation induced by ON-state stress in GaN-based Schottky barrier diodes (SBDs). When a high stress current is applied to the device, turn-ON voltage (V_{TON}), forward voltage (V_F), and ON-resistance (R_{ON}) are affected by charge carrier trapping occurring at the AlGaIn surface close to the anode corners and/or into the AlGaIn barrier layer. We have investigated the degradation of SBDs under different stress conditions, analyzing the influence of temperature and voltage, investigating the activation energy of the traps, and hence the trapping mechanisms. In addition, thanks to this approach, the device lifetime has been evaluated, proving good device reliability.

Index Terms—AlGaIn/GaN Schottky diode, gated edge termination (GET), lifetime, ON-resistance (R_{ON}), ON-state stress, reliability, trapping/detrapping mechanisms, turn-ON voltage (V_{TON}).

I. INTRODUCTION

THANKS to the intrinsic properties of the adopted materials, GaN-based power devices represent today one of the best candidates for switching power applications [1]–[4]. In particular, they feature a higher breakdown voltage and a lower ON-resistance with respect to silicon-based devices, because of the wider bandgap of the III-N compounds and the formation of the 2-D electron gases (2-DEG) at the AlGaIn/GaN heterointerface, due to spontaneous and piezoelectric polarization [5], [6].

However, high performance is not enough to dominate the power electronic market, as a low fabrication cost and a high level of reliability under heavy-duty operation must be guaranteed. A low-cost fabrication approach relies on the epitaxial growth of GaN over large diameter silicon (Si) substrates, by means of metal-organic chemical vapor deposition (MOCVD) [7]–[10]. Furthermore, this technology,

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being CMOS-compatible, can take advantage of a widely available and mature technological infrastructure.

The reliability of GaN-based power devices is mainly limited by trapping and detrapping phenomena occurring when transistors or diodes have to withstand large electric fields or current density during OFF- and ON-state operation mode, respectively.

Although many papers about trapping mechanisms in GaN high electron mobility transistors (HEMTs) have been published [11]–[18], limited work has been done on the trapping effects affecting GaN-based Schottky barrier diode (SBD) reliability [19], especially regarding the degradation under ON-state stress.

Terano *et al.* [20] investigated the relationship between the 2-DEG density and the reverse leakage current in AlGaIn/GaN SBDs, asserting that a leakage reduction of several orders of magnitude is achieved by slightly reducing the 2-DEG density.

In [21], the temperature dependence of the leakage current mechanisms affecting Schottky contacts, fabricated on AlGaIn/GaN HFET, was investigated. The authors found out that at room temperature, the reverse leakage is dominated by carrier transport via conductive dislocations, whereas at higher temperatures, the Frenkel–Poole emission represents the main source of the reverse leakage.

The degradation mechanism and the influence of the anode recess on the electrical properties of the SBDs were analyzed in [22], highlighting that the anode recess process activates traps with relatively short capture and escape times, hence leading to a higher degradation of the I – V characteristics in short reverse stress experiments.

Finally, Hu *et al.* [23] by combining experimental and simulation results have proposed the physical origin of the current collapse and ON-resistance degradation in Au-free AlGaIn/GaN SBDs occurring when a negative bias is applied on the anode. In particular, they have linked the gradual increase in the R_{ON} to those traps featuring an energy of 1 eV below the conduction band and located at $\text{Si}_3\text{N}_4/\text{AlGaIn}$ interface. On the other hand, a sudden collapse of the ON-current has been related to the traps having an energy of 0.5 eV positioned around the Schottky contact corner and playing a role only for the negative bias above a critical value (-175 V in that case).

In this paper, we extensively analyze the degradation mechanisms occurring when a large direct stress current (ON-state) is forced through Au-free AlGaIn/GaN SBDs.

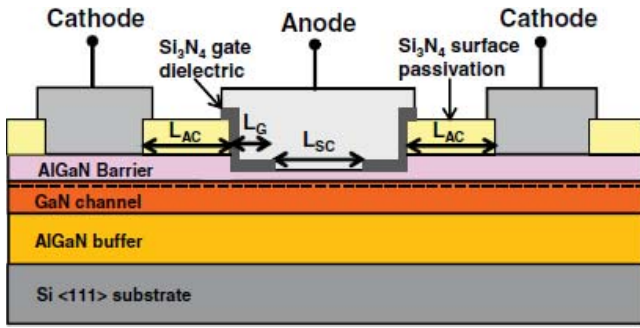


Fig. 1. Schematic of the AlGaIn/GaN-on-Si GET-SBDs (not in scale) [7]. The AlN spacer between the AlGaIn barrier and the GaN channel and the SiN cap between the AlGaIn barrier and the Si₃N₄ surface passivation are not shown.

We experimentally investigate the impact of the stress on the main figures of merit, such as the turn-ON voltage (V_{TON}), the forward voltage (V_F), and the ON-resistance (R_{ON}). Stress analyses at different voltages and temperatures are performed and the recovery phase, happening after removing the stress, is monitored. Thanks to this approach, it is possible to ascribe the V_{TON} and the R_{ON} degradation to different defects. In particular, the turn-ON voltage is affected by defects located under the anode contact into the AlGaIn barrier. Moreover, the SBD lifetime was evaluated under ON-state operation mode proving a good device reliability.

This paper is organized as follows. In Section II, the devices under test and the measurement approach are described. In Section III, the experimental results are reported and discussed. Finally, in Section IV, we summarize the main achievements of the work.

II. DEVICE STRUCTURE AND MEASUREMENT TECHNIQUE

Gated edge termination-SBDs (GET-SBDs) (Fig. 1) fabricated on silicon wafers by IMEC [7] with a nominal forward voltage (V_F) of ≈ 1.25 V are considered in this study. The epitaxial structure is grown on an 8-in (111) silicon substrate by means of MOCVD and features a stack of: 200-nm-thick AlN nucleation layer (on top of the Si substrate), followed by a 2800-nm-thick AlGaIn buffer, 150-nm-thick GaN channel, 0.5-nm-thick AlN spacer, 10-nm-thick Al₂₅Ga₇₅N barrier, and 5-nm-thick SiN cap. Then the whole epitaxial stack is passivated with 140 nm of Si₃N₄ by rapid thermal chemical vapor deposition. Prior to the deposition of metal stack, the Si₃N₄ passivation layer is removed at the anode region by SF₆ dry etch and the AlGaIn barrier is recessed by about 5 nm through atomic layer etching.

It is worth noting that with the anode recess, the forward characteristic is improved by reducing the V_{TON} and the V_F with respect to the case of nonrecessed devices. Moreover, the GET-SBD functionality not only as a stand-alone diode but also in combination with MISHEMT process flow was proved [7].

A further 25-nm-thick Si₃N₄ deposition with a subsequent etching in the central region of the anode (with length L_{SC}) is performed in order to make the GETs (Fig. 1). Finally, Au-free anode and cathode contacts are realized. In particular,

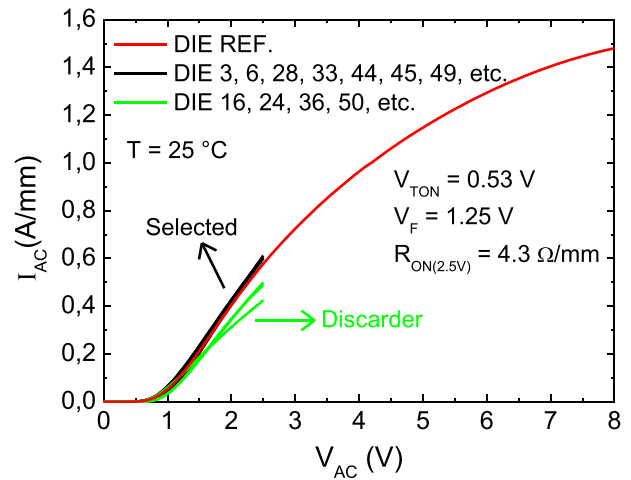


Fig. 2. Forward characteristics of the GET-SBDs. Due to the variability of the process along the wafer, a screening of devices featuring similar I - V characteristics has been performed.

an Au-free metal stack, consisting of 20-nm TiN/20-nm Ti/250-nm Al/20-nm Ti/60-nm TiN, is deposited and etched to define the diode anode. A more detailed description of the diode process is reported in [7].

The experimentally tested devices feature a central anode finger with two independently addressable cathode contacts. By referring to Fig. 1, the Schottky diode length (L_{SC}) is 9 μm , the edge termination length (L_G) is 1.5 μm , the anode to cathode spacing (L_{AC}) is 5 μm , and the finger width is 100 μm .

The reliability study has been carried out by adopting the conventional measure/stress/measure (MSM) technique. During the stress phase, a constant voltage (V_{AC_S}) was applied on the anode contact while short-circuiting the two cathodes with the substrate. The stress was periodically interrupted in order to monitor V_{TON} , V_F , and R_{ON} shift by measuring a full I - V characteristic from 0 to 2.5 V. The turn-ON and forward voltages were extrapolated at the current density of 1 and 100 mA/mm, respectively, whereas the R_{ON} was evaluated by considering the slope in linear region between 1.5 and 2.5 V. At the end of the stress phase, the reverse leakage current was evaluated by sweeping V_{AC} between 0 and -6 V. Finally, the recovery was monitored by applying 0 V (V_{AC_R}) and periodically analyzing V_{TON} , V_F , and R_{ON} .

It is worth noting that, in order to evaluate the degradation (and recovery) under different stress (and recovery) conditions, several devices (22) featuring a similar fresh I - V characteristic (Fig. 2) have been selected. Moreover, for each stress/recovery analysis, different devices have been initially considered in order to verify the statistical dispersion of the measurements.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Introduction to Different Trapping/Detrapping Mechanisms Causing V_{TON} Degradation

The turn-ON voltage shift occurring during the ON-state stress and recovery is shown in Fig. 3(a). Four devices,

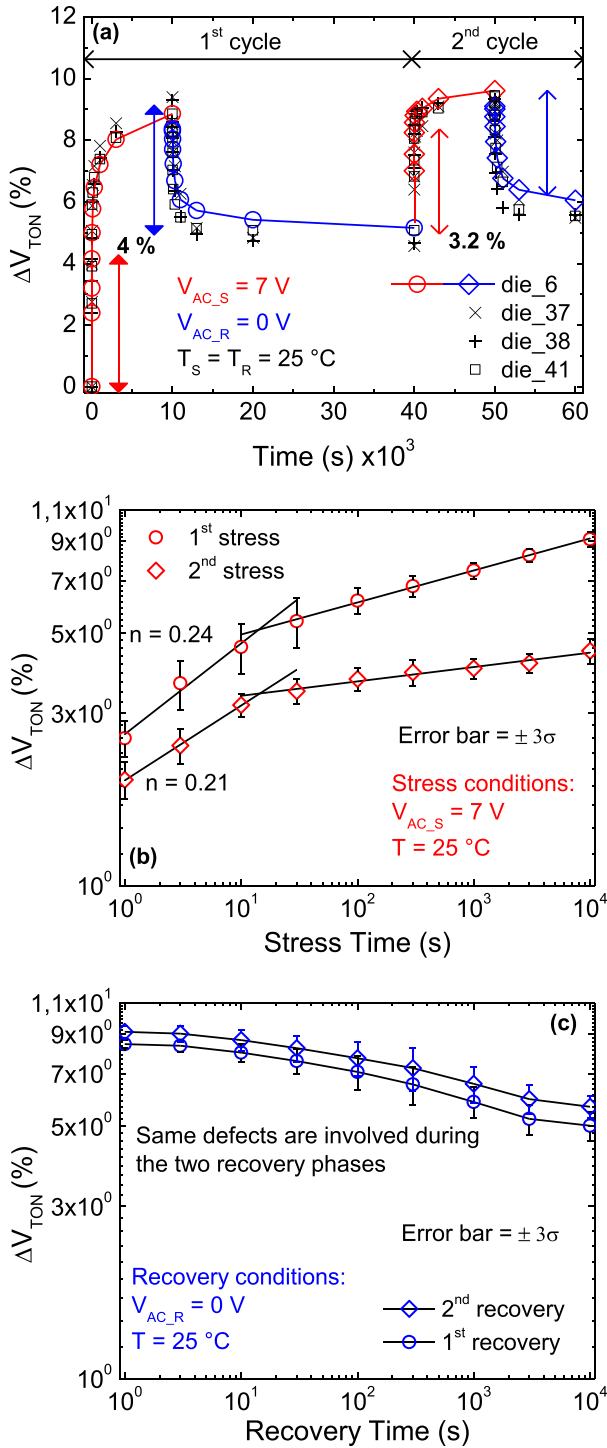


Fig. 3. Turn-ON voltage shift during two cycles of ON-state stress and recovery for four devices positioned in different dies. V_{TON} was extracted at a current density of 1 mA/mm and the following conditions were considered: $V_{AC,S} = 7$ V (during stress), $V_{AC,R} = 0$ V (during recovery), and $T = 25$ °C (both phases). (a) Four samples show similar V_{TON} degradation and recovery. (b) Dual slope shown in the stress phase is probably attributed to two different mechanisms, build-up of charges and new trap creation, precisely. ΔV_{TON} degradation related to the second cycle is calculated with respect to the end of the first recovery phase. (c) Two recovery phases show a similar dynamics, meaning that the same defects are involved in the detrapping mechanism.

positioned in different dies and selected as shown in Fig. 2, have been characterized under the same stress and recovery conditions in order to prove a good reproducibility of the

V_{TON} degradation induced by trapping/detrapping mechanisms. During the stress phase, electrons are trapped in the region under the anode (Schottky junction) causing an increase in the Schottky barrier height, and hence in V_{TON} . Then, as the stress is removed (recovery phase), some defects are detrapped and a partial V_{TON} recovery occurs.

A second cycle of stress and recovery has been performed in order to understand which kind of trapping/detrapping mechanism occurs, by comparing the two stress and recovery dynamics.

It is worth noting that Fig. 3(b) and (c) shows the average of four samples [reported in Fig. 3(a)]. In order to account for the statistics dispersion, the error bars were calculated as $\pm 3\sigma$ (standard deviation).

From the evolution of V_{TON} reported in Fig. 3(b), it is possible to distinguish two degradation phases characterized by different power slopes that may be associated with two different trapping mechanisms. For stress time up to 20 s, the build-up of charge in pre-existing defects appears to be the dominant mechanism causing the degradation, whereas afterwards, as discussed in Section III-C, the creation of new defects becomes the dominant one.

Based on Fig. 3(a)–(c), it is possible to observe the following.

- 1) In both degradation cycles [Fig. 3(a)], the relative degradation occurring during the first 10 s of stress is comparable to the amount of the corresponding subsequent recovery ($\approx 4\%$ and $\approx 3.2\%$ for the first and second cycles, respectively).
- 2) For short stress times (≈ 10 s), the V_{TON} degradation features the same dynamics (same slope) in both cycles [Fig. 3(b)].
- 3) The two recovery phases exhibit the same trend [Fig. 3(c)].

In conclusion, by considering together these aspects, we can conclude that the shift of the turn-ON voltage in the first 10 s of stress and during the whole recovery phase, in both cycles, may be mainly ascribed to the trapping and detrapping of the same pre-existing defects.

In addition, these results suggest that pre-existing defects are the source of the recoverable degradation component, whereas the new created defects cause a quasi-permanent or slowly recoverable component.

Thanks to the adopted MSM technique, the impact of degradation on reverse leakage during ON-state stress and recovery has been analyzed (Fig. 4).

A slight nonrecoverable reduction of the reverse leakage after the ON-state stress, due to electrons trapping, is shown in Fig. 4. By trapping negative charge in the AlGaIn barrier layer or at $\text{Si}_3\text{N}_4/\text{AlGaIn}$ interface, the 2-DEG density in the channel is reduced; therefore, as observed in [19], a reverse leakage reduction may occur.

B. Voltage Dependence

It is worth noting that from here on, the reverse leakage measurement has not been performed in order to avoid a possible alteration of the defects state due to negative

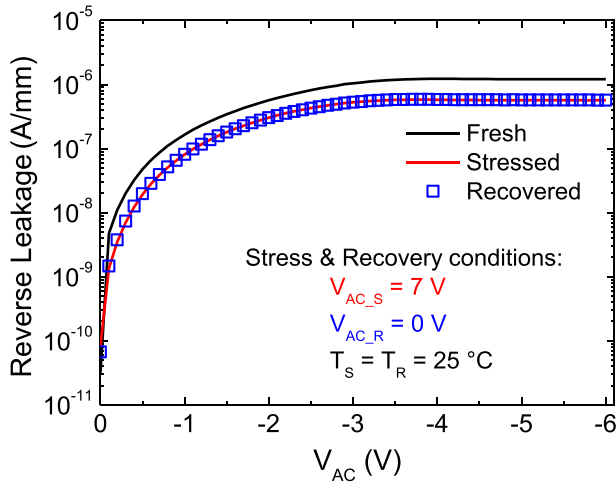


Fig. 4. Reverse leakage measured in fresh condition after 10^4 s of stress and after 3×10^4 s of recovery. The electrons trapping during the ON-state stress lead to a slight reduction of the reverse leakage. This behavior is also verified at high temperatures (not shown).

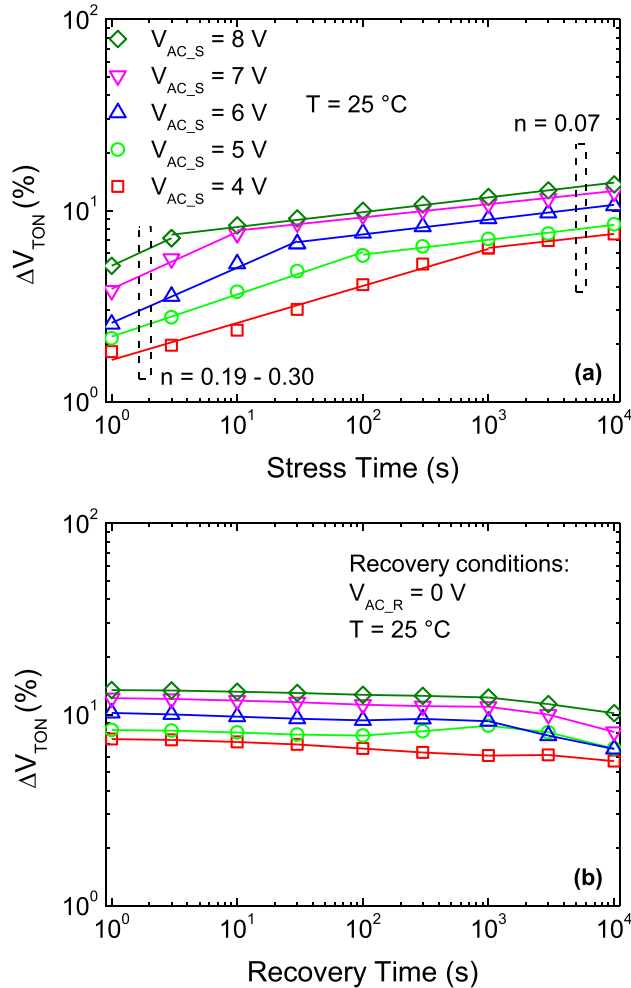


Fig. 5. (a) V_{TON} shift for different ON-state stress conditions. (b) Corresponding recovery phase happening after the end of the stress. By stressing at higher voltage, the pre-existing traps filling is faster. As a result, (a) change in the power slope occurs for shorter stress time.

voltage sweep. Moreover, given the limited statistical dispersion reported in Fig. 2, from here on a single device is used for each stress/recovery condition.

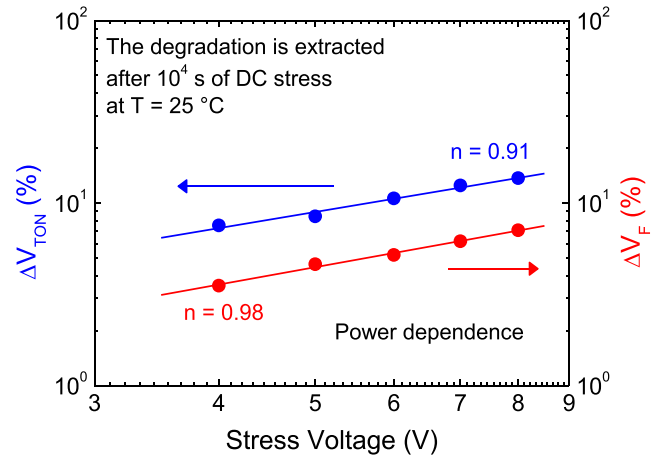


Fig. 6. Turn-ON and forward voltage degradation versus stress voltage. A power dependence is observed for both parameters.

The V_{TON} degradations for different stress voltages and the corresponding recovery phase are reported in Fig. 5(a) and (b), respectively. As already discussed with reference to Fig. 3(b), two degradation phases are evident, and the first one may be attributed to pre-existing traps filling. Indeed, by increasing the stress voltage, the end of the first degradation phase (i.e., the change of the power slope) occurs for shorter stress time. This is expected when a fixed number of traps, with a fixed energy level, are present in the fresh device. By applying a higher stress bias, a faster charge trapping occurs, leading to a larger degradation and to a faster filling of the available traps.

Independently of the amount of degradation at the end of the stress, the recovery dynamics is slow, meaning that the traps feature a long detrapping time constant.

Finally, as it is possible to observe in Fig. 6, the voltage dependence of both turn-ON and forward voltage degradations can be modeled by a power law.

The ON-resistance shifts (ΔR_{ON}) during stress and recovery phase are reported in Fig. 7(a) and (b), respectively. The evolution of ΔR_{ON} and its dependence on stress bias are much more complex, and chaotic, compared with the case of turn-ON voltage.

By moving the stress bias from 4 to 5 V, a larger R_{ON} degradation occurs; a further increase of the stress voltage, hence going from $V_{AC,S} = 5$ to 8 V, produces a higher degradation for short stress time (<10 s) and a lower degradation for longer stress times (>100 s). In addition, by observing Fig. 8, the current monitored during the stress, in the case of $V_{AC,S} = 8$ V, shows an increase after an initial decrease (≈ 3 s), which is in good correlation with the observed R_{ON} degradation. As soon as the stress is removed for R_{ON} measurement (10, 30, 100 s, etc.), a recovery mechanism, opposite to that occurred in the case of $V_{AC,S} = 5$ V, occurs. We think that the combined effects of higher stress voltages, hence higher stress currents, and higher temperatures due to self-heating effect can enable different trapping/detrapping mechanisms.

Moreover, it is worth noting that a certain variability of this phenomenon affecting the R_{ON} , probably linked to variability

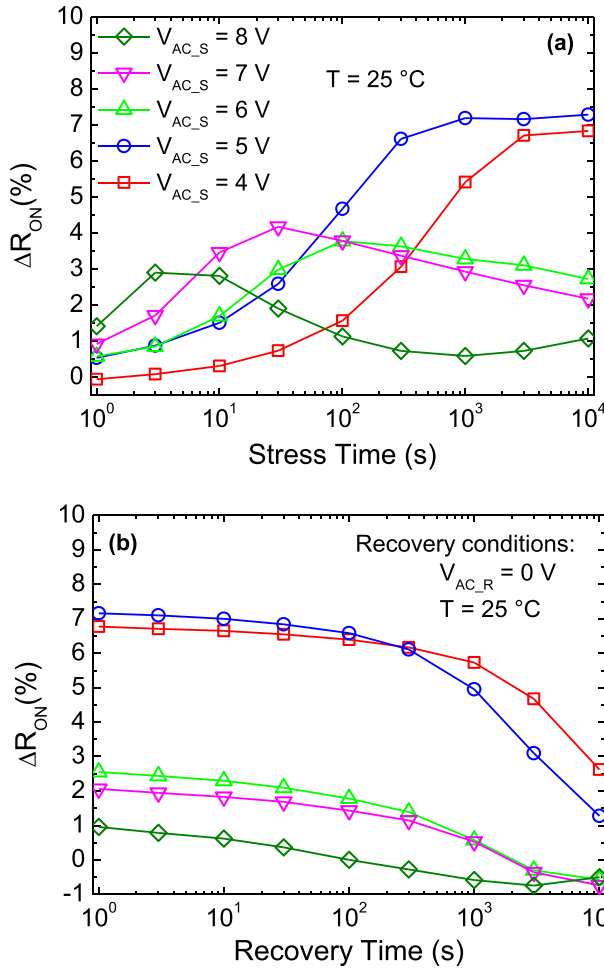


Fig. 7. R_{ON} shift, due to (a) ON-state stress and (b) recovery, for different stress conditions. For stress voltages higher than 5 V, an additional trapping/detrapping mechanism is involved. As a result, lower R_{ON} degradations are shown (a). Unlike V_{TON} [Fig. 5(b)], R_{ON} degradation seems to be quasi-totally recoverable (b) in the considered recovery time.

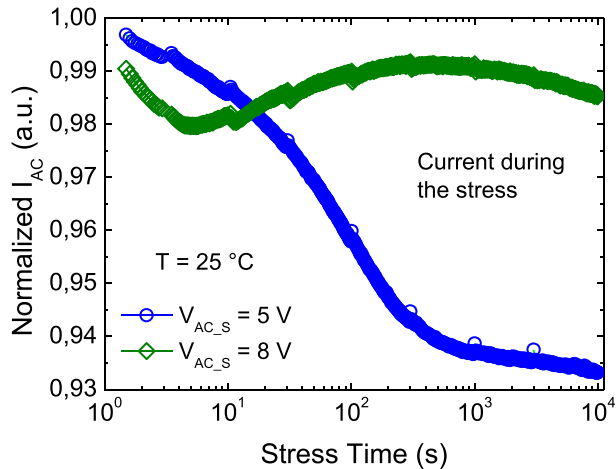


Fig. 8. Currents monitored during the ON-state stress. In the case of $V_{AC,S} = 8\text{ V}$, an additional trapping/detrapping mechanism is involved causing an increase in the current during the stress. Further analysis is necessary for understanding the mechanisms underneath this phenomenon.

of the process along the wafer, has been observed. By stressing devices with the same stress conditions but positioned in different dies, the R_{ON} decrease during the stress phase can occur for shorter or longer stress time.

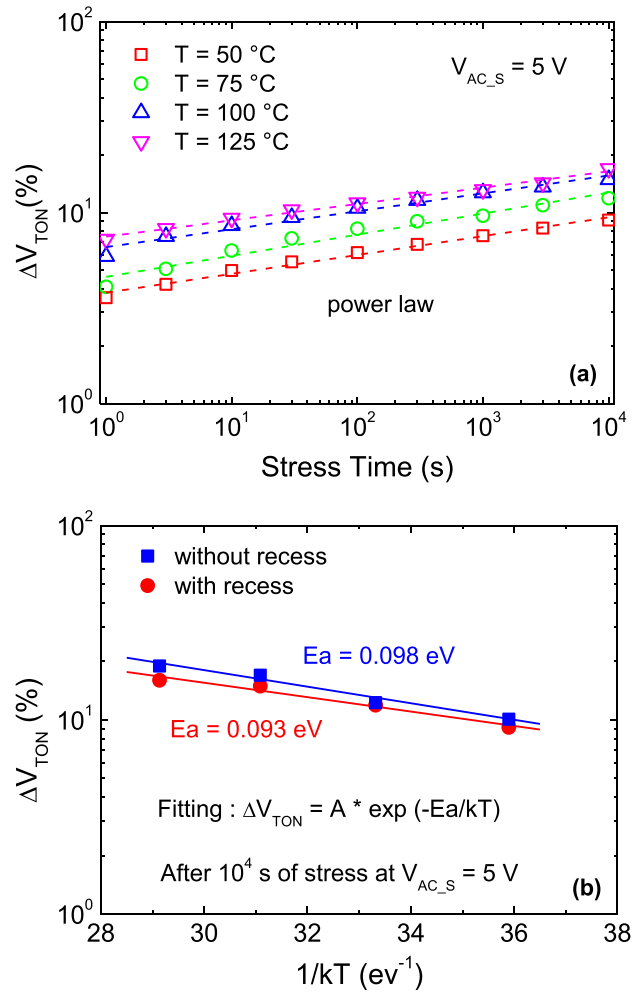


Fig. 9. V_{TON} shift for (a) different temperatures stress and (b) Arrhenius plot. The V_{TON} shift has been extracted at the end of the stress (10^4 s) in devices with (circle) and without (square) anode recess. By considering the database of the deep levels in GaN- and AlGaIn-based devices [24], the activation energy of $\approx 0.09\text{ eV}$ is linked to the nitrogen vacancies.

In conclusion, further analyses are necessary for understanding the physical mechanisms behind the R_{ON} degradation and its variability.

Instead, by focusing on the recovery phase [Fig. 7(b)], unlike the case of turn-ON voltage, after $\approx 100\text{ s}$, a faster detrapping mechanism occurs and a quasi-total recovery is reached. Therefore, R_{ON} and V_{TON} degradations may be related to different defects positioned in different regions.

C. Temperature Dependence

The role of temperature on the ON-state degradation has been investigated. Fig. 9(a) shows the shift of the turn-ON voltage as a function of temperature.

It can be noticed that by stressing at temperatures higher than $25\text{ }^\circ\text{C}$, the dual slope of the V_{TON} degradation is not clearly observed [Fig. 9(a)], contrary to the case of room temperature [Fig. 5(a)]. As a matter of fact, by increasing the temperature, the process of filling of pre-existing traps, according to our results, is shorter than 1 s. Moreover, curves at different temperatures feature a similar slope (0.09).

By considering the Arrhenius plot of Fig. 9(b), an effective activation energy of 0.093 eV has been extracted from V_{TON} degradation. By considering the database of the deep levels in GaN- and AlGaN-based devices (see [24]), traps having an activation energy of 0.09 eV can be ascribed to the nitrogen vacancies. A similar value has been found by Bisi *et al.* [24] in AlGaN/GaN HEMT, by means of the current transient investigation at several temperature levels, linking these traps to the AlGaN barrier in the region under the gate.

In our diodes, the V_{TON} shift under forward stress is ascribed to an increase in Schottky barrier height and features a similar activation energy (0.093 eV). Hence, we can assume that traps, responsible for V_{TON} degradation, are located in the AlGaN barrier layer under the anode metal.

An activation energy of 0.093 eV suggests that the traps are fairly shallow, and hence they should feature a short trapping/detrapping time constant. On the contrary, in our case, the activation energy is extracted after 10^4 s of stress. This observation confirms that the creation of new defects is the responsible mechanism causing the permanent or slowly recoverable degradation.

In order to understand which is the cause of the nitrogen vacancies, a study of the temperature dependence of V_{TON} degradation has also been performed on devices without anode recess [Fig. 9(b)]. By considering the Arrhenius plot of Fig. 9(b), we can observe the following.

- 1) Devices without recess show a comparable (or slightly higher) V_{TON} degradation.
- 2) The V_{TON} shift in both typologies of device is induced by the same kind of traps because of the similar activation energies.

As a result, nitrogen vacancies are not caused by the recess process but are probably linked to the crystal quality of the AlGaN barrier layer. By avoiding the anode recess, the AlGaN barrier under the anode metal is thicker; as a consequence, a larger number of bulk defects are present, leading to a slightly higher V_{TON} degradation.

Finally, the study of the R_{ON} degradation for different temperatures is shown in Fig. 10(a). It seems from Fig. 10 that no R_{ON} degradation increase is observed for higher temperatures. On the other hand, from Fig. 10(b), it is possible to observe a decrease in the ON-current during the stress and a huge recovery happening during each measurement phase. It is well known that by increasing the temperature, the detrapping mechanism becomes faster, and hence the detrapping time constant could be lower than the delay time introduced by measurement setup. As a result, the ON-resistance degrades during the stress but it is not possible to catch the real degradation with this technique.

However, it is again proved that R_{ON} and V_{TON} degradations are due to different defects.

D. Device Lifetime Estimation

The analysis of the ON-state degradation at different stress bias, by means of constant voltage-stress method, allowed us to estimate the lifetime of the AlGaN/GaN-on-Si GET-SBDs at the temperatures of 25 °C and 150 °C,

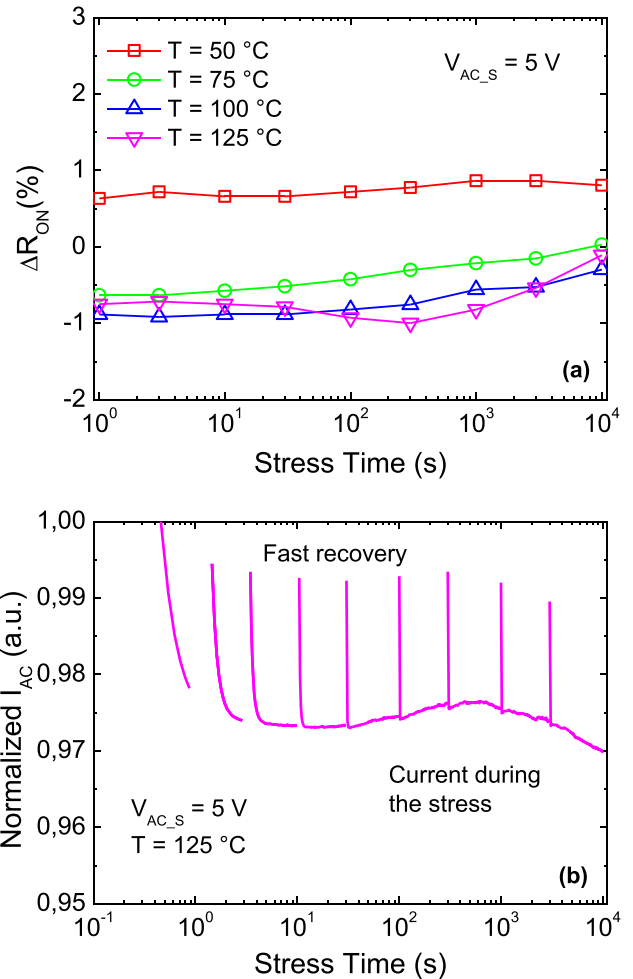


Fig. 10. (a) R_{ON} degradation at different temperatures. By increasing the temperature, as the stress voltage is removed in order to perform I - V characteristics, (b) a fast recovery of the ON-current is observed. As a result, (a) no R_{ON} degradation is observed.

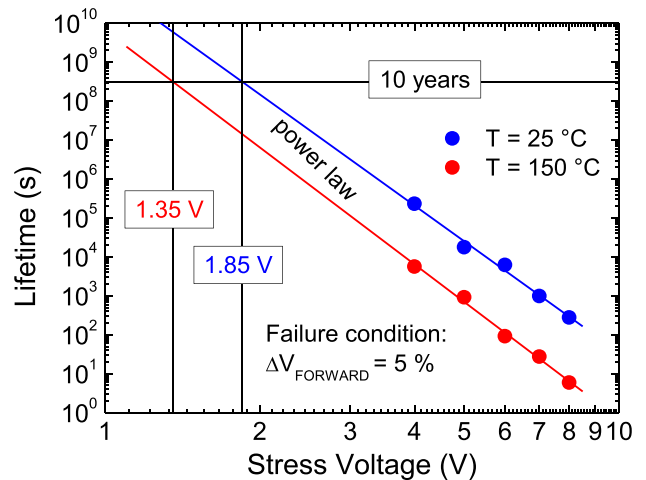


Fig. 11. Lifetime extrapolation. The failure criterion is considered as the 5% of the forward voltage shift in ten years at the temperature of 25 °C and 150 °C. In the worst case (150 °C), the maximum applicable voltage is higher than nominal operating voltage ($V_F \approx 1.25$ V).

as reported in Fig. 11. The lifetime has been extrapolated by considering the forward voltage degradation since it takes into account both V_{TON} and R_{ON} degradations by the

following relationship:

$$\Delta V_F = \Delta V_{TON} + (\Delta V_{ON} * I_{AC}). \quad (1)$$

By adopting as a failure criterion a shift of 5% in ten years, the maximum applicable voltages at temperatures of 25 °C and 150 °C are 1.85 and 1.35 V, respectively. For the considered samples, the nominal operating voltage in forward condition is 1.25 V, corresponding to a nominal forward current of 100 mA/mm. Therefore, under these assumptions, we expect a lifetime higher than ten years. It is worth noting that SBDs in actual application are forced to work with fixed ON-current, rather than with fixed V_F (as reported in Fig. 11). However, the change of the ON-current, during the stress (see Fig. 8) at fixed voltage, is relatively low.

IV. CONCLUSION

In this work, we have investigated the degradation of the turn-ON voltage, forward voltage, and ON-resistance induced by ON-stress in AlGaN/GaN-on-Si GET-SBDs.

By performing stress and recovery phases at different voltages and temperatures, we found out that R_{ON} and V_{TON} degradations are triggered by different defects.

Traps causing R_{ON} degradation are quickly and quasi-totally recoverable in the monitored time window, especially at higher temperatures.

On the other hand, defects triggering V_{TON} degradation are located into the AlGaN barrier layer under the Schottky contact, slowly recoverable, and due to nitrogen vacancies because of 0.093 eV of activation energy. In order to further improve the reliability of the devices, therefore, defectiveness on AlGaN barrier should be reduced.

Moreover, we have shown a power voltage dependence of the V_{TON} degradation, pointing out that the first phase of the stress and the quasi-total recovery phase (noticeable at 25 °C) are dominated by charging and discharging of the preexisting defects, respectively.

Finally, GaN-based SBDs have shown a good reliability to ON-state stress. In fact, by using them at the nominal operating voltage ($V_F \approx 1.25$ V) and at a temperature of 150 °C, the lifetime exceeds ten years by considering the 5% of forward voltage shift.

REFERENCES

- [1] J. Everts, J. Das, J. Van dan Keybus, M. Germain, and J. Driesen, "GaN-based power transistors for future power electronic converters," in *Proc. IEEE Benelux Young Res. Symp.*, Mar. 2010.
- [2] C. Abi Abboud, M. Chahine, C. Moussa, H. Y. Kanaan, and E. A. Rachid, "Modern power switches: The gallium nitride (GaN) technology," in *Proc. IEEE Conf. Ind. Electron. Appl. (ICIEA)*, Hangzhou, China, Jun. 2014, pp. 2203–2208.
- [3] M. A. Briere, "The power electronics market and the status of GaN based power devices," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Waikoloa, HI, USA, Oct. 2011, pp. 1–4.
- [4] T. Ueda, "Recent advances and future prospects on GaN-based power devices," in *Proc. IEEE Int. Power Electron. Conf.*, Hiroshima, Japan, May 2014, pp. 2075–2078.
- [5] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaIn/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, 1999.
- [6] O. Ambacher *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaIn/GaN heterostructures," *J. Appl. Phys.*, vol. 87, no. 1, pp. 334–344, 2000.

- [7] S. Lenci *et al.*, "Au-free AlGaIn/GaN power diode on 8-in Si substrate with gated edge termination," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1035–1037, Aug. 2013.
- [8] S. Lenci, J. Hu, M. Van Hove, N. Ronchi, and S. Decoutere, "Improvement of the dynamic characteristics of Au-free AlGaIn/GaN Schottky diodes on 200 mm Si wafers by surface treatments," in *Proc. IEEE Int. Symp. Power Semiconductor Devices IC's*, Waikoloa, HI, USA, Jun. 2014, pp. 265–268.
- [9] H. Ishikawa, G.-Y. Zhao, N. Nakada, T. Egawa, T. Jimbo, and M. Umeno, "GaN on Si substrate with AlGaIn/AlN intermediate layer," *Jpn. J. Appl. Phys.*, vol. 38, no. 5A, pp. L492–L494, 1999.
- [10] J. W. Chung, K. Ryu, B. Lu, and T. Palacios, "GaN-on-Si technology, a new approach for advanced devices in energy and communications," in *Proc. IEEE Eur. Solid-State Device Res. Conf. (ESSDERC)*, Seville, Spain, Sep. 2010, pp. 52–56.
- [11] M. Meneghini *et al.*, "OFF-state degradation of AlGaIn/GaN power HEMTs: Experimental demonstration of time-dependent drain-source breakdown," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 1987–1992, Jun. 2014.
- [12] M. Meneghini *et al.*, "Trapping and reliability assessment in D-mode GaN-based MIS-HEMTs for power applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2199–2207, May 2014.
- [13] D. Marcon *et al.*, "Reliability of AlGaIn/GaN HEMTs: Permanent leakage current increase and output current drop," in *Proc. IEEE Int. Symp. Phys. Failure Integr. Circuits (IPFA)*, Suzhou, Jul. 2013, pp. 249–254.
- [14] D. Marcon *et al.*, "Reliability analysis of permanent degradations on AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3132–3141, Oct. 2013.
- [15] G. Meneghesso *et al.*, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008.
- [16] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.
- [17] J. Joh and J. A. del Alamo, "Critical voltage for electrical degradation of GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 287–289, Apr. 2008.
- [18] J. Joh and J. A. del Alamo, "A current-transient methodology for trap analysis for GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, Jan. 2011.
- [19] J. Hu *et al.*, "Current transient spectroscopy for trapping analysis on Au-free AlGaIn/GaN Schottky barrier diode," *Appl. Phys. Lett.*, vol. 106, no. 8, pp. 083502-1–083502-4, Feb. 2015.
- [20] A. Terano, T. Tsuchiya, and K. Mochizuki, "Investigation of relationship between 2DEG density and reverse leakage current in AlGaIn/GaN Schottky barrier diodes," *Electron. Lett.*, vol. 48, no. 5, pp. 274–275, Mar. 2012.
- [21] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanisms in Schottky contacts to GaN and Al_{0.25}Ga_{0.75}N/GaN grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 99, no. 2, pp. 023703-1–023703-6, 2006.
- [22] M. Florović, J. Kováč, P. Benko, A. Chvála, J. Škriniarová, and P. Kordó, "Electrical properties of recessed AlGaIn/GaN Schottky diodes under off-state stress," *J. Elect. Eng.*, vol. 65, no. 5, pp. 313–316, Nov. 2014.
- [23] J. Hu *et al.*, "Physical origin of current collapse in Au-free AlGaIn/GaN Schottky barrier diodes," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 2196–2199, Sep./Oct. 2014.
- [24] D. Bisi *et al.*, "Deep-level characterization in GaN HEMTs—Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013.



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