A Folding Dickson-based Fully Integrated Wide Input Range Capacitive DC-DC Converter achieving Vout/2-Resolution and 71% Average Efficiency

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***Abstract*—This paper presents a fully integrated capacitive DC-DC converter with a wide input voltage range. The folding Dickson converter is used to implement four discrete voltage conversion ratios, capable of operating over a wide input voltage range. A subconverter is added, enabling four additional voltage conversion ratios, improving the input voltage resolution from V_{out} to $\frac{1}{2}V_{out}$. This way, the extra conversion ratios increase the overall efficiency, and at the same time reduce output ripple specifications. Implementing this additional converter at the end of the Dickson cascade reduces the complexity of driving the extra power train switches. This improved folding Dickson converter achieves an average efficiency above 70% at maximum output power, and operates over an input voltage range of 2.5-8V for an output voltage of 1.2V. The converter has been implemented and validated in a standard 90nm technology.**
(Keywords: Monolithic, Wide Input Range, Switched Capacitor and DC-DC Converter)

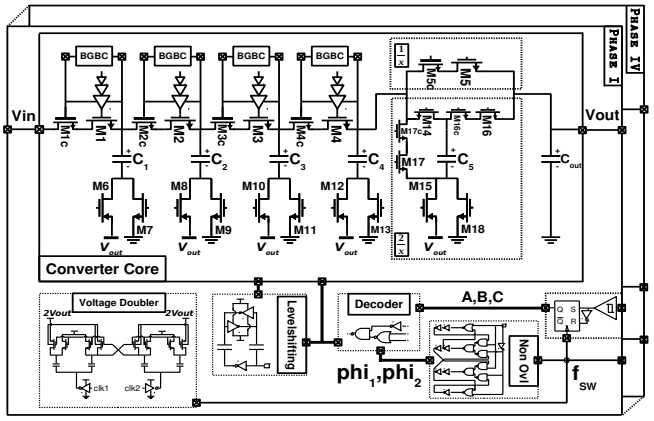

Fig. 1. System overview of the folding Dickson-based converter.

I. Introduction

High power density [1], [2], ultra-low ripple [3] and very fast transient response [4] designs have appeared in state-of-the-art fully integrated switched capacitor DC-DC converters and are bringing the topic to a state of maturity. However, few designs employ gearboxing to a large extent, usually limited to 2-3 topologies [3]–[6], and those that do never stray far from the V_{dd} of the used technology. In [7], DAC-like techniques give rise to a great number of voltage conversion ratios (VCRs), allthough at reduced output powers.

This paper introduces an improvement on the folding Dickson converter as presented in [8], which has an input voltage range of $> 4V_{dd}$, but suffers from reduced efficiency at higher conversion ratios, and requires high levels of fragmentations to keep the output ripple in check. Several insights and the addition of an extra subconverter, which is used to implement four extra topologies, allow us to maintain a high efficiency over a wide input voltage range.

This paper is organised as follows. In Section II, the design and operation of the converter is discussed, along with certain key insights. Section III presents the measurement results and compares the adapted folding Dickson converter with other fully integrated gearbox designs, before finally drawing conclusions in Section IV.

II. System Overview and Operation

A. The Folding Dickson Converter

Fig. 1 shows the schematic of the fragments, which are controlled by an on-chip hysteretic control loop. The converter builds further upon the folding Dickson converter, as seen in [8], which implements N voltage conversion ratios for an N-stage Dickson converter. Folding is realised by virtually merging the top and bottom plates of two or more flying capacitors, creating an equivalent lumped flying capacitor (Fig. 5). Merging is realised by changing the clock of the power train switches. Dedicated converters [8] generate the voltage supply required to drive flying switches M_{1-4}, whose operating conditions depend on input voltage and VCR. For a four stage Dickson converter, four topologies ($\frac{1}{2}, \frac{1}{3}, \frac{1}{4}, \frac{1}{5}$) are realised.

B. Improved Folding Dickson Converter

With the addition of the subconverter (see Fig. 3), four additional topologies ($\frac{2}{3}, \frac{2}{5}, \frac{2}{7}, \frac{2}{9}$) are possible, while leaving the operation of the folding Dickson converter unhampered. These extra topologies increase the overall efficiency over the input voltage range, and relax the ripple requirements, since each topology needs to cover a shorter range of V_{in} (leading to an increased input voltage resolution), and both are related to

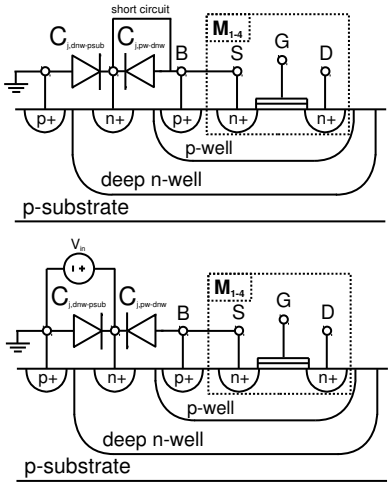

Fig. 2. Two well biasing strategies for power train switches M_{1-4}. In this implementation, the second option is chosen.

$\gamma = \frac{V_o}{V_{in} VCR}$ in the SSL-region [9].
Two additional design strategies allow us to maintain a good efficiency even for the higher conversion ratios:

1) Sizing of the switches by using a parasitic capacitance-based optimisation per topology, followed by a weighted average distribution. Instead of using a $G \cdot V^2$-metric for the switches, the following is used (as seen in [9]):

$$M_{sw,i} = \frac{G_i (v_{rated,i})^2}{C_G v_G^2, i + C_D v_{rated,i}^2 + C_B v_{B,i}^2} \quad (1)$$

with C_G, C_D and C_B the parasitic gate, drain-source and bulk capacitance, G the conductance per area, v_{rated} the maximum drain-source voltage, and v_G and v_B the voltage swing seen at the gate and bulk. Using this switch metric along with an energy loss cost constraint, switch sizing can be optimised for a given R_{FSL} and lowest parasitic losses [9].

2) Two approaches exist to bias the triple well structure of switches M_{1-4}. One is to short bulk, source and deep n-well together, preventing this first junction from conducting, as well as keeping the psub/deep n-well junction reversely biased. However, this means that the large junction capacitance $C_{j,dnw-psub}$ is subject to the voltage swing, causing increased parasitic losses. The other approach is to bias the N-well of isolated switches M_{1-4} with V_{in}. V_{in} is additionally decoupled, and the voltage swing is seen over the smaller junction capacitance $C_{j,pw-dnw}$, while keeping all junctions reversely biased (see fig. 2). In this implementation, the latter option is chosen.

C. Subconverter Operation

A detailed schematic of the subconverter is shown in Fig. 3, while the detailed gate drive signals and capacitor terminal voltages are shown in Fig. 4. In the $\frac{1}{x}$-mode, M_5 is turned off in phase phi_1, while it is conducting in phi_2, and capacitor C_5 is in parallel with C_4 in both phases (Fig. 5), which leads to the default folding Dickson converters, and allows operation in the $\frac{1}{2}$-,$\frac{1}{3}$-, $\frac{1}{4}$- and $\frac{1}{5}$-modes.

In the $\frac{2}{x}$-mode however, C_4 and C_5 are connected in parallel in phi_1, and connected in series in phi_2. To implement this converter, 5 additional switches (M_{14-18}) are required, as well as dynamic bulk biasing for M_5.

In the $\frac{2}{x}$-mode, the drain of M_{5c} drops below V_{out}, which would cause M_5 to turn on, and cause its body diode to start

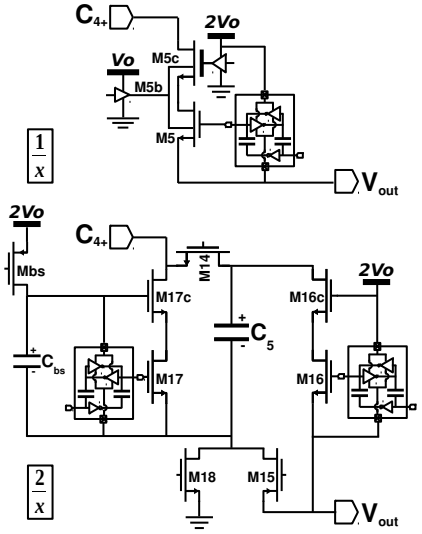

Fig. 3. Subconverter used to implement $\frac{1}{x}$ and $\frac{2}{x}$ conversion ratios.

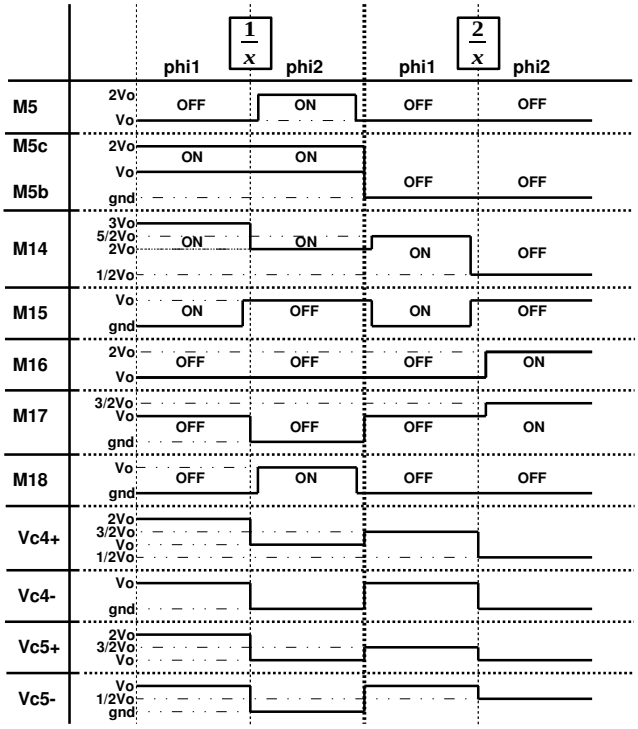

Fig. 4. Switching signals and voltages of the subconverter.

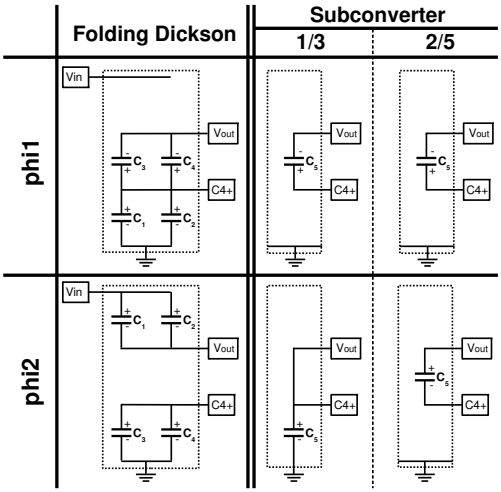

Fig. 5. Example converter operation in the $\frac{1}{3}$- and $\frac{2}{5}$-mode.

conducting. To prevent this, the bulk is connected to ground, as well as the gate of M_{5c}. In the $\frac{1}{x}$-mode, the gate of M_{5c} is connected to $2V_{out}$, generated by an on-chip voltage doubler (see Fig. 1), and the bulk is connected to V_{out}.

M_{15} and M_{18} reside between V_{out} and ground, which requires no special gate drive. M_{16} is driven from the on chip $2V_{out}$ supply, since it's source is connected to V_{out}. To drive M_{17}, an additional bootstrapping circuit is introduced. When C_5^- is connected to V_{out}, which occurs in both modi, M_{bs} turns on, and C_{bs} is charged from the $2V_{out}$-supply to V_{out}. In the other phase, C_{bs} can be used to turn on M_{17}, if required. The voltage over C_{bs} is also used to bias cascode M_{17c}. M_{bs} and C_{bs} are sized to achieve a time constant of $\tau_{bs} = \frac{T_{sw,min}}{5}$, and to allow a discharge of 10% when turning on M_{17}.

Since the source of M_{14} is connected to C_{4+}, the floating rail generated by the fourth Bootstrapped Gate Boost Converter (BGBC4) can be used to turn on this switch. These BGBC's use bootstrapping to copy the flying capacitor's top plate voltage, and charge a floating capacitor to V_{out}, which is then used to turn on switches $M_{1\text{-}4,14}$ and to bias their cascodes. The full operation and detail of the BGBC circuits can be found in [8]. As an example, Fig. 5 shows how the two modi are translated to the flying capacitor arrangement in the $\frac{1}{3}$- and the $\frac{2}{5}$-mode.

Flying capacitors are implemented using stacked MOM and MIM capacitors to increase density, for a total of 1.64nF. Output decoupling is done with 4nF MOSCAPs, while the input is decoupled with 400pF MOMCAP, capable of dealing with higher voltages.

III. Measurements

The efficiency has been measured over one decade of output power (2mW-20mW), while the output voltage is regulated to 1.2V. For P_{out}=20mW, the efficiency and input current are shown in Fig. 6. Besides the efficiency, Fig. 6 also shows the measured input current of the converter, and the ideal input current of a generic DC-DC converter with a fixed output

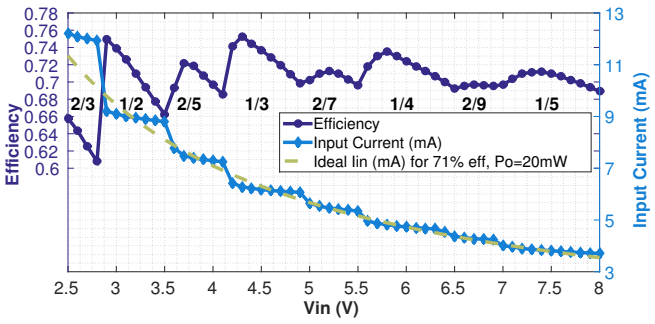

Fig. 6. Measured efficiency and input current (and ideal input current) for P_{out}=20mW, over V_{in} .

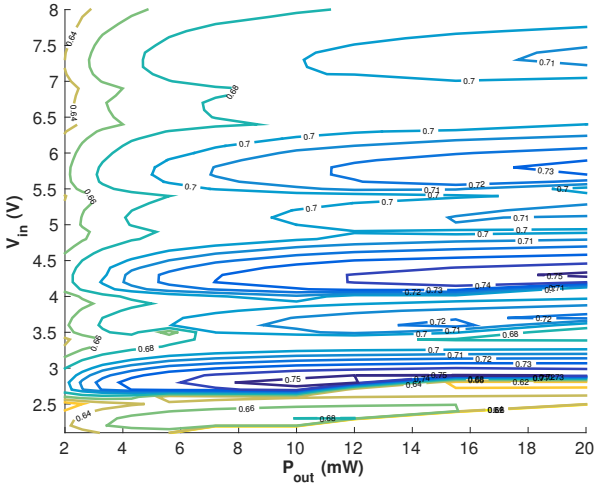

Fig. 7. Measured efficiencies for P_{out}=2-20mW and V_{in}=2.1-8V.

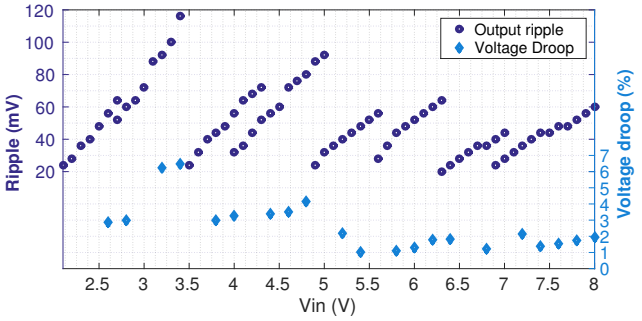

Fig. 8. Measured maximum output ripple, and load transient (I_{out}=1.67mA→11.67mA) as a function of input voltage.

power and an efficiency of 71%. Interestingly, it is seen that both input currents match closely, allowing the converter to keep its efficiency fairly constant. Increasing the resolution of the converter would allow to match this generic converter even more closely.

At maximum output power, efficiencies up to 75% are recorded in the $\frac{1}{2}$- and $\frac{1}{3}$-topologies, while most other topologies achieve peak efficiencies above 70%. Conversion ratio $\frac{2}{9}$ achieves the lowest peak efficiency, since its switching frequency is highest of all conversion ratios for a given R_{SSL}

Work	**[2]**	**[3]**	**[4]**	**[5]**	**[7]**	**[8]**	**This work**
technology	32nm SOI	90nm CMOS	65nm LP CMOS	28nm FD-SOI	0.25μm CMOS	90nm CMOS	90nm CMOS
$VCRs$	$\frac{2}{3},\frac{1}{2},\frac{1}{3}$	$\frac{2}{3},\frac{1}{2}$	$\frac{2}{5},\frac{1}{3}$	$\frac{5}{2},\frac{2}{1},\frac{3}{2}$	4-bit recursive	$(\frac{1}{2},\frac{1}{3},\frac{1}{4},\frac{1}{5})$	$\mathbf{\frac{2}{3},\frac{1}{2},\frac{2}{5},\frac{1}{3},\frac{2}{7},\frac{1}{4},\frac{2}{9},\frac{1}{5}}$
C_{fly}	MOS	1.15nF MO(M/S)	3.88nF MOS	MO(M/S)	3nF MIM	2nF MIM	1.64nF M(I/O)M
ρ (mW/mm2)	550	38.6	190	4.9	0.94	16.3	13.3
η_{avg}	66.5%	81%	74.3%	88%	69.2%	67%	**71%**
V_{out}	0.55-1.1V	0.7V	1V	1.2-2.4V	0.1-2.18V	1.2V	1.2V
V_{in}	2V	1.2-2V	3-4V	1V	2.5V	2.8-8V	**2.5-8V**

TABLE I: Comparison with other fully integrated gearbox DC-DC converters.

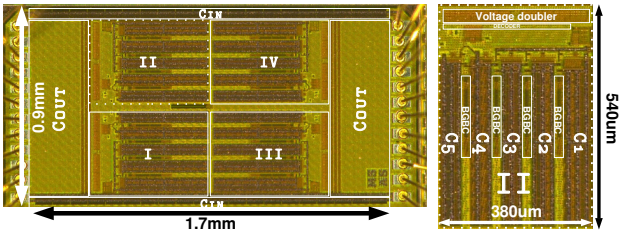

Fig. 9. Chip micrograph of the folding Dickson-based converter, and detail of one fragment.

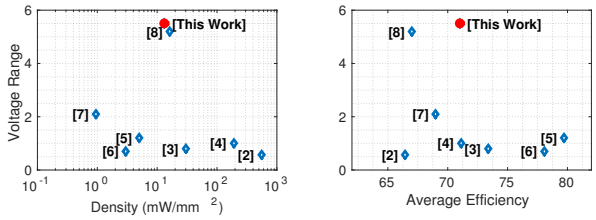

Fig. 10. Comparison of voltage range, power density and average efficiency of several monolithic gearbox converters.

[9]. However, it still achieves a peak efficiency of 69.7%.

The contour plot of the efficiency over V_{in} and P_{out} can be seen in Fig. 7. V_{in} ranges from 2.5V to 8V, allthough at power backoff the converter is able to work down to 2.1V. Efficiencies above 65% are seen over almost the entire range, and the average efficiency remains between 66% and 71% for the measured output power range.

Fig. 8 shows the maximum observed ripple during measurements. Step down ratio $\frac{1}{2}$ suffers most from increased output ripple due to its fast switching frequency backoff, but remains nonetheless below 10% of the output voltage. Also shown is the load transient response for an increase of 10mA/8ns in output current. Slew rate was limited by the off-chip load.

The chip micrograph can be seen in Fig. 9, along with a detailed figure of one fragment. The fragment shows the position of the decoding logic, on-chip voltage doubler, flying capacitors and helper converters (BGBCs).

A comparison with other gearbox designs is made in Fig. 10 and table I. While the power density of this design is neither high nor low compared to other designs, this DC-DC converter stands out at the achieved input voltage range, which is over 4.5 times the V_{dd} of this technology. Other designs achieve better average efficiencies, allthough over a much smaller input/output voltage range.

IV. Conclusion

The design, operation and measurement results of an improved folding Dickson converter have been discussed in this paper. By implementing an additional subconverter with 5 switches and 1 flying capacitor, four extra topologies are implemented, improving the input voltage resolution, having each topology operate over 0.6V V_{in}-range ($\frac{1}{2}V_{out}$) instead of 1.2V (V_{out}). This allows the converter to maintain high overall efficiencies, while mitigating demands on the output ripple. Peak efficiencies are measured up to 75%, with an average efficiency of 71% over the input range of 2.5-8V. This subconverter does not interfere with the folding Dickson's operation, which can be extended to any number of stages.

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