Saturation Photo-Voltage Methodology for Semiconductor/Insulator Interface Trap Spectroscopy

O. Madia,^{a,z} V. V. Afanas'ev,^a D. Cott,^b H. Arimura,^b C. Schulte-Braucks,^c H. C. Lin,^b D. Buca,^c N. Von Den Driesch,^c L. Nyns,^b T. Ivanov,^b D. Cuypers,^b and A. Stesmans^{a,*}

^aSemiconductor Physics Laboratory, KULeuven, 3001 Leuven, Belgium

^bIMEC, B-3001 Leuven, Belgium

^cPeter Grunberg Institut (PGI-9), Forschungszentrum Julich GmbH, 52428 Julich, Germany

The presence of large densities of electrically active defects is still an unsolved issue for future high-mobility/high-k CMOS device technologies. This relates to degraded device performance and reliability. Regrettably, conventional admittance-based characterization techniques often fail when applied to non-Si based devices. Among others, enhanced generation of minority carriers and much longer defect time constants make their results inaccurate. Rather than of seeking to adapt commonly-used techniques, we instead aim at direct measuring the semiconductor surface potential by means of the Saturation surface PhotoVoltage (SPV) technique. This approach allows for a DIT estimation which is not limited by the trap response time or hindered by minority carrier generation. Moreover, the DIT can be estimated over the whole bandgap regardless of sample doping type. We here report several case studies in support of the proposed approach. We will also show that SPV can be applied for the characterization of multi-layered Ge and III-V devices incorporating high-k insulators.

Integration of high-mobility semiconductors, like Ge or III-V compounds, as channel material in combination with high-k gate insulators in future nodes of Complementary Metal-Oxide-Semiconductor (CMOS) technology is increasingly advocated as a feasible solution to the well-known limitations of silicon. However, the presence of high densities of electrically active defects acting as charge traps largely hampers these efforts,¹⁻³ leading to degraded performance and poor reliability. Obviously, an accurate and reliable assessment of the interface trap density (N_{IT}) and energy distribution of their levels (D_{IT}) is critically needed for the development and evolution of novel channel architectures.

Yet, trap spectroscopy is still based on various combinations of capacitance-voltage (CV) and admittance measurements developed for Si/SiO₂ interface analysis nearly half a century ago.⁴ Over the past decade it has become increasingly clear that this approach is by far insufficient to provide reliable information about interface traps in high mobility semiconductor/high permittivity insulator channel stacks.⁵ Several problems emerge with the determination of trap density and the energy distribution of trap levels in the semiconductor bandgap.

First, in the case of semiconductors with bandgap smaller than silicon ($E_g(\text{Si}) = 1.12$ eV at 300 K), the minority carrier response is observed at high probing signal frequencies, hampering isolation of the capacitance or admittance signals associated with interface traps. Furthermore, since significant trap densities are present close to the semiconductor bandgap edges, it appears difficult to reach the high frequency regime in the capacitance measurements, which makes it problematic to determine the flatband voltage (V_{FB}).

Second, in addition to the fast interface traps, there is a significant contribution to N_{IT} of defects in the near-interface oxide layer, which have large time constants (> 10 ms)^{2,3,6,7} and cannot be assessed by using conventional ac admittance measurements. At the same time, application of the quasi-static CV technique is generally complicated by a low level leakage current across the thin high-k insulating layer. Also, application of high-temperature capacitance- and conductance-voltage (CV/GV) measurements may degrade the interface by subjecting samples to the bias-temperature stress. Finally, determination of the semiconductor surface potential (band bending) appears to be a problem by itself, for neither high-frequency nor quasi-static CV measurements can reliably be performed.

Several authors have proposed adjusted MOS admittance models to account for some of the issues mentioned above.^{8,9} Nevertheless, unambiguous interpretation of the admittance response of high-mobility semiconductor/high-k insulator interfaces is still under debate, with feasible solutions requiring full processing of a gate-controlled diode or a MOS transistor.

In this paper we will show that the problem of determining the interface trap energy distribution still can be solved in a MOS capacitor by using the saturation surface photovoltage (SPV) technique. This method has first been proposed in the early 70's¹⁰⁻¹² to directly measure the semiconductor surface potential ψ_s at any given gate bias V_G as the saturation photovoltage (SPV) value that corresponds to the variation of the band bending caused by high-intensity sample illumination. Then, the density distribution of interface charge trapping centers D_{IT} can be inferred with little additional computation from the difference between the measured $\psi_s(V_G)$ relationship and the ideal curve corresponding to the defect-free interface case. Additionally, the zero crossing of such $\psi_s(V_G)$ curve will always correspond to the flatband voltage and can be found without performing additional measurements.

We intend to demonstrate the effectiveness of the SPV technique by reporting a series of case studies: a (100)Si/SiO₂ reference; a Ge/GeO₂/Sc₂O₃/HfO₂ entity, a sample provided with a Ge *virtual substrate* (VS; thickness > 1 μ m) grown on a Si carrier wafer and with an high-k oxide stack (GeO_x – Al₂O₃ – HfO₂); a Si/Ge

VS/GeSn_{0.029}/HfO₂ structure; a lattice matched InP/In_{0.53}Ga_{0.47}As sample with a bi-layered GdAlO₃-HfO₂ insulator.

Comparison between the experimental results and the computed ideal $\psi_s(V_G)$ curve shows that the gate voltage induced surface potential variations can be accurately monitored in all studied samples. We will show that SPV is able to accurately extract the D_{IT} distributions over the full bandgap, regardless of the doping type of the sample under investigation.

Saturation Surface PhotoVoltage Technique

The principle of the SPV technique lies in the illumination-induced change in the semiconductor surface potential band bending: When the surface of a semiconductor is illuminated by a light pulse, electron-hole pairs are generated, resulting in redistribution of charge carriers near the surface causing reduction of the semiconductor band bending. This reduction defines the photovoltage (PV) value. If the light intensity is high enough to flatten the bands, the PV signal reaches the saturation value, which corresponds *exactly* to the initial surface potential value. Thus, by measuring the saturation PV, one may directly determine the semiconductor band bending for any given DC bias applied to the MOS capacitor. Noteworthy is that in saturation the flatband state is insensitive to the presence or occupancy of interface traps.¹³

Experimentally, the setup employs a Xe flash lamp producing high intensity light pulses (2 J max energy per $\approx$ 100 μ s long pulse) combined with low-pass filter optics $\lambda >$ 360 nm to avoid electron-hole pair generation in the insulator oxide layer, which would otherwise cause charge trapping in this layer upon illumination.

The PV was sensed externally on a load resistor R_L in series connection with the sample under investigation. The load resistor value was adjusted ($R_L = 40 \text{ k}\Omega - 5.6 \text{ M}\Omega$) according to the sample capacitance so that the resulting RC_{ACC} time constant (C_{ACC} is the capacitance of the sample biased in accumulation) is always greater than the light pulse width. This long time constant prevents charge loss during measurement, so that the whole PV signal will appear on R_L .

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Prior to each measurement, the PV is measured on the sample biased in accumulation or depletion as a function of the light intensity. Saturation of this value indicates that the light absorbed by the sample is sufficient to flatten the bands, and the recorded PV transient maxima correspond to the initial semiconductor band bending in darkness.

As a final remark, a time lapse of 3 seconds between consecutive light pulses was chosen in order to guarantee relaxation of the sample to the equilibrium state in darkness and avoid over-heating. Thus, we were able to detect traps with characteristic time constant ≤ 3 s. The accuracy on the final surface potential value extracted was estimated to be about 0.05 V. It is worth mentioning that, in different experimental implementations, one might want to trade off the sensitivity to traps with such large response time with a faster measurement. On this regard, a possible experimental configuration could make use of a laser shutter operated by a lock-in amplifier such as proposed in Ref. 14. Once the relationship between the band bending and the gate voltage is established, the defect contribution is calculated accordingly to Terman's model.¹⁵ By sweeping the DC gate voltage slowly enough (quasi-static measurement), the surface potential measured through SPV will correspond to the re-charging of interface traps, the density of which is then calculated as:

$$D_{IT}(\psi_s) = C_{ox}$$

$$q$$

$$\frac{d\psi_s}{dV_G}$$

$$-1$$

$$-1$$

$$-$$

$$-C_{s(\psi_s)}$$

$$q$$

$$[1]$$

where C_{ox} is the capacitance of the insulating stack, $\frac{d\psi_s}{dV_G}$

is the slope

of the band bending-gate voltage relationship as probed by the SPV measurements, and $C_{s(\psi_s)}$ is the semiconductor surface capacitance, computed assuming a uniform doping in-depth.

This methodology of interface trap density determination was tested on several MOS structures. For comparison, conventional CV/GV measurements were carried out as well using an HP4284A LCR meter.

Sample Preparation

Reference MOS capacitors were fabricated on a (100) p-type Si wafer by dry oxidation. The final oxide thickness was measured by spectroscopic ellipsometry to be 31 ± 1 nm. Devices were then completed by thermoresistive evaporation of semi-transparent Au electrodes of 0.5 mm² area on top of the oxide layer. The Si/SiO₂ interface defects were analyzed both on pristine samples and after subjection to a defect passivation anneal at 400 °C for 30 minutes in molecular hydrogen (1 atm).¹⁶

The second case study involves a Ge substrate passivated by Sc₂O₃ and GeO₂ layers, with a HfO₂ film as oxide insulators on top. Starting from an HF 2% dip for 30 seconds of the Ge wafer, 0.5 nm Sc₂O₃ layer was grown by the atomic layer deposition (ALD) process at 300 °C. Subsequent O₂ plasma oxidation, performed through the Sc₂O₃ layer, resulted in the formation of a GeO₂ interlayer (plasma conditions: 400 W, 5 sec, 300 °C). The process was concluded with the growth of

10 nm HfO₂ by the ALD process at 300 °C using HfCl₄ and H₂O as precursors. More details on the fabrication of the Sc₂O₃ layers can be found elsewhere.¹⁷

The samples of the third type are manufactured on a Ge VS (thickness $\geq 1 \mu\text{m}$) epitaxially grown on a Si carrier wafer on top of a strain-relief buffer. After a HF 2% clean for 30 s, an Al₂O₃ layer of ≈ 1 nm thick was deposited by ALD at 300 °C (10 cycles). Subsequently, O₂ plasma oxidation (800 W for 10 s at room temperature) was performed through the alumina layer in order to form a Ge oxide interlayer. Finally, an HfO₂ insulating cap was deposited on top by ALD at 300 °C using HfCl₄ and water as precursors. The final thicknesses of the insulating layers were estimated by XPS to be about 1 nm for GeO_x, 0.6 nm for Al₂O₃ and 2.3 nm for HfO₂.

The fourth sample has also been prepared on a Ge VS epitaxially grown on a Si carrier wafer: on this, a lattice-matched, fully strained, GeSn layer was subsequently grown by Reduced Pressure Chemical Vapor Deposition (RPCVD) using SnCl₄ and Si₂H₆ as precursors. The final Sn concentration was estimated at $[\text{Sn}] = 2.9 \pm 0.5\%$ and the thickness, as estimated by RBS, was 51 nm. After HF:HCl-last surface cleaning, a 10 nm thick HfO₂ layer was deposited by ALD using tetrakis(methylamino) hafium and ozone at 300 °C. More details on the fabrication process of these samples can be found in the literature.^{18–20} The last sample analyzed was fabricated on a (100)InP substrate with a lattice matched In_{0.53}Ga_{0.47}As layer on top. The insulator processing started with ALD deposition of a 2 nm 50% GaAlO₃ layer at 250 °C, followed by the deposition of 2 nm HfO₂ at 300 °C. All capacitors were completed by evaporation of semitransparent (13 nm thick) Au electrodes on top of the oxide.

Results

(100)Si/SiO₂.— First, we report on a case study of a Si/SiO₂ MOS structure to assess the validity, sensitivity, and accuracy of the SPV methodology by directly comparing the trap energy distributions derived from the SPV, to those inferred from conventional CV/GV measurements. As mentioned earlier, the measurements were conducted on Si/SiO₂ samples both without and with hydrogen passivation.¹⁶ Fig. 1a shows the PV transients measured for varying bias conditions on the (100)Si/SiO₂ structures after passivation treatment in molecular hydrogen. In Fig. 1b the corresponding surface potential is plotted versus gate bias (open symbols), together with the surface potential curve as measured with a step size of $\Delta V_G = 0.01$ V (black curve) and the theoretical curve computed according to Ref. 4 (blue curve).

The experimental $\psi_s(V_G)$ curves on the H-passivated sample exhibit good agreement with the theoretical one except for the deep depletion region ($V_G > 1$ V) where the low-level leakage current prevents the formation of the inversion layer, as also indicated by the CV curves presented in Fig. 1c. Nevertheless, SPV is still able to read the surface potential in this region and, importantly, no impact is expected on the trap density estimation, for the slope of the curve measured in depletion is, within accuracy, unaffected (see below).

Figure 1b also shows the SPV curve measured on the Si/SiO₂ samples after the defect passivation heat-treatment in molecular hydrogen (red curve). The different slope of the curves measured in the depletion gate bias range prior and after the passivation anneal reflects the contribution of unpassivated defects (Si dangling bond defects).

Finally, the D_{IT} vs E_{IT} (where E_{IT} is the interface trap energy relative to the valence band maximum (VBM)) energy distributions calculated using Eq. (1) are reported in Fig. 1d together with the ones extracted using the conventional AC-conductance method (bold

curves and open symbols, respectively). Overall, the results show good agreement and are consistent with the defect densities reported in the literature:²² DITs extracted from the pristine sample (red symbols in Fig. 1d) are in the order of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, clearly displaying the two characteristic peaks at $E_{IT} = 0.25$ and 0.85 eV corresponding to the $(+/0)$ and $(0/-)$ transitions of the Pb_0 centers at the $(100)\text{Si}/\text{SiO}_2$ interface. By contrast, the densities extracted on the passivated sample (black symbols) are in the low $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ range.

Figure 1. (a) Plot of voltage signals vs. time measured, at several gate biases (indicated numbers), on the p-type $(100)\text{Si}/\text{SiO}_2$ reference sample after passivation annealing in molecular hydrogen. The signal acquisition is set to be triggered by the falling phase of the electrical pulse generated to command the light source. Open symbols indicate the extracted surface potential values. (b) Surface potential versus gate bias (open square symbols correspond to the signals of Fig. 1a) as measured on the sample prior and after defects passivation in H_2 (red and black curve, respectively) and the theoretical curve as computed according to Ref. 4 by using the CVC software²¹ (blue curve). (c) CV curves as measured in the frequency range 1 kHz – 1 MHz on the sample after passivation anneal. (d) DIT(E_{IT}) distributions as evaluated by SPV and AC-conductance technique (bold curves and open symbols, respectively) on the sample prior- (red curve and symbols) and after passivation anneal in H_2 (black curve and symbols).

It is worth noting that, unlike the ac conductance method, the SPV technique is able to characterize the interface defect energy distributions across the entire bandgap on a sample of one doping type.

Ge/GeO₂/Sc₂O₃/HfO₂.— As mentioned in the introduction, enhanced minority carrier response in devices fabricated using semiconductors with a bandgap narrower than that of Si overlaps with the admittance signals coming from interface traps. Also, several authors have reported on a considerable contribution to defect densities present in devices fabricated with a high-mobility semiconductor and a high-k insulator that are characterized by a large time constant.^{2,3,6,7} Both phenomena pose fundamental threats to the characterization of such systems by means of conventional room-temperature ac admittance measurements. To gain further insight on these limitations we present a first case study on a Ge/GeO₂/Sc₂O₃/HfO₂ sample.

Figure 2. (a) 100 Hz and 100 kHz CV curves measured at room temperature

on the Ge/GeO₂/Sc₂O₃/HfO₂ sample. (b) Surface potential versus gate bias as measured by SPV (square symbols) and as computed by the CVC software (blue curve)²¹ by substituting characteristic parameters of Ge taken from Ref. 23 (c) D_{IT}(E_{IT}) energy distributions estimated by the ac conductance method (open symbols) and by means of the SPV technique (black curve).

Figure 2a shows the normalized CV curves measured on such sample at 100 Hz and 100 kHz (open and solid symbols, respectively). Here, it can be seen how the low frequency CV curve rises with advancing depletion, indicating enhanced generation of minority carriers (cf. page 105 of Ref. 4). Furthermore, the observed large hysteresis affecting these curves indicates the presence of a large density of *slow* traps. Figure 2b shows the surface potential versus gate bias relationship as measured (black open symbols) by the SPV technique and as computed according to Ref. 4 (blue curve). A first noteworthy consideration concerns the flatband voltage V_{FB}. As evident from Fig. 2a, the large hysteresis affecting the CV curves impedes accurate estimation of the V_{FB}. By contrast, the zero crossing of the SPV curve can be reliably found, giving V_{FB} ≈ 0.25

± 0.05 V. The D_{IT} distributions extracted through the ac conductance and SPV methods are compared in Fig. 2c (open and solid symbols, respectively). Remarkably, despite the additional contribution by the minority carriers response, the defect densities extracted by using the ac conductance method (open symbols) lies on a low range of 1 to 3 × 10¹² cm⁻² eV⁻¹, inconsistent with the large hysteresis affecting the CV curves. Instead, the results obtained through the SPV method (full symbols) are characterized by a more uniform distribution of about 9 to 12 × 10¹² cm⁻² eV⁻¹. This data is particularly interesting considering that it can be calculated for this insulator that approximately 2 V hysteresis shift on the CV curves would correspond to a defect density of about 8 × 10¹² cm⁻² [indicated by the dashed line in Fig. 2c].

Thus, evidence is found that the majority of the charge trapping centers present in the samples under investigation is characterized by a large time constant, for they can retain charge long enough to give rise to the large hysteresis in the CV characteristics. This makes them largely invisible to the conventional room temperature ac conductance method, whose extracted D_{IT} density distributions are inconsistently low. By contrast, results obtained through the SPV technique appear to be compatible with the hysteresis analysis.

Multi-layer Ge-based devices.— Novel high-mobility channel MOS devices are, for a large majority, fabricated as multi-layer structures on a Si carrier wafer. The presence of buried interfaces in the sample under investigation might be a reason of concern: Each interface will introduce a space charge region that may potentially interfere with the SPV signals measured at the surface (cf. Ref. 23). Nonetheless, if the additional interfaces lie deep enough below the semiconductor surface, the quasi-neutral region in between will screen their effect. Yet, as already stated by Kronik and Shapira,²³ little experimental work has been dedicated to this topic. To evaluate the possibility of accurately sensing the surface potential in multi-layer structures, we here present two case studies of MOS capacitors fabricated on a Ge *virtual substrate* grown on a Si carrier wafer.

Figure 3a shows an example of SPV data as collected on a Si/Ge VS/1 nm GeO_x/0.6 nm Al₂O₃/2.3 nm HfO₂ sample (black open symbols), together with the theoretical (blue) curve computed according to Ref. 4, using the Ge bulk parameters (bandgap width, intrinsic carrier concentration, and effective density of states in conduction and valence bands) and, for the oxide insulator, the measured areal capacitance. The agreement between the two curves is clear and, considering

that the somewhat different slope of the experimental curve is due to the effect of charge trapping, we can conclude that the presence of the buried interfaces between the Ge VS and the strain relief buffer, as well as between the buffer and the Si carrier wafer, has no measurable effect on the SPV response.

Figure 3b shows the CV curves measured in the frequency range 100 Hz – 1 MHz. The presence of buried layers results in a large series resistance causing a large frequency dispersion. The lack of reliable high-frequency curves impedes *de facto* the estimation of the flatband voltage. Also, no peaks could be resolved from the conductance response and thus no D_{IT} extraction could be performed by means of this ac conductance method. By contrast, the zero crossing of the surface potential curve measured through SPV can be found at about $V_{FB} = -0.05 \pm 0.05$ V and the D_{IT} energy distribution, as estimated by the SPV method, is shown in Fig. 3c.

To further affirm these results, a similar analysis was performed on a Si/Ge VS/GeSn_{0.03}/HfO₂ sample, the results of which are shown in Figs. 4a,4b,4c. Also in this case the theoretical surface potential versus gate bias curve [blue curve in Fig. 4a] was computed by using the characteristic parameters of Ge as, within the accuracy offered by the experimental set-up put in place, the presence of 2.9% Sn in alloy with Ge as no major effect on the semiconductor bandgap width or on the surface potential span. As can be seen, the $\psi_s(V_G)$ curve measured by SPV closely agrees with the theoretical curve across the entire gate voltage span. Similarly to the case study presented above, the CV/GV characteristic was found to be disturbed by a large series resistance and no D_{IT} values could be extracted; Fig. 4b shows the CV curves measured in the frequency range 100 kHz to 1 MHz. As a result, Fig. 4c shows only the D_{IT} density distribution as calculated by Eq. 1 from the SPV data.

In conclusion, the results shown here indicate that the effect of buried interfaces on the measured SPV signal falls within the experimental accuracy, provided that they lie deep enough below the semiconductor surface.

Figure 3. (a) Surface potential versus gate bias measured by SPV on a Si/Ge/GeO_x/Al₂O₃/HfO₂ sample (square symbols) and as computed (blue curve) by the CVC software²¹ by substituting characteristic parameters of Ge as retrieved from Ref. 23 (b) CV curves measured in the 100 Hz to 1 MHz frequency range at room temperature. (c) DIT energy distribution as estimated by mean of the SPV method.

InP/In_{0.53}Ga_{0.47}As/GdAlO₃/HfO₂.— An additional reason of concern, specifically regarding the application of the SPV characterization method to III-V semiconductor interfaces, arises from the possible presence of the Dember potential. This PV component is due to the different diffusion speed of electrons and holes in the bulk semiconductor. The electric field generated to compensate this difference would appear as an additional potential at the gate. Nonetheless, as noticed in Ref. 11, considering that the Dember potential does not saturate with respect to growing carrier injection, the existence of a saturation surface PV itself is an indication that the Dember potential is negligible since the latter should increase linearly with the intensity of the incident.

To confirm the validity of this consideration, we report results Obtained on an In_{0.53}Ga_{0.47}As/GdAlO₃/HfO₂ structure fabricated on an InP carrier wafer. Fig. 5 shows the $\psi_s(V_G)$ curves (panel a) measured by means of the SPV technique and as computed according to Ref. 4 (black open symbols and blue solid curve, respectively), and (panel

b) the CV curves measured in the frequency range 100 Hz – 1 MHz. As can be seen in Fig. 5a the surface potential can be efficiently

Figure 4. (a) Surface potential versus gate bias measured by SPV on a Si/Ge/GeSn_{0.03}/Al₂O₃/HfO₂ sample and as computed by the CVC software²¹ by substituting characteristic parameters of Ge as retrieved from Ref. 23 (b) CV curves measured at room temperature in the frequency range 100 kHz to 1 MHz. (c) DIT(EIT) energy distribution as extracted by means of the SPV method.

swept from accumulation to inversion and the experimental values are in good agreement with the theoretical curve. Fig. 5c shows the DIT distributions as extracted by means of SPV and the conventional conductance method (black curve and open symbols, respectively). Remarkably, the two results closely agree with a mid-gap density of about $D_{IT}(\text{mid-gap}) = (5 \pm 1) \times 10^{12}$ (cm⁻² eV⁻¹).

Thus, all considered, we found no evidence for the presence of additional contribution given by the Dember potential.

Figure 5. (a) Surface potential vs gate bias $\psi_s(V_G)$ curves as measured through the SPV technique (open symbols) and as computed by the CVC software²¹ (blue curve) by using the semiconductor parameters as retrieved from Ref. 23. (b) Resume of the CV curves as measured in the frequency range 100 Hz – 1 MHz on the InP/In_{0.53}Ga_{0.47}As/2 nm GdAlO₃/2 nm HfO₂ sample. (c) The DIT distributions estimated by the SPV technique (black curve) and by mean of the ac conductance method (open squares).

Conclusions

To conclude, we have performed SPV experiments on a variety of samples, spanning from the conventional (100)Si/SiO₂ to a InP/In_{0.53}Ga_{0.47}As/GdAlO₃/HfO₂ structure.

We have assessed the validity of the methodology put in place by comparing SPV results with conventional CV and ac conductance measurements on a (100)Si/SiO₂ sample prior- and after defect

passivation heat-treatment in molecular hydrogen. We have demonstrated that the surface potential can be directly measured and the D_{IT} distribution and flatband voltage V_{FB} can be accurately extracted by means of SPV, even in the case of inequilibrium depletion.

Next, results obtained on a Ge/GeO₂/Sc₂O₃/HfO₂ sample provided a case study of the limitations that conventional admittance-based characterization techniques face when applied to high-mobility/high- k devices. Above all, a large hysteresis affecting the CV curves was observed in spite of the relatively low D_{IT} s as estimated by means of room temperature ac conductance measurements. We thus concluded that the majority of the charge trapping centers found in the sample under investigation are characterized by a large time constant and consequently fall outside the experimental window of conventional room temperature admittance-based characterization techniques. By contrast, results obtained through the SPV technique appear to be compatible with the hysteresis analysis.

Results obtained on Si/Ge *virtual substrate*/1 nm GeO_x/0.6 nm Al₂O₃/2.3 nm HfO₂ and Si/Ge VS/GeSn_{0.03}/HfO₂ entities showed that the surface potential can be measured also in presence of buried interfaces, provided that they lie deep enough below the semiconductor/insulator interface. Comparison of the experimental data to the calculated surface potential vs. gate bias relationship reveals that whether or not the additional space charge regions in the sample have an effect on the band bending at the semiconductor surface, lies within the attained experimental accuracy.

Finally, results obtained on the InP/In_{0.53}Ga_{0.47}As/GdAlO₃/HfO₂ structure reveals that the presence of a Dember potential, a component predicted to arise in III-V semiconductors, has no measurable effect on the measured surface potential. Moreover, in this last case the D_{IT} distributions extracted by means of SPV and ac conductance methods show good agreement.

All in all, the results reported show that the SPV technique enables direct measurement of the effective surface potential modulation in a MOS capacitor. As a result, it allows one to reliably characterize D_{IT} distributions, mitigating well-known limitations of the more widely used techniques. Above all, SPV can sense the whole semiconductor bandgap regardless of the semiconductor doping type.

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