Constant voltage electromigration for advanced BEOL copper interconnects

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Abstract - For characterizing the electromigration (EM) reliability of advanced interconnects, we propose a constant voltage approach (CV-EM) as an alternative method to traditional constant current tests (CI-EM). As extremely scaled interconnects require very thin barriers, their current shunting capabilities will be reduced. When close to full void formation, we show that this lack of current shunting capability leads to unrealistically high stress conditions during CI-EM while more realistic stresses are induced during CV-EM. We also demonstrate that the void detection capability is highly improved after CV-EM. We use simulations and experiments to compare CV-EM with CI-EM where we obtain a) slightly longer lifetimes for CV-EM, b) the same failure mechanisms and c) similar E_a and n values.

Keywords - Mn-based barriers; electromigration; constant voltage-EM; constant current-EM; multiple failure; void detection capability

I. INTRODUCTION

Due to the downscaling of interconnects for future CMOS technologies, the effective resistivity and line resistance of Cu interconnects increase drastically [1]. Compared to conventional thick conductive barriers, i.e. 3-6nm PVD TaNTa, an aggressively thinner conductive or even non-conductive barrier will be needed for advanced Cu interconnects. Thinner barriers allow for more copper area in similar trench dimensions and non-conductive barriers can reduce the electron scattering at the barrier/copper interface [2], leading to a reduction of the effective resistance.

Electromigration (EM) is one of the main metal failure mechanisms of BEOL interconnects. EM is the result of the movement of copper due to an electron wind caused by an electrical current [3]. EM in copper interconnects ultimately results in voids that span the whole line width and height. Curve A in figure 1 shows a typical resistance versus time trace of a copper interconnect with a traditional conductive barrier which is subjected to an electromigration stress (high temperature and current density). Three phases are observed. In phase I, which is linked to the void formation process, no significant change in the resistance is observed. Once a void is formed that spans the whole line width and height, the current

locally has to flow through the metallic barrier, a phenomenon often referred to as current shunting [4]. Such an event is characterized by a jump in the resistance versus time curve (phase II). After this jump, a linear increase of the resistance as a function of time is observed (phase III). During this phase, the void grows in the direction of the line length.

Due to the fact that very thin conductive or non-conductive barriers have limited current shunting capabilities (curve B in figure 1), the local electrical parameters close to full void formation are different compared to traditional Ta-based barriers. In this paper, it will be shown that during conventional constant current EM (CI-EM) unrealistic stresses occur in extremely scaled interconnects. Hence, we believe a revision of the EM-test methodology is needed and that constant voltage EM (CV-EM) testing could become more appropriate to characterize EM for advanced interconnects.

Also note that another advantage of CV-EM is earlier reported in [5,6], where it is proposed that CI-EM is more

Figure 1. The comparison of R-t curves between conductive barrier (A) and non-conductive barrier (B).

affected by variations in cross sectional area, where this type of variations can become problematic and remedial measures are being taken [7]. The authors argue in [5,6] that, as $V=J*\rho*L$ (where V , J , ρ , L are voltage, current density, resistivity and the length of line respectively), a constant voltage stress does not depend on the variation of the cross sectional area, suggesting that CV-EM becomes a more appropriate method to study intrinsic EM without taking process variability into account.

In this paper, the CV-EM test methodology is studied in detail for interconnects with non-conductive barriers. Failure times, current exponents n , activation energies E_a and void detection capability and locations are compared between CV-EM and CI-EM using simulations and experiments.

II. PROCESS AND EXPERIMENTS

As a case study, we use Cu interconnects with a non-conductive Mn-based self-forming barrier (SFB), where promising time dependent dielectric breakdown and electromigration (EM) performance was recently reported [8]. The test vehicle consists of 20nm $\frac{1}{2}$ pitch lines integrated in a SiO₂ intermetal dielectric using Spacer-Defined-Double-Patterning (SDDP) [9]. The trenches were filled using a 1nm thick Mn-based SFB followed by a Mn-doped PVD Cu Seed, plating and CMP. The lines were capped with a 30nm SiCN dielectric layer and a thick passivation consisting of 300nm SiO₂ and 500nm SiN. The use of a Mn-based SFB is expected to show no current shunting due to the fact that Mn forms MnSi_xO_y silicates, where such silicates can be considered as dielectrics and will not be able to shunt current after full void formation.

The electromigration structure consists of a 100 μ m long single damascene line (no via's) with a line width of 20nm and an aspect ratio of 3. Both CI- and CV-EM tests were done on a package level reliability tester from Cascade Microtech. All EM tests were done at temperatures between 270°C and 330°C. CI-EM was performed at current densities between 3.0 and 7.5 MA/cm². CV-EM voltages were chosen in a way that the initial stress current densities were similar to those applied during CI-EM. At each stress condition, 8-16 devices were tested. Failure Analysis was done using top-down Scanning Electron Microscopy (SEM) inspection and Transmission Electron Microcopy (TEM) after void formation, where the passivation layers were removed prior to the SEM inspection.

III. RESULTS AND DISCUSSION

Figure 2 shows typical resistance versus time traces for a CI-EM test. As expected, no current shunting is observed. However, an erratic behavior (referred to as multiple failure) happens close to full void formation for most samples. Hence, different lifetimes are observed for different failure criteria, as shown in figure 3, which is not expected for structures that do not have current shunting capabilities and which makes lifetime assessment difficult. Also, we will show below that void location assessment and failure analysis is complicated due to this erratic behavior.

Figure 2. Typical resistance versus time traces during CI-EM.

Figure 3. Failure times for different failure criteria.

In order to better understand the erratic behavior at the final phase of void formation and after full void formation, we conducted calculations to estimate the local current density through the Cu at the location of the void (J_{Cu}) and the voltage drop over the void (V_{void}) in trenches with either TaNTa (= conductive) or Mn-based (= non-conductive) barriers. We also included a so-called semi-conductive barrier in our calculations, where a semi-conductive barrier has high, but not infinite, resistivity. Such barrier is representative for extremely thin conductive barriers. The void formation model has been taken from [10-11]: the void is assumed to form with a fixed length (assumed to be 50nm in our calculations) into the line with a height H_{void} as a function of time. The assumptions of barrier thickness and resistivity for the different cases are summarized in table I.

The results are summarized in figure 4, where both the CI- and CV-EM cases are considered. Note that only the end of the void formation process is plotted, where H_{void} is close to the total trench height which is considered to be 60 nm in our calculations.

TABLE I. ASSUMED BARRIER THICKNESS AND RESISTIVITY FOR THE DIFFERENT CASES CONSIDERED

Barrier	Thickness (nm)	Resistivity ($\mu\Omega\cdot\text{cm}$)
Conductive	1.5	250
Semi-conductive	0.7	1000
Non-conductive	1	N.A.

Figure 4. Simulation of (A) the local current density (J_{Cu}) in the void region and (B) the potential difference (V_{void}) over the void before full void formation.

For the case of a conductive barrier, J_{Cu} and V_{void} show similar trends for both CI-EM and CV-EM. In the case of CI-EM, J_{Cu} is limited at the end of the void formation phase: the resistance of the remaining Cu becomes much higher than the resistance of the barrier and thus the electron wind flows mainly through the barrier, keeping J_{Cu} low. Also V_{void} is limited as the total resistance of the void is a parallel connection between the remaining Cu and the barrier. In the case of CV-EM, J_{Cu} and V_{void} are limited through the experimental set-up: the moment the resistance becomes too high, the current (and thus J_{Cu}) goes down to keep the voltage constant.

The case of a non-conductive barrier, however, is different. Due to the lack of current shunting capabilities, both J_{Cu} and V_{void} during CI-EM become very high, resulting in an acceleration of void formation. This acceleration is unrealistic as such high V_{void} values do not occur in practice. Due to its particular experimental set-up, CV-EM induces more steady stresses in the void region close to full void formation, as shown in figure 4.

These simple calculations suggest that CV-EM is a more appropriate method for EM characterization when barriers become less conductive. Note that in the case of a semi-conductive barrier high values of J_{Cu} and V_{void} are expected as

well, suggesting CV-EM might become more appropriate for highly scaled conductive barriers as well.

In order to understand and quantify possible differences in failure mechanism, EM lifetimes and reliability parameters between CI-EM and CV-EM, our simple void formation model was extended by assuming that the void depletion rate is the same in all cases (CI-EM versus CV-EM and conductive versus non-conductive barriers) and only depends on J_{Cu} , neglecting Joule heating effects.

Our calculations suggest that, in order to avoid the multiple failures shown in figure 2, two solutions are possible. First, the compliance voltage of the current source can be reduced such that the excessive V_{void} -values at the end of the void formation phase during CI-EM are limited by the current source. Such solution is difficult in practice as setting the compliance voltage will depend on the resistance of the structure during EM and also does depend on the chosen test structure and stress condition. Alternatively, CV-EM can be performed. Figure 5 shows typical resistance versus time curves during CV-EM. The voltage was set in such a way that the initial current density was the same as the current densities applied for the CI-EM experiments shown in figure 2. It can clearly be observed that the erratic behavior observed during CI-EM is not existing during CV-EM.

Simulated resistance versus time traces are shown in figure 6, where a void depletion rate of $0.15\text{h}/\text{nm}^3$, which is a representative value for our samples tested at 300°C and $1\text{MA}/\text{cm}^2$, was assumed. Also, the activation energy E_a and current acceleration factor n from Black's equation [12] obtained from our CI-EM measurements are taken as starting values. The simulations suggest that the non-conductive Mn-based barriers fail slightly faster than conductive TaNTa barriers and that CI-EM leads to slightly shorter lifetimes than CV-EM. The larger J_{Cu} shown in figure 4A induces faster failures. Note that the differences mentioned above are rather small and insignificantly fall within typical error bars obtained on lifetimes obtained during technology qualification.

Figure 5. Typical resistance versus time traces during CV-EM. No multiple failures and no change of failure time with failure criterion is observed.

Figure 6. R_{void} change with stress time during void formation by simulation. Assumption: void depletion rate only depends on J_{Cu} .

Experimental evidence of the above mentioned differences is shown in figures 7 and 8. Figure 7 shows details of one typical resistance versus time curve, which can be separated into two parts (part-1 and part-2). The lifetime of part-1 for CI-EM and CV-EM shows no difference, as shown in figure 8. This is because the initial stress conditions do not differ between CI-EM and CV-EM, as suggested in figure 4. Figure 8 also shows that when the void is almost fully depleted and significantly contributes to the total resistance (part-2), the lifetime during CV-EM is longer due to its more limited stress (Figure 4A). Therefore, the total failure time in CV-EM is slightly longer than that in CI-EM.

We also use our simulations to investigate eventual differences between activation energy E_a and n . As shown in figure 9, the simulation results suggest that similar n and E_a will be obtained during CI-EM and CV-EM. This is experimentally validated by our experiments as summarized in figure 10.

Figure 7. Typical resistance versus time curve before full void formation with different parts indicated: part-1 (R is constant) and part-2 (R increase).

Figure 8. Comparison of CV-EM and CI-EM at a same stress condition-330°C&4.5MA/cm². CV-EM shows a longer lifetime in part-2, but not in part-1.

Figure 9. Simulation of lifetime under CV-EM and CI-EM, (a) n extracted by varying J , $T=105^\circ\text{C}$, (b) E_a extracted by varying T , $J=1\text{MA/cm}^2$.

Figure 10. Comparison of n and E_a obtained from CI-EM and CV-EM measurements. Similar n and E_a were obtained, which is in agreement with our simulations shown in figure 9.

Finally, we compared the void locations using top-down SEM inspections. It was found that all the voids were formed close to the cathode side, which is expected for our single-damascene test vehicle [13], indicating no difference in failure mechanism. Also, for some samples tested with CI-EM, voids could not be detected at all. The percentage of samples where voids were detected depends on the compliance voltage V_c of our current source, as summarized in Table II. One possible reason is that voids were rapidly repaired by the high voltage drop over the full void (Figure 4B). The TEM cross-section shown in figure 11 shows that the copper at the two sides of the void are very close to each other, which could be the possible explanation for the observed erratic behavior due to a refill of the void by the high electrical fields between small voids.

IV. CONCLUSIONS

Traditional constant current electromigration tests (CI-EM) on advanced interconnects with ultra-thin semi-conductive or non-conductive barriers will lead to unrealistically high stress conditions at the end of the void formation phase, where an erratic behavior of the resistance after full void formation is observed. As an alternative to CI-EM, we propose constant voltage EM (CV-EM). Both CI-EM and CV-EM test approaches lead to the same failure mechanism with similar activation energy E_a and current acceleration factor n , where a slightly longer failure time is observed for CV-EM, due to the limitation of the voltage over the void at the end of the void formation phase. Due to its more realistic stress conditions close to full void formation and a higher yield of void detectability, we propose CV-EM as a more appropriate method to characterize EM in future generation interconnects.

TABLE II. STATISTICS OF TDSEM IMAGE ON SAMPLES WITH DIFFERENT EM STRESSES. CV-EM SHOWS A HIGHER YIELD OF VISIBLE VOIDS.

Type of test	Void location	% of samples where void is detected
CI-EM ($V_c=10V$)	Cathode side	30
CI-EM ($V_c=1.5V$)	Cathode side	85
CV-EM	Cathode side	100

Figure 11. Cross sectional TEM image of one failed sample stressed with CI-EM with $V_c=10V$.

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