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Redundancy Effect on the Performance of Digitally-Assisted SAR ADCs

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Abstract—This paper presents a thorough assessment of the impact redundancy has on background calibration performance in SAR ADCs with static and dynamic non-idealities. A configurable model that is capable of implementing different SAR architectures is used to inject various implementation impairments and analyze the impact redundancy has on them. The effects of a redundant capacitor array on calibration are first analyzed in the presence of static non-idealities, after which then incomplete settling effects and noise are added. The effect of redundancy in the spread of the calibrated ENOB of multiple simulations is assessed. A tradeoff between increased tolerance to settling errors and calibration performance is shown, allowing to optimize the amount of redundancy and number of SAR cycles for minimum energy consumption for a given target ENOB.

Index Terms—SAR ADC, background calibration, redundancy, dynamic effects, weight calibration, capacitor mismatch correction

I. INTRODUCTION

Successive Approximation SAR ADCs are well known for their advantage in terms of CMOS scaling, power consumption and die-area in low-to-medium resolution converters. By combining them with other ADC techniques their applications can broaden; their resolution can be increased through pipelining [1], and their conversion speed can be improved through time-interleaving [2]. The main issues that affect SAR ADC performance are capacitor mismatch, comparator offset, and incomplete settling. Extensive research has been done in the digital background correction of these issues; most of these approaches include some form of redundancy.

Redundancy can be introduced into a SAR ADC by modifying the ratios of its capacitor array. A generalized redundancy design scheme is presented in [3]. The effect of redundancy in facilitating the digital correction of static non-linearities, and the tolerance it adds to dynamic conversion errors has been demonstrated for different calibration approaches [4]–[6]. A mathematical model that predicts the minimal number of cycles and redundancy needed for a given DAC is presented in [7]. However, no analysis has systematically assessed the impact of redundancy on the post-calibration ADC performance spread, and this under joint static and dynamic non-idealities. In this work it is shown how increasing redundancy is linked to an increase in reliability of post-calibration target performance compared to converters without redundancy. Both under static and/or dynamic non-idealities an optimum amount of redundancy can be found given the expected amount of mismatch and the desired capacitor array settling time.

The modeling of the static and dynamic non-idealities

of the SAR ADC are presented in Section II. Section III presents the digital calibration algorithm that will be used to calibrate the binary and non-binary converters, and its relation to redundancy. Finally, Section IV presents the results of the analysis of the impact of redundancy on the calibration of static and dynamic non-idealities, with and without noise added.

II. STATIC AND DYNAMIC NONLINEARITY MODELING IN SAR ADCs

A. SAR ADC configurable model

The proposed base model of the SAR ADC consists of an array of capacitors that form the CDAC, each with a given randomly generated mismatch, a comparator with a configurable amount of noise and offset, and digital synchronous SAR control logic. The model used for the simulations presented in this work is fully differential. The CDAC is here modeled using the split charge redistribution scheme as in [8], although simulations show that CDAC architecture has not significant impact on the post-calibration performance.

B. Effects of static non-idealities in ADC output

Each capacitor has a value C_i . Each of the N conversion steps has a given weight W_i given the ratio:

$$W_i = \frac{C_i}{C_{00} + \sum_{k=0}^{k=N} C_k} \quad (1)$$

Each analog value W_i has a digital counterpart $\hat{W}_i$, initialized to the ideal value of W_i . The N output bits b_i and the digital weights $\hat{W}_i$ are then used to reconstruct the digital output $\hat{X}$.

$$\hat{X} = \sum_{i=1}^N \hat{W}_i b_i \quad (2)$$

Due to capacitor mismatch, the ratios between the capacitors differ from their ideal value C_i due to a mismatch error e_{C_i} . Because of this, the analog weights W_i differ from their digital counterparts $\hat{W}_i$ by an error e_{W_i} :

$$W_i = \frac{C_i + e_{C_i}}{C_{00} + e_{C_{00}} + \sum_{k=0}^{k=N} C_k + e_{C_k}} = \hat{W}_i + e_{W_i} \quad (3)$$

The digital output $\hat{X}$ of the SAR ADC can be represented as the weighted sum of the bits b_i :

$$\hat{X} = \sum_{i=1}^N (\hat{W}_i + e_{W_i}) b_i = \sum_{i=1}^N \hat{W}_i b_i + \sum_{i=1}^N e_{W_i} b_i \quad (4)$$

which can be separated into the terms X_{ideal} and the error term $e_{\hat{X}}$:

$$e_{\hat{X}} = \sum_1^N e_{\hat{W}_i} b_i \quad (5)$$

If we add the comparator offset X_{offset} and noise X_{noise} , the final digital output $\hat{X}$ can be seen as:

$$\hat{X} = X_{ideal} + e_{\hat{X}} + X_{offset} + X_{noise} \quad (6)$$

The idea behind the capacitor calibration of a SAR ADC is to adjust the digital weights $\hat{W}_i$ by estimating and subtracting the weight errors $e_{\hat{W}_i}$ and the value of the comparator offset. These estimates can be obtained by using an LMS algorithm. This will be explained in more detail in Section III. Mismatch in the model is generated randomly with a normal error probability with zero mean and a given standard deviation σ . The σ value of the mismatch in the unitary capacitor of the array (The LSB capacitor is one unitary capacitor) is given as an input to the model. Larger capacitors are built from smaller unitary ones, hence automatically adjusting the mismatch accordingly. The total capacitance C_T of all arrays used in our comparisons is the same, in order for them to have the same kt/C noise floor, and so the unitary capacitance C_u of an array is calculated by dividing the total capacitance by the sum of the ratios of the converter.

C. Redundancy

Mismatch in a SAR's capacitor array can translate into two kinds of errors. Either values are assigned to a wrong (but unique) digital code (a 'missing code' in the transfer curve), or multiple input values are assigned to the same digital code (a 'missing level'). In a radix 2 SAR ADC each capacitor is exactly equal to the sum of the capacitors smaller than it. Ideally, this results in a perfect transfer curve, yet the slightest capacitor mismatch creates missing codes and missing levels. While missing levels can be corrected by digital calibration, missing codes cannot hence decreasing ADC performance. By introducing redundancy, additional redundant output codes are created on purpose, in such a way that, after calibration, the likelihood of missing levels decreases drastically. In such sub-radix 2 arrays capacitor is smaller than the sum of the smaller part of the array (usually known as sub radix 2 arrays), thus ensuring that even when mismatch is present, no 'gaps' will occur (to a certain degree) [6]. The amount of redundancy has to be carefully weighted against the desired performance yield, the expected amount of mismatch, and the power consumption penalty it might bring. Redundancy has, due to its creation of redundant output codes, beneficial effects on dynamic circuit impairments. If due to incomplete settling a wrong decision is done by the comparator, it is possible to still reach the correct code due to these redundant decision paths.

D. Modeling of dynamic effects

Dynamic errors in SAR ADCs are caused primarily by incomplete capacitor settling. If the comparator makes a decision before the capacitor being switched in a given SAR step

Fig. 1. Calibration method used

finishes settling, an error can occur. This can be prevented by a sufficiently large conversion step period, which sets a limit on the conversion speed of the ADC. To improve speed and power consumption a reduced step period might be beneficial. This increases ADC bandwidth, while avoiding power-hungry, fast-settling, stable reference buffers.

The voltage V_{CDAC} at the input of the comparator at the end of conversion step n , taking settling into account, is calculated by:

$$V_{CDAC}(n) = \sum_{i=0}^{i=n} \hat{W}_i b_i e^{-\frac{(n-i+1)T_{cs}}{\tau_i}} (V_{REF+} - V_{REF-}) \quad (7)$$

Each capacitor in the CDAC array has its own RC time constant τ_i to settle. As this model is for an internally synchronous SAR, each decision occurs after a given step conversion period T_{cs} , which is the same for all SAR cycles. At each conversion step the contribution of each capacitor is recalculated, as capacitors used in previous conversions have had $(n-i+1)$ conversion periods to settle. A settling error will cause V_{CDAC} to deviate from its ideal value, the comparator sometimes making a wrong decision that will result in a conversion error. Incomplete settling effects are hard to combat with digital calibration, and are typically tackled through a combination of increased drive strength reference buffers and increased redundancy. As both come with a power penalty, it is important to carefully assess this trade-off, taking the impact on post-calibration performance into account.

III. SAR CALIBRATION

In order to show how background calibration benefits from redundancy, a modified split-ADC method based on [9] will be used. In this approach the capacitor's CDAC is split in two almost identical arrays, each with half the area of the original. The final output is the average of both conversions, as shown in Figure 1. Unlike the original implementation, which requires constant reshuffling of the capacitors, offsets similar to [6] are used to provide different decision paths between both branches. Their difference ε minus the value of Δ is used to calibrate the ADC weights.

The coefficients of the LMS estimation are the bit weights for each converter $\hat{W}_A$ and $\hat{W}_B$ and the calibration offset $\hat{\Delta}$. Their value at conversion step $t+1$ is dependent on the value of the bits and the difference signal ε at a given conversion step T_{cs} . The compensation of $\hat{\Delta}$ can also correct for comparator

Fig. 2. Mismatch effect on Monte Carlo runs before and after calibration

offset errors.

$$\hat{W}_{A(i,t+1)} = \hat{W}_{A(i,t)} - \mu_w \varepsilon_t b_{Ai} \quad (8)$$

$$\hat{W}_{B(i,t+1)} = \hat{W}_{B(i,t)} - \mu_w \varepsilon_t (-b_{Bi}) \quad (9)$$

$$\hat{\Delta}_{t+1} = \hat{\Delta}_t - \mu_\Delta \varepsilon_t \quad (10)$$

The LMS update rates μ_w and μ_Δ are chosen conservatively so the convergence of the algorithm is guaranteed.

IV. SIMULATION RESULTS AND TRADEOFF ANALYSIS

In the following subsections a thorough analysis of the effects that redundancy has on calibration will be presented. The literature often compares binary (radix 2) converters with sub-binary (sub-radix 2) converters with the same number of effective bits, hence resulting in more conversion steps for sub-binary. Unlike other works we choose to compare binary and sub-binary converters with the same number of steps, and the same total capacitance, to make a fair judgement under equal power consumption. The following experiments will show that the performance after calibration can be higher depending on the amount of mismatch. Linearity is measured in ENOB, based on SNDR measurements:

$$ENOB = (SNDR - 1.76)/6.02 \quad (11)$$

A. Redundancy effect on static non-idealities

Fig. 2 shows the effect that different values of capacitor mismatch σ have on the calibration of 14-bit capacitor arrays. Figs 2a and 2b show a comparison between a radix 2 and a radix 1.86 converter at different mismatch levels. It can be seen that when mismatch is low, binary converters have a better performance, but the spread between the calibrated results of Monte Carlo simulations is higher than for the sub-binary converter. When mismatch increases the performance of the binary converter decreases, and the spread of the calibrated values increases. The performance and the spread of the sub-binary converter stay almost the same. Figure 3 shows the ENOB after calibration for a wide range of mismatch σ values and radices, where the same trend can be observed. One can see that depending on the amount of mismatch, an optimal degree of redundancy can be found that maximizes post-calibration performance. The figure presents the average and distribution of the calibrated results. It can be observed that

Fig. 3. LSB mismatch σ value effect on ENOB and ENOB spread for calibrated 14 cycle converters of different radices

TABLE I
SPREAD OF CALIBRATED ENOB FOR DIFFERENT RADIX CONVERTERS AND σ , 14 CYCLES

σ	Radix				
	2	1.96	1.9	1.86	1.76
.05	.31	.04	.05	.05	.05
.07	.36	.04	.06	.06	.06
.15	.56	.06	.06	.09	.08
.2	.6	.07	.08	.1	.1
.3	.56	.14	.12	.17	.12

the standard deviation of the calibrated values is much lower when redundancy is present.

Table I shows the effect that different σ have on the calibrated spread values. The spread of the binary converter is much larger than the rest of the converters. Interesting to note is that the spread of all other converters is very similar, even the ones with little redundancy. However, even though the spread remains similar, it can be seen in Fig. 3 that performance drops faster as mismatch increases when redundancy is smaller.

B. Adding dynamic effects to calibration

Fig. 4 shows the effect of redundancy in SAR calibration under noise, static and dynamic impairments for converters with different number of conversion steps. Each point in the curve represents the average of a hundred Monte Carlo simulations for a given conversion step period T_{cs} . The x-axis presents the ratio between T_{cs} and the MSB capacitor's settling time τ . For every array, there is a certain tolerance to decreasing T_{cs} , before performance drops drastically. Up until this point calibration works as expected, and after it both calibrated and uncalibrated ENOB values plummet, and calibration is no longer effective. Figs. 4a and 4b show different converters of 9 and 14 steps respectively. The performance up to where the binary converter starts failing ($T_{cs} \approx 6\tau$) is very similar to the static analysis done in Section IV-A. The results however show clear benefits of redundancy beyond this point. Increasing amounts of redundancy allow to operate with shorter settling times, this comes with a decrease in

Fig. 4. Effect of various step conversion period values (in # of MSB τ 's) before and after calibration for $\sigma = 0.3$.

TABLE II
REDUNDANCY AND NUMBER OF CYCLES NECESSARY FOR A 12 BIT ADC
WITH 99.7% CONFIDENCE

σ	N cycles	Min radix [7]	N cycles	Min radix This work	Max radix
0	12	2	12	2	2
.05	14	1.86	13	1.91	1.99
.1	15	1.75	13	1.92	1.96
.15	17	1.66	14	1.87	1.98
.2	18	1.59	14	1.91	1.95

maximum ENOB performance. Hence a trade-off between performance (ENOB) and power consumption (settling time) is achievable by playing with the amount of redundancy added. Fig. 4a shows that this trade-off becomes more notorious as the number of bits of the converter increases. Fig. 4c shows what happens if C_T of an 11 bit converter is sized so the noise floor is at 10 bits. Calibrated ENOB clips at 10 bits for the binary converter, and as it is now noise limited instead of mismatch limited the spread of its calibrated ENOB decreases. In the previous experiments the effect that calibration has on reducing the spread of the calibrated values due to static errors and the resilience it adds to dynamic errors was shown. Table II presents a summary of the minimum and maximum redundancy for the minimal number of cycles needed to reach 12-bit ENOB with a confidence of 99.7% after calibration. By choosing the maximum redundancy allowed, the target ENOB is reached while keeping the highest resilience against dynamic errors possible. This table also compares with the analytical values presented in [7]. This analytical approach seems to be too constrictive, as no missing levels are allowed in the DAC transfer curve. Simulations show that even when missing levels in the DAC occur the desired ENOB can be achieved with three standard deviations, relaxing the needed redundancy and number of SAR cycles.

V. CONCLUSION

By using a configurable SAR ADC model a thorough assessment of the effects that redundancy has on the calibration of static non-idealities taking noise and settling errors into account. It was shown that by adding redundancy the calibrated ENOB of Monte Carlo simulations has a much

lower spread for sub-binary converters than for a binary one with the same number of conversion steps, the tolerance to settling errors increase, while the maximal achievable ENOB decreases depending on the amount of mismatch. With these results an optimum level of redundancy can be found for a particular SAR design, depending on the expected mismatch and the timing constraints of the design. In general, even a little amount of redundancy can greatly reduce the spread of the calibrated results. If the expected mismatch is large, redundancy can provide the same or higher calibrated ENOB than a binary converter with the same number of conversion steps, even though their ideal ENOB values differ.

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