Fast Switch Bootstrapping for GS/s High-Resolution Analog-to-Digital Converter

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***Abstract*—This paper presents a novel bootstrapped switch to serve as an input frontend for high resolution ADCs operating in the GHz frequency range. The switch reduces the on-resistance value and keeps it constant, resulting in precise sampling of input signals and better tracking bandwidth. The proposed bootstrapped switch is designed and simulated in TSMC 28 nm Digital CMOS. Simulation results at 800 MSamples/s show an improved and relatively constant spurious-free dynamic range (SFDR) and total harmonic distortion (THD) up to an input frequency of 1.6 GHz, which makes it suitable for a Time-Interleaved configuration.**

Keywords*—Analog-to-Digital converter, bootstrapped switch, high speed, high linearity.

I. Introduction

Sampling of the time-varying input signal is the first step in any type of Analog-to-Digital (A/D) converter. For high resolution A/D converters operating in the GHz frequency range, a high performance Sample-and-Hold (S/H) circuit is needed as its frontend component. The linearity of the frontend S/H circuit directly impacts the linearity, and consequently, the total performance of the ADC. High performance S/H circuits are usually implemented as discrete-time, often Switched Capacitor (SC) circuits. The performance of a S/H circuit is usually limited by the performance of the input switch. Sampling switch non-linearity is mainly attributed to the non-linear signal dependent on-resistance and associated parasitic capacitance which produce harmonic distortion when sampling high frequency signals.

To address the aforementioned issues, Abo and Gray introduced a bootstrapped switch [1]. This innovative structure makes V_{GS} relatively constant, which reduces the on-resistance modulation, increasing S/H's linearity. With the increased demand for high speed high resolution ADCs though, the conventional bootstrapped switch has reached its limitations in terms of sampling linearity, as well as turn-on/off times, especially when operating at full swing range. Several methods have been proposed to further improve linearity [2], [3], [4], [5], [6]. Although these methods can be helpful, they have either limited input bandwidth or introduce increased design complexity. Furthermore, not much attention is paid to the reliability of the transistors composing the bootstrap loop, mainly due to the fact that these designs employ a non-full swing input voltage.

Bottom-plate sampling [7] in the GHz frequency range requires a short tracking time and an even shorter turn-off time, because a bootstrapped switch on the summing node has to define the tracking instant and turn off completely before the one on the top-plate of the capacitor turns off. Furthermore, widely used passive sampling networks, without sample-and-hold amplifier, require fast bootstrapped switches to track the input signal.

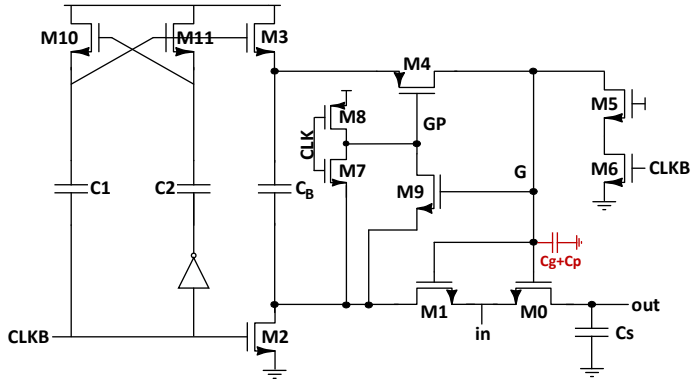

Fig. 1. Conventional bootstrapped switch [1].

This work presents an improved bootstrapped switch to be used in a GHz range Time-Interleaved (TI) ADC. The proposed structure reduces the turn-on time by keeping a lower and more constant on-resistance than the conventional design while turn-off time is slightly improved by reducing the parasitic capacitance on the critical nodes. Thus, sampling linearity at high frequencies is improved.

The remainder of this paper is structured as follows. The conventional bootstrapped switch and its limitations are analyzed in section II. Section III introduces the improved architecture proposed in this work, followed by simulation results in section IV. Finally, conclusions are drawn in section V.

II. Conventional Bootstrapped Switch

The conventional bootstrapped switch introduced by Abo and Gray [1], is shown in Fig. 1. During HOLD phase, CLK is low and V_{DD} is applied across the bootstrap capacitor C_B through switches M2 and M3. At the same time M5 and M6 discharge the gate of M0 to ground, keeping the switch off.

During TRACK phase, the pre-charged C_B acts as a battery across the gate and source of M0, bootstrapping it to V_{DD}. In this way, V_{GS} of M0 is kept constant, therefore rendering a constant on-resistance regardless of the input signal. M5 is

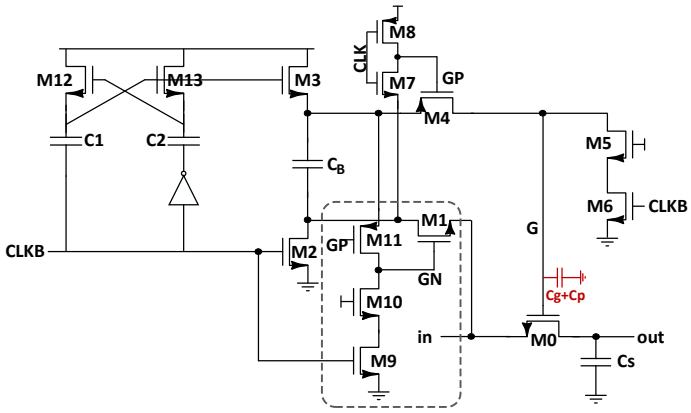

Fig. 2. Proposed bootstrapped switch.

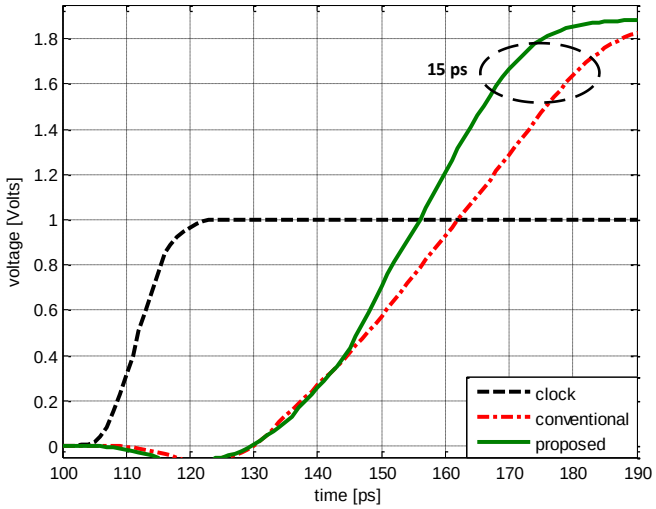

Fig. 3. Overdrive of M0 for both conventional and proposed switch.

added for reliability reasons, to relax the voltage pressure over M6, which can go up to 2*V_{DD}. However, charge sharing occurs due to parasitic capacitance of M1, M4, M5, M6 and M9, which makes V_{GS} less than V_{DD}. In this topology, the rise time of G is determined by the time constant of the bootstrap loop $(M1{-}C_B{-}M4)$, given by the series of C_B and $C_G{+}C_P$ and the values of on-resistors R_{M1} and R_{M4}. C_G is the switch gate load and C_P is the total parasitic capacitance on that node. The time constant can be expressed as:

$$\tau_{bootstrap} = (R_{M1} + R_{M4})\frac{C_B(C_G + C_P)}{C_B + C_G + C_P} \qquad (1)$$

At the initial phase of the TRACK transient, M7 turns on and GP, the gate voltage of M4, is pulled down to ground. Consequently, M4 begins to turn on and brings up node G. Before G assumes a sufficiently large value to fully turn on M1, M4 dictates the current flowing from C_B to charge node G. The slowly rising G defines the on-resistance of M1, which influences how quickly G rises to accurately track the signal. Increasing M4 does not make the transient fast enough and introduces more parasitics. This mechanism in combination with a large C_B, which is needed to avoid loss of overdrive, at the beginning of the bootstrapping phase, and the associated parasitics (a) limits the switch bandwidth and modulates M0 on-impedance for a significant portion of the tracking phase, and (b) limits the bootstrap bandwidth causing loss of sampling linearity at high frequencies. It would be desirable to have a very fast internal bootstrap loop, able to track the signal in a much shorter time than the tracking time, therefore avoiding the aforementioned drawbacks.

III. Proposed Bootstrapped Switch

The transistor level implementation of the proposed bootstrapped switch is shown in Fig. 2 with its key changes in a gray dashed box. Compared to the conventional circuit, M9 is removed from the main bootstrap loop and M1 is disconnected from node G. Instead, transistors M9-M11 are added to control the switching sequence of M1. The other transistors and capacitors are the same as the structure in Fig. 1.

At the beginning of TRACK phase when CLK goes high, M7 turns on and immediately turns on M11, each of them pulling nodes GP and GN to ground and V_{DD} respectively almost simultaneously. Consequently, M1 and M4 both start immediately conducting with a constant gate-source voltage and thus low and constant on-resistance through the whole input range. Therefore, node G rises quickly to track the input signal, reducing significantly the modulation of M0 on-impedance. Furthermore, removing M9 from the conventional design and decoupling M1 from node G removes their parasitic capacitance contribution on that node, further improving the rise transient.

During HOLD phase, G is discharged similarly to the conventional case, with the difference that M5 and M6 can be smaller for the same slope, which is the third contributor to the shorter turn-on time. Node GN is discharged through M9-M10 instead of loading M5-M6 with one more gate load. M10 is added for reliability reasons, to relax the voltage pressure on M9. Since the speed on the falling edge of this node is not as critical as of node G, the discharging transistors can be sized just as big as required to keep GN smaller or equal to a threshold voltage above zero. With a threshold voltage of around 350 mV, these transistors can be more than a factor of ten smaller than the main discharging transistors M5, M6. Considering the fact that all transistors can be sized smaller than the conventional case due to faster internal bootstrap loop, the proposed mechanism provides a better overall performance without increasing the area of the sampling switch.

IV. Simulation Results

The proposed bootstrapped switch has been designed and simulated in TSMC 28 nm Digital CMOS process. The nominal power supply voltage is 1 V. Since the target is to use this switch as the frontend of an ADC, differential configuration performance is considered in all the following results. A sine-wave with 2 V_{pp} differential swing and frequencies from 6 MHz up to 1.6 GHz is applied to both conventional and proposed bootstrapped design. The input signal is sampled at 800 MHz and one fourth of the sampling period is allocated for tracking (3.2 GHz). The capacitive load is determined based on the noise requirements of the total ADC and set to 450 fF.

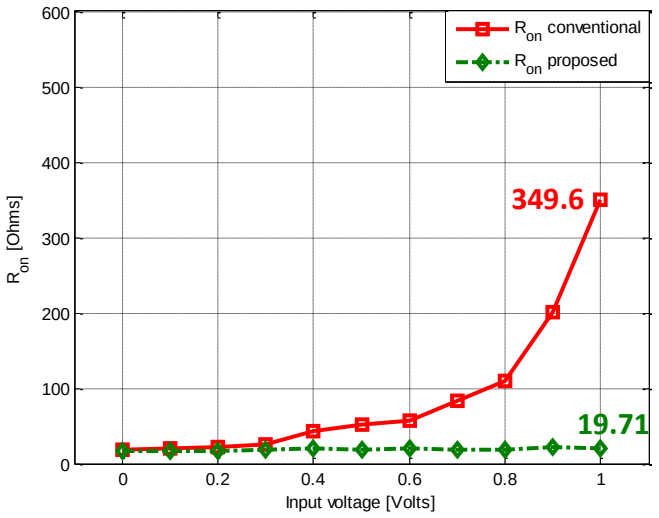

Fig. 4. Simulated on-resistance for both conventional and proposed switch.

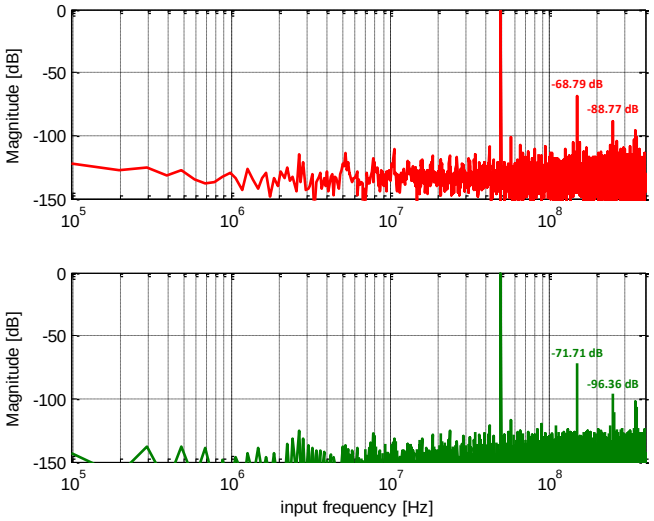

Fig. 5. Output spectrum of conventional (top) and proposed (bottom) switch for $f_{in} = 49.5\ MHz$, $f_s = 800\ MS/s$.

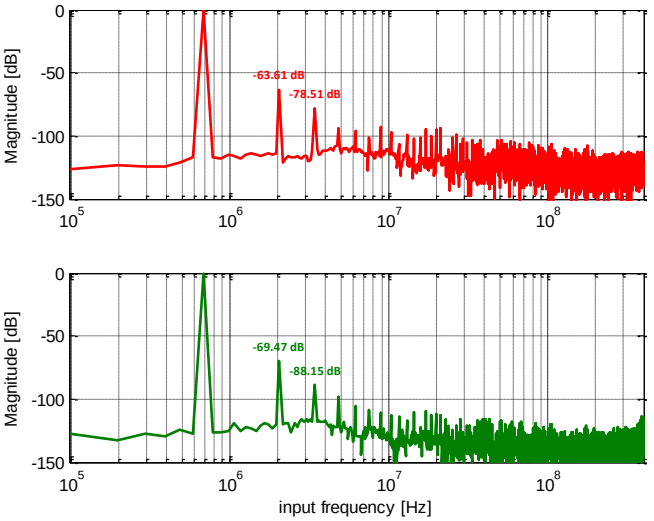

Fig. 6. Output spectrum of conventional (top) and proposed (bottom) switch for $f_{in} = 1.59\ GHz$ (folded), $f_s = 800\ MS/s$.

The capacitor's value and the allocated tracking time require an on-resistance value of smaller than 50 Ω for sufficient settling accuracy.

Fig. 3 shows with a green solid line the overdrive voltage of the sampling switch in the proposed design and with a red dotted-dashed line shows the equivalent overdrive in the conventional design, while sampling a maximum input voltage of V_{DD}. As explained previously, the rise time of the proposed switch is shorter than the conventional, yielding smaller on-resistance and constant during a larger amount of the tracking period.

Fig. 4 compares the performance, in terms of on-resistance, for both the conventional and the proposed bootstrap switch for a voltage range from zero to full scale. As seen, the on-resistance of the conventional switch is modulated quite significantly for input voltages above 400 mV. The main reason for this is that the track transient is not fast enough to reach the full value of the input voltage, therefore yielding smaller overdrive voltage, thus higher on-resistance. For the proposed switch this is not the case, and the on-resistance of the main switch remains at levels of below 20 Ω across the whole input range, meeting the aforementioned estimated requirements.

The coherently FFT-processed output spectrum of both the conventional and the proposed design is shown in Fig. 5 and Fig. 6 for input frequencies of 50 MHz and 1.6 GHz respectively and an amplitude of 2 $V_{pp,diff}$. Even order harmonics are canceled due to differential structure and as expected, HD3 is the dominant performance limiting harmonic tone. Table I summarizes the performance results and compares them with a reference design.

Finally, the dynamic performance in terms of THD for both bootstrapped switches is shown in Fig. 7 for input frequencies up to 1.6 GHz (4^{th} Nyquist zone), at a sample rate of 800 MS/s. The proposed switch maintains a linearity of better than 11 bits (71 dB) up to the first Nyquist zone (400 MHz), while THD drops by only 2 dB up to the 4^{th} Nyquist zone. The conventional switch on the other hand, shows a degradation as input frequency increases, which is attributed to its limitation

TABLE I. HARMONIC DISTORTION

Design	THD	SFDR	Reliability
ref [5] @ $f_{in} = 100MHz$ $f_s = 1GHz$	-65dB	N/A	preserved
conventional @ $f_{in} = 1.6GHz$ $f_s = 800MHz$	-63.2dB	63.61	preserved
proposed @ $f_{in} = 50MHz$ $f_s = 800MHz$	-71.4dB	71.71	preserved
proposed @ $f_{in} = 1.6GHz$ $f_s = 800MHz$	-69.3dB	69.47	preserved

to handle the full input bandwidth during tracking phase. The flatness in THD of the proposed switch renders it capable of being used in a Time-Interleaved ADC with $>$ 1 GHz bandwidth requirement.

Table II summarizes the simulation results of the proposed bootstrapped switch.

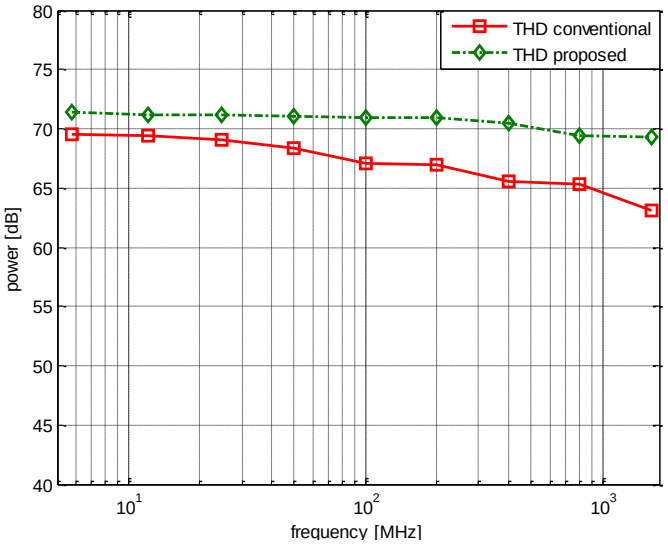

Fig. 7. Dynamic performance versus input frequency.

TABLE II. PERFORMANCE SUMMARY

Process	28 nm Digital CMOS
Supply	1 V
Input	2 $V_{pp,diff}$
Sample rate	800MS/s
3dB input bandwidth	>4GHz
SFDR @ 1^{st} Nyq. zone	71.09dB
THD @ 1^{st} Nyq. zone	-71dB
SFDR @ 4^{th} Nyq. zone	69.47dB
THD @ 4^{th} Nyq. zone	-69.3dB

V. CONCLUSION

A novel fast bootstrapped switch capable of operating with a very low and constant on-resistance has been presented. The switch is intended to be used in GS/s high resolution ADCs. The better performance is obtained changing the main bootstrap loop mechanism, thus reducing the parasitic capacitance on the most critical nodes which results in higher tracking bandwidth and better linearity especially at GHz input frequencies. Finally, the performance improvement is achieved with no additional area and power, while ensuring reliability of all devices.

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