30.2 Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption

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The efficiency of small-molecule OLED devices increased substantially in recent years, creating opportunities for power-efficient displays, as only light is generated proportional to the subpixel intensity. However, current active matrix OLED (AMOLED) displays on foil do not validate this power-efficient advantage, as too much power is lost in the AM backplane. AMOLED displays use the analog voltage on the gate of a drive transistor (e.g. M1 in Fig. 30.2.1) to control the pixel current and hence the pixel brightness. Accurate and uniform pixel currents can only be obtained when transistor M1 is driven is saturation. In high-resolution technologies on foil, transistor parameters W, L and the mobility μ are limited by technology, imposing a minimal V_{GS}–V_T to obtain sufficient current, i.e. V_{GS}–V_T > 4V for a-IGZO on foil [1]. Subsequently, to obtain saturation, V_{DS} > 4V, which translates in a static backplane power loss surpassing the OLED power consumption (see red stars in Fig 30.2.1). However, when the OLED pixel impedance around a specific reference current can be matched along a display column line, the accurate pixel current control can be imposed by current DACs implemented in external silicon display column drivers. In this work, we operate M1 as a switch and pixel intensity variations are obtained using Pulse Width Modulation (PWM) of a predefined pixel current, i.e. 2μA/pixel [80*80μm^2] (which corresponds in our OLED technology to a light output of 2000Cd/m^2). When, in a future implementation the external DACs are calibrated at 0.2μA/pixel, the full brightness would correspond to the typical display brightness of a portable PC, i.e. 200Cd/m^2. This concept enables us to reduce the display power voltage at full brightness from 8.2V in a classical AMOLED display on foil configuration to 5V (measured) and for future implementations even down to 4V (see Fig. 30.2.1). As the OLED current load remains equal, a corresponding static power reduction of the display (and increased battery lifetime) is obtained. Digital driving methods of AMOLED displays have been shown before. However, ΔΣ techniques [2] still integrate charge packets on the gate of M1 and hence do not solve the power issue on foil. Other PWM techniques [3] activate only a single active line in the linedriver yielding difficulties to obtain color depths above 6 bits. When multiple independent linedrivers are implemented and their output is multiplexed to alternately drive a single select line, a higher color depth can be obtained [4]. This leads however to a bulky linedriver, which is hard to get within an e.g. 80μm pitch. The design and implementation of a compact integrated linedriver on foil enabling multiple alternating active signals through a single shift register is demonstrated here.

To demonstrate the functionality of the select linedriver, it has been integrated in a small high-resolution red half-QQVGA display on PEN foil (64*160 pixels@80*80μm^2, 0.54 inch diagonal]. It comprises 22352 a-IGZO transistors, from which 1872 in the linedriver (see Fig. 30.2.2). Externally, the display is driven as a 64*320 pixel display. An etch-stop-layer stack is used to fabricate the a-IGZO backplane and a red small-molecule top-emitting OLED stack (at 2.6Cd/A) is evaporated on top. Devices are realized on top of PEN foil including top and bottom moisture barrier. The dedicated linedriver can be decompiled in 16 blocks, each comprising 10 linedrivers (see Fig. 30.2.2, bottom).

In order to obtain an 8b PWM at a duty cycle of almost 100%, we have split each frame into 8 subframes and during the first 7 subframes, the select lines are driven twice, with a fixed delay between drive cycles. This delay is alternated each subframe (see table Fig. 30.2.3). Figure 30.2.3 shows the pulses on a set of select lines during the first subframe. In the first subframe, the n-th select line is driven a second time after the n+10-th select line is driven for the first time. We implemented a dedicated single shift register with a 3-clocking scheme. Each 10 lines, the clocking scheme is rotated and the select line is driven on a different clock (see green dashed line in Fig. 30.2.3) to prevent that two select lines are driven at the same time.

Each time a select line is driven, M1 of Fig. 30.2.1 is switched on or off. This is done according to the table in Fig. 30.2.4, for an 8b pixel intensity equal to $b_{7..0}$ [4]. Figure 30.2.4 also shows the on-off switching of a pixel during the driving of 1 full frame (8 subframes) when the pixel intensity is 10011001. This implementation enables almost a 100% duty cycle. The table in Fig. 30.2.4 can be extended to 16b color depth when applied to larger size display. The table in Fig. 30.2.4 shows that subframes are scheduled with increasing delay between both moments the select lines are driven. This, combined with the fact that the select lines during the last subframe are only driven once, avoids overlap between subframes and enables driving at almost 100% duty cycle. As the backplane only comprises n-type a-IGZO transistors, we also designed the integrated linedrivers in unipolar n-type logic. In n-type logic, it is typically challenging to obtain short rise times for charging large capacitances, such as the select lines of a display. Recently reported techniques, such as bootstrapping enable fast rise times in unipolar technologies [5]. The top of Fig. 30.2.5 shows the schematic of the 3-phase clocked linedriver, comprising 2 clocked inverting stages and 1 bootstrapped stage. The overlap capacitance between the gate and source of M9 (510fF) acts as bootstrap capacitance, so no dedicated bootstrap capacitance has been added in the layout. To enable that a single shift register drives alternating two select lines, spatially separated by a multitude of 10 lines, the clocking scheme is rotated each 10 lines amongst the 3 clocks. As an interface between blocks operated with a specific clock scheme, we designed a 2-clock phase delay linedriver, which is inserted each 10 select lines to cycle the clock phase. It is comprised of two bootstrapped stages (see Fig. 30.2.5, bottom)

A copy of the linedriver has also been instantiated on the same foil to enable electrical characterization (see bottom of Fig. 30.2.7). Although the linedriver in the display is driven at 15V (and consuming less than 97μW) and at 200kHz clock speed, we explored the lowest voltage and highest clock frequency the linedriver continued to operate (see Shmoo plot of select line 157 in Fig. 30.2.6). Figure 30.2.6 shows also the select line 4, 10 and 157 voltage pulses when driven at 9V and 240kHz and loaded with the 0.1pF input capacitance and 1MΩ input resistance of a Picoprobe (model 12C from GGB industries). We notice correct timing, but the select line amplitude gets only to within 4V of the rail voltage. This is partially due to the Picoprobe load and partially due to the slew rate.

Finally, Fig. 30.2.7 shows at the top some images from the digital PWM-driven 320 ppi AMOLED display on flex operated at 200 subframes per second. Each display column is driven by a current DAC (DAC902 from TI), driving a multiple of 2μA. Five Xilinx FPGAs send the image data to these 64 current DACs and the data lines. The all-pixels fully-on static power consumption of this digital driven backplane is: 160*64*2μA*5V = 102.4mW, whereas the corresponding classic driving method would have consumed 168mW. As both data lines and select lines are driven at a higher rate, the dynamic power increases. Data lines are driven with 10V swing and have a capacitive load of 9.3pF each, select lines are driven with 15V swing and have a capacitive load of 5.6pF. The dynamic driving power at 30 frames/s increases as a consequence to a maximum of 2.5mW. The overall energy consumption for this digital driving implementation is 62% of the energy consumption of its analog counterpart. Finally, digital driving of AMOLED displays does not need to be restricted to only displays on foil, as digital driving also opens a whole set of other advantages, similar to the introduction of DLP for projection displays.

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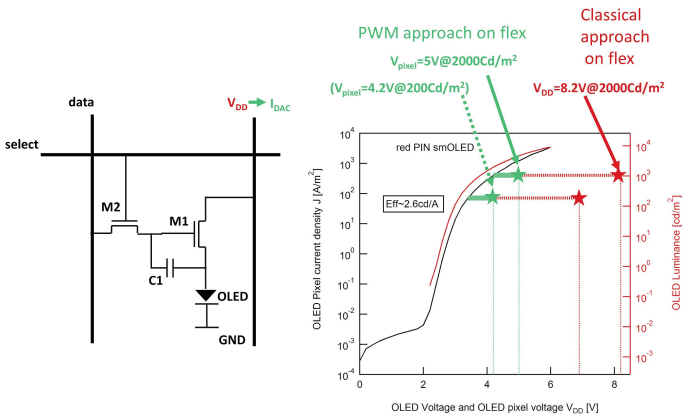


Figure 30.2.1: (left) 2T1C AMOLED pixel schematic, in which M1 can act as current control element or as a switch. (right) Current density-voltage and luminance-voltage characteristics of our red OLEDs. The overall pixel voltage drop is also indicated.

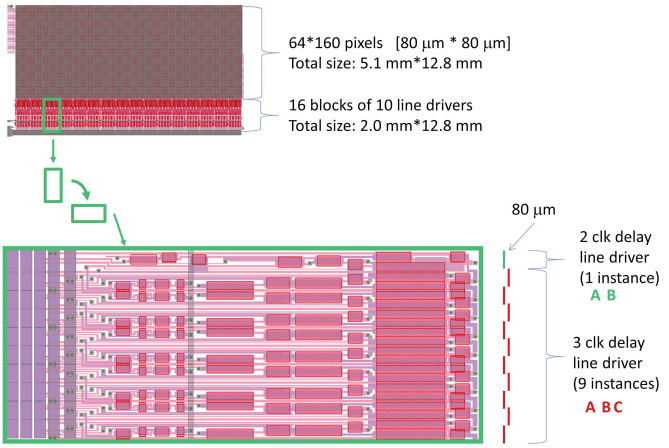
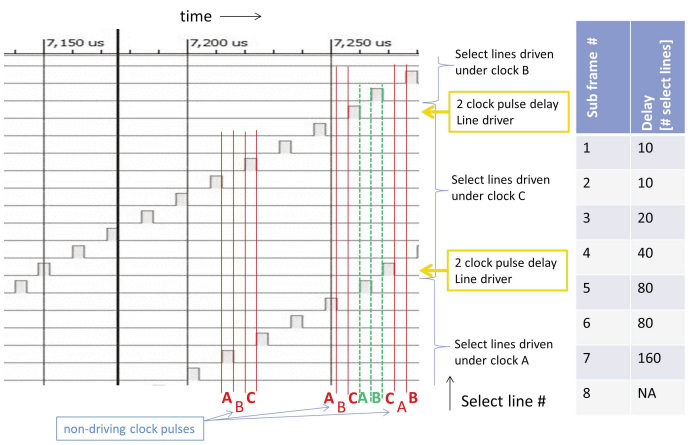


Figure 30.2.2: (top) Lay-out of the 320dpi a-IGZO AMOLED for digital PWM driving comprising the integrated line driver. (bottom) Block of 10 line drivers, each with 80µm pitch. A 5µm design rule is used.



Sub frame #	Delay [# select lines]
1	10
2	10
3	20
4	40
5	80
6	80
7	160
8	NA

Figure 30.2.3: Subsequent select lines driven by the clocks A, B and C. Every 10 select lines, a non-driving clock pulse is skipped. This enables the shift of two active signals through the line driver, without simultaneous driving of a select line. The table indicates the delay of the select lines.

Subframe number (part α β)	bit driven after the first select line is active	bit driven after the second select line is active
1 (10, 310)	0	b_7
2 (10, 310)	b_0	b_7
3 (20, 300)	b_1	b_7
4 (40, 280)	b_2	b_7
5 (80, 240)	b_3	b_6
6 (80, 240)	b_7	b_6
7 (160, 160)	b_4	b_6
8 (320, /)	b_5	/

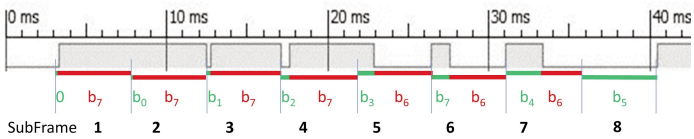


Figure 30.2.4: (top) Encoding table for the eight bit number b7..0, which ensures accurate pixel intensity control. (bottom) Encoding applied for 1 frame, i.e. 8 subframes for the binary number 10011001. The frame rate is 25 frames/s.

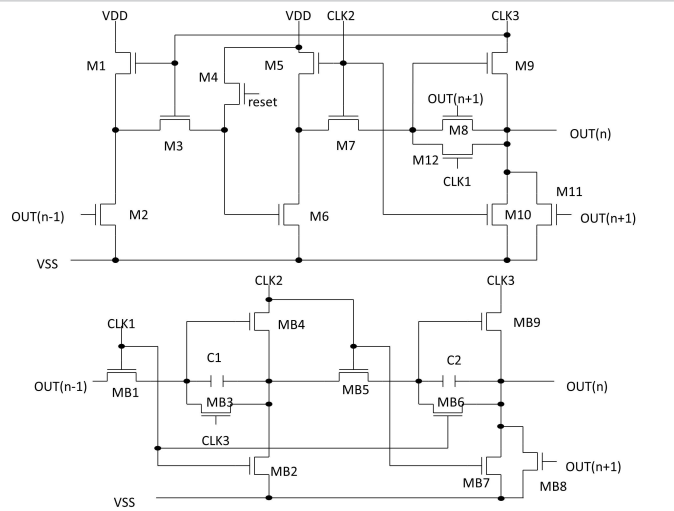


Figure 30.2.5: (top) Line driver schematic with a delay of 3 clock pulses. (bottom) Line driver schematic with a delay of 2 clock pulses to allow a skip of one cycle when going to the next block of 10 line drivers.

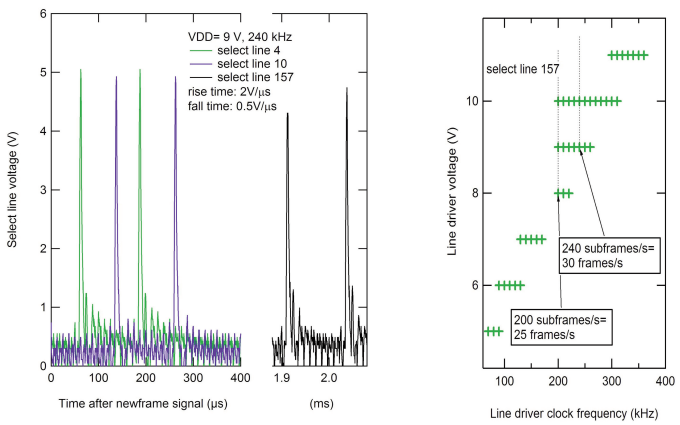


Figure 30.2.6: (left) Picoprobe measurements of the select line signals in the first subframe. (right) Shmoo plot of the select line 157 signal illustrating the line driver voltage versus the line driver clock frequency.

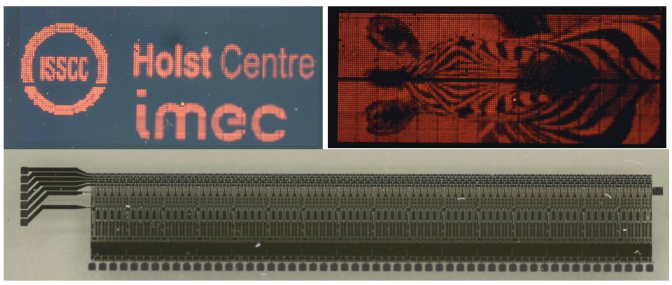


Figure 30.2.7: (top) Photographs of the PWM 64*160 AMOLED display on foil with embedded line driver in the a-IGZO backplane. (bottom) Micrograph of the separated line driver on the same foil (for testing). Only select lines numbered 3n+1 have a bonding pad.

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