Interpretation of frequency dependent capacitance-voltage curves of amorphous Indium Gallium Zinc Oxide (a-IGZO) thin film transistors

Ajay Bhoolokam [a,b], _Manoj Nag_ [a,b], _Adrian Chasin_, _Soeren Steudel_ [a], _Jan Genoe_ [a,b], _Gerwin Gelinck_ [c], _Guido Groeseneken_ [a,b] _and Paul Heremans_ [a,b]
[a]**imec, Kapeldreef 75, 3001 Leuven, Belgium.** *Tel: +32 16 28 76 47, E-mail: ajay.bhoolokam@imec.be*
[b]**ESAT, Katholieke Universiteit Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium.**
[c]**Holst Centre, High Tech Campus 31, 5656 AE Eindhoven, The Netherlands.**

The subgap trap states which are inherent in a-IGZO TFTs, due to the disordered nature of the material, play a key role in determining the electrical characteristics of the TFT. Multi-frequency capacitance voltage (CV) method [1-2] is one of the techniques used to obtain information about the trap states. The technique works on the assumption that the frequency dispersion in CV curves is caused due to trap charges.

In this study we show that the resistance of a-IGZO channel is the dominant reason for frequency dispersion of CV measurements on a-IGZO transistors. The effect can be modeled with a transmission line model (TLM) and is shown to fit for all channel lengths. So extraction of the subgap trap density from the frequency dependence of CV measurements should be done with great care. Fig 1 (a) and (b) show the CV characteristics of 2 TFTs in the frequency range of 250Hz to 1MHz. The channel length is 50 and 250 µm. As the channel length increases, the amount of capacitance change also increases. If only the trap states were the cause for frequency response there should not have been a channel length dependency. The presence of this dependency strongly supports the need of TLM for dispersion analysis. From [3] for TLM analysis we get,

$$C = C_{MIS} * \left[\frac{\sinh(\zeta)+\sin(\zeta)}{\zeta.(\cosh(\zeta)+\cos(\zeta))}\right] \quad \ldots\ldots (1) \qquad G = \omega * C_{MIS} * \left[\frac{\sinh(\zeta)-\sin(\zeta)}{\zeta.(\cosh(\zeta)+\cos(\zeta))}\right] \quad \ldots\ldots (2)$$

Where $\zeta = \sqrt{\omega C_{MIS}/2G_{ch}}$, G_{ch} is conductance of the RC network. $C_{MIS} = \frac{C_{OX}C_{SC}}{C_{OX}+C_{SC}}$, $C_{OX} = C_{ox}'*W*L$ and $C_{SC} = C_{sc}'*W*L$, C_{sc}' and C_{ox}' is the semiconductor and oxide capacitance per unit area. The capacitance values at different voltages as a function of frequency is show in Fig. 1(c) along with fits to equation (2) for L = 50 µm. The extracted G_{ch} is compared with the conductance value obtained from DC I_{ds}-V_{gs} measurements (G_{meas}) by calculating $I_{ds}/V_{ds.}$ There can be three contributions to G_{ch}. One from voltage dependent contact resistance, another from channel resistance and lastly from charging and discharging of traps. Transfer line method was used to check the importance of contact resistance and was found to be negligible. As G_{meas} is equal to G_{ch} the impact of trap states is masked by the impact of channel conductance, because if the conductance related to trap states was comparable to the channel conductance the extracted G_{ch} value would be lower than G_{meas}.

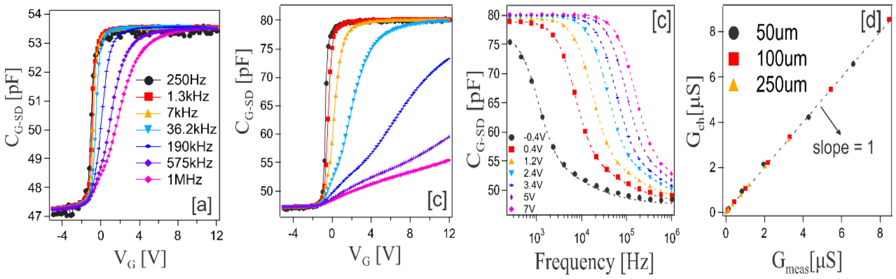

Fig. 1: CV characteristics as a function of frequency for TFTs with channel length of 50 µm [a] and 250 µm [b]. Legend is same for [a] and [b]. Capacitance values at different voltages as a function of frequency for TFTs with channel length of 250 µm [c].Measured and extracted G_{ch} values [d]. Dotted line has a slope of 1.

Acknowledgement

This work was carried out at imec, Belgium and Holst Centre, Netherlands.

References

1. Sangwon Lee, Sungwook Park, Sungchul Kim, Yongwoo Jeon, Kichan Jeon, Jun-Hyun Park, Jaechul Park, Ihun Song, Chang Jung Kim, Youngsoo Park, Dong Myong Kim, and Dae Hwan Kim, *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 231-233, Mar. 2010
2. Hagyoul Bae, Sungwoo Jun, Choon Hyeong Jo, Hyunjun Choi, Jaewook Lee, Yun Hyeok Kim, Seonwook Hwang, Hyun Kwang Jeong, Inseok Hur, Woojoon Kim, Daeyoun Yun, Euiyeon Hong, Hyojoon Seo, Dae Hwan Kim, and Dong Myong Kim, *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1138-1140, Aug. 2012
3. Jong S. Choi, and Gerold W. Neudeck, *IEEE Electron Device Lett.*, vol 39, no 11, pp. 2515-2522, Nov. 1992