A 6-b UWB Subsampling Track & Hold with 5.5-GHz ERBW in 40 nm CMOS

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***Abstract* — This paper presents an ultra wideband track and hold (T/H) circuit using direct RF subsampling for radar applications. The circuit enables digitization of the whole received UWB pulse instead of a sole distance measurement used in correlating receivers. In this way, more target information is acquired for further digital processing. Subsampling was applied to achieve a low power concumption of 1.4 mW which includes the T/H core and clock generator. The circuit operates on a rail-to-rail input using the bootstrapping technique. To avoid reliability issues caused by bootstrapping the sampling switch, bulk switching and precharge techniques are introduced. An effective resolution bandwidth of 5.5-GHz was measured with an accuracy of 6-b. The track and hold circuit has been implemented in 40 nm CMOS.**

***Index Terms* — CMOS integrated circuits, Ultra wideband radar, track and hold.**

I. Introduction

Ultra wideband signals in the 3.1-10.6 GHz range have been proposed for a vast amount industrial and medical applications [1]. Common targeted applications include the investigation of steel reinforcement in concrete, ground penetrating radar (GPR), wireless measurement of heart beat and respiration rate [2] or the detection of breast cancer. To allow a low cost implementation for these applications, this paper presents a high bandwidth subsampling track and hold (T/H) circuit. The subsampling technique, also referred to as equivalent time sampling (ETS), can be justified for radar applications where signals are sampled at a rate slightly different from the pulse repetition rate [3] to relax the analog to digital converter (ADC) in terms of throughput and bandwidth. However, the T/H circuit must still be able to cope with the full RF bandwidth at the input. This can be achieved by designing the circuit with a large switch transistor or a small hold capacitor. This choice affects both linearity and noise floor. For high SNR it is important that the T/H works rail-to-rail. An additional challenge in deep-submicron technologies due to scaling is the decreasing voltage headroom. For this reason the T/H core uses bootstrapping and the operational amplifiers are designed with complementairy input pairs. However by introducing the bootstrapping technique without taking any other precautions, the reliability of the sampling switch is not guaranteed. Compared to previous work [4], [5], [6], we propose two techniques: bulk switching and precharging, to keep the voltages between two terminals of the sampling switch lower than V_{dd} at all times.

This paper is organized as follows. Section II explains the operation of the system architecture. The T/H core is discussed in section III and measurement results are shown in section IV.

II. System architecture

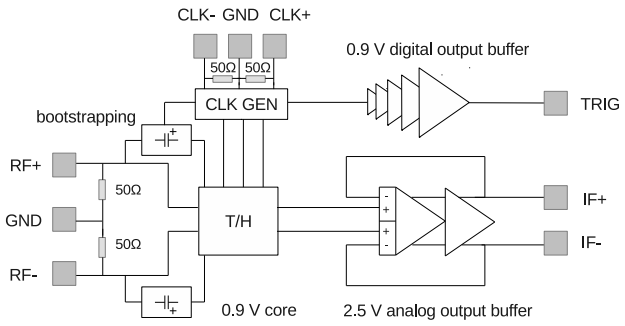

Fig. 1. System level architecture of the UWB T/H chip

The system representation of the UWB subsampler is shown in Fig. 1. The RF signal is applied differentially for a better power supply rejection ratio (PSRR), also eliminating droop on the hold capacitor and is terminated in 50 Ω resistors. Any DC biasing is avoided, using symmetrical supplies. To achieve high bandwidth and rail-to-rail operation, the bootstrapping technique is applied on the sampling switch. The on-chip multiphase clock generator derives 100 MHz output signals from a 1.6 GHz input sine wave. On-chip, the sine wave is converted to a square wave and divided 16 times before it drives several non-overlapping clock generators to control the T/H core. In order to trigger the oscilloscope for measurement purposes, a digital output buffer is included. The T/H core and digital logic both operate from a separate 0.9 V supply. Also for

measurement purposes, a 2-stage Miller compensated fully differential difference amplifier (FDDA) [7] is included operating on a 2.5 V supply. It operates in unity gain feedback. The 2-stage amplifier makes it possible to have both a small parasitic input capacitance and 50 Ω drive capability at the output.

III. Circuit Level Implementation

A. T/H core with multiphase clock signals

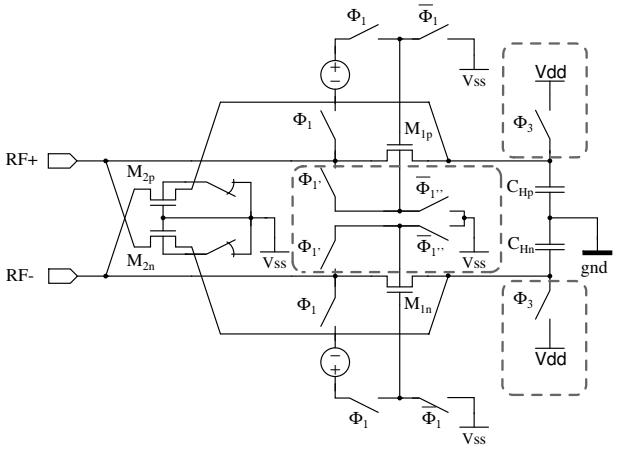

Fig. 2. Circuit level of the T/H core with bulk and precharge switches

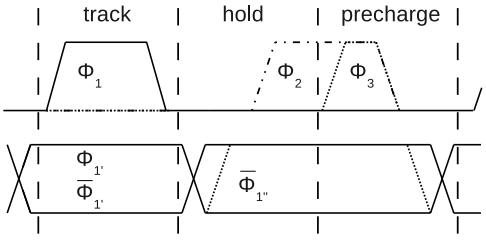

Fig. 3. Multiphase clock generator output

Fig. 2 represents the transistor level implementation of the T/H core. Transistors M1 are the sampling switches and M2 is always off but is used as RF feedthrough cancellation during the hold phase. These are implemented in a triple well technology. The bulk of M2 is connected to V_{SS} via the identical switch transistor for better matching. The hold capacitor C_H was chosen 65 fF, sufficiently higher than the parasitic input capacitance of the output buffer for linearity purposes. Bottom plate sampling is avoided here to achieve higher bandwidth. Three main switching phases can be seen in Fig. 3. During the track phase, switches ϕ_1 are closed and M1 operates in the linear region. Its V_{gs} now approaches V_{dd} due to bootstrapping. Clock signals ϕ_1' and $\overline{\phi_1'}$ are non-overlapping clock signals

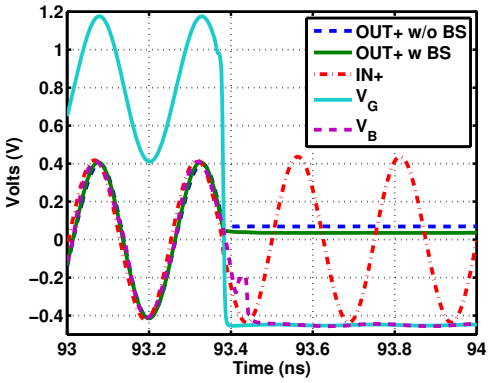

Fig. 4. Simulated voltages of the sampling transistor M_{1p}

with ϕ_1 and drive the CMOS transmission gate between the RF input and the bulk of the switch transistor. In the track phase, this switch is closed such that the body effect and its influence on V_T, and hence on R_{ON} is avoided. In both other phases, this transmission gate is open and the bulk of the sampling switch is connected to V_{ss} via $\overline{\phi_1''}$ for increased isolation between the RF input and the sampled value. The sampled signal at the output of the chip is discrete in time, but analog in value. It is digitized with an oscilloscope which is triggered with clock ϕ_2 and has its rising edge in the middle of the hold phase. A third precharge phase is included to further avoid reliability issues with the sampling switch. Assume the previous sampled value was V_{ss}, if the current input equals V_{dd}, the sampling transistor will have an instantaneous V_{gs} of twice the full supply voltage. By precharging the hold capacitor with ϕ_3 to V_{dd} before each track phase, this situation is avoided. The precharge switch can have small dimensions in the case of subsampling because there is more time for charging C_H. In this way, there is a minimal impact on the bandwidth.

B. Simulated performance using bulk switching

By introducing bootstrapping, the worst case V_{gb} is $2V_{dd}$ for a rail-to-rail input and if the bulk is connected to the lowest voltage. In order to keep every voltage between two transistor terminals smaller than V_{dd}, the bulk must be connected to the input. A possibility is to make a fixed connection but if we assume a sampled value of V_{ss}, then the bulk-source PN-junction can be forward biased during the hold phase resulting in a false discretization. For these reasons, we propose to switch the bulk between the input and V_{ss}. Fig. 4 depicts the simulated terminal voltages of the sampling switch during transition from track to hold phase. The importance of using non-overlapping clock signals can be clearly seen. First the gate voltage drops to V_{ss} before the bulk voltage. Otherwise the instantaneous

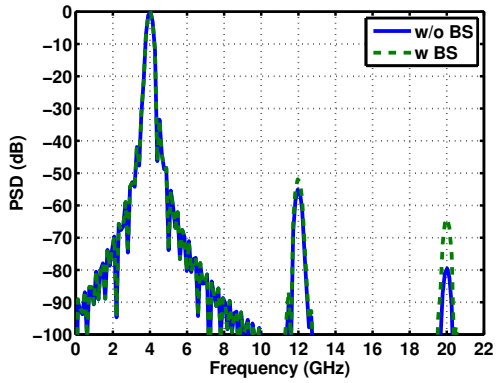

Fig. 5. Simulated spectra of the subsampled signal w/o and w bulk switching

V_{gb} is larger than the supply voltage. For the same reason, the bulk is connected first to the input before bootstrapping the gate at the start of the track phase. Although the switching of the bulk can be considered in the same way as clock feedthrough [8] using formula 1, simulations indicate that its impact can be neglected at 6-b accuracy. In the formula, V_{in} is the differential input signal and ΔV is the change in differential output.

$$\Delta V = \frac{C_{SB}}{C_{GS} + C_{SB} + C_H} V_{in} \tag{1}$$

Simulated spectra of the sampled signal are shown in Fig. 5 and indicate that the effect only becomes important if a resolution of around 8-b is targeted. Even if this resolution is targeted, the effect can be compensated in an analogous way as clock feedthrough compensation. However, this is at the cost of more paracitics and decreased bandwidth.

IV. Measurement Results

The presented rail-to-rail input UWB T/H circuit with analog and digital output buffers was fabricated using a 40 nm CMOS process. A micrograph of the chip is included in Fig. 6. Both the T/H core and multiphase clock generator consume 0.012 mm^2, the output buffers consume 0.020 mm^2. The total chip area also including bonding pads, termination resistors and decoupling capacitors results in 1.09 mm^2. For subsampling operation in all measurements, a small time offset t_{s_ET} of 4 ps is added to the internal sampling clock of 100 MHz. This implies a necesarry internal clock frequency of 99.96 MHz. Using equation 2, this results in an applied clock signal of 1.59936 GHz.

$$f_{CLK} = 16 \frac{1}{\frac{1}{f_s} + t_{s\_ET}} \tag{2}$$

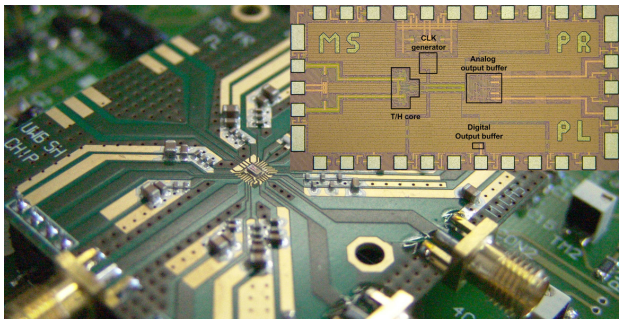

Fig. 6. Chip PCB and micrograph

The chip performance was characterized by sweeping the input frequency from 1 to 10 GHz while keeping the input power constant at 7 dBm. No de-embedding of the measurement setup was done. Fig. 7 depicts the measured SNDR (ENOB), SNR and SFDR. Up to 4 GHz, an ENOB of 6.3 bit and corresponding 39.6 dB of SNDR is achieved. At 5.5 GHz ERBW the ENOB is reduced to 5.8 bit or 36.6 dB SNDR. The T/H core power consumption is 0.2 mW, the digital frequency divider and clock generator consume 1.2 mW. The latter can be considered as a cost for low jitter specification because most power is disipated in the first stage of the divider operating at nearly 1.6 GHz. For measurement purposes, an aditional 3.8 mW and 69.2 mW are consumed in the digital and analog output buffers respectively.

For the proposed UWB application, an UWB gaussian pulse with a center frequency of 4.5 GHz and -10 dB bandwidth of 1.5 GHz was generated using an arbitrary waveform generator (AWG). This pulse was sampled using a real time sampling (RTS) oscilloscope at 50 Gs/s with 20 GHz bandwidth for comparison with the chip output at an ETS rate of 250 GHz. Both signals are shown in Fig. 8. The fidelity as given in equation 3 is used to evaluate the UWB pulse distortion due to the receiver chip. Therefore the pulse is compared to the actual transmitted pulse of the AWG and results in a fidelity of 99.5% indicating a good conservation of the pulse shape. As indicated in Fig. 8 there only exists an amplitude mismatch due to losses in the setup.

$$F = max\left(\int_{\tau=-\infty}^{\tau=\infty} x_{tx}(t) x_{rx}(t-\tau)\,\mathrm{d}t\right) \tag{3}$$

Different specifications are listed and compared to previously published subsampling T/H circuits in Table I. The FoM is calculated using $P/(2^{ENOB} f_s)$. For [4], only the power consumption of the analog part is taken into account for fair comparison. In [5], a time-interleaved 16 channel T/H is discussed. The referenced power consumption of the timing generator and T/H buffers is divided by 16,

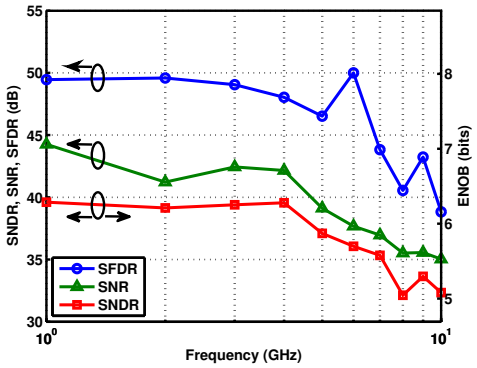

Fig. 7. Measured SNDR (ENOB), SNR and SFDR for a 7 dBm input signal achieving 6.3 bit up to 4 GHz

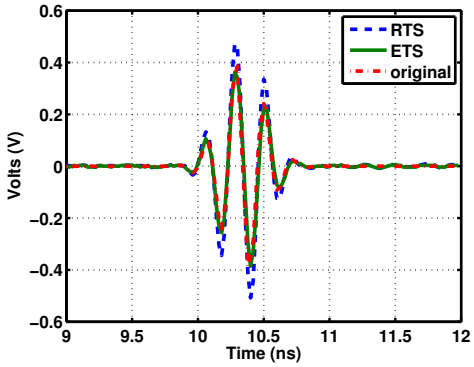

Fig. 8. Original and measured UWB pulses sampled with RTS vs. ETS resulting in 99.5% fidelity

thereby underestimating the power consumption of common blocks which are also needed for a single channel. In [6], no separate power consumption of the core circuit is mentioned which doesn't allow a comparison in terms of FoM. Compared to prior work, this T/H achieves higher ERBW and conversion rate for the same order of power dissipation resulting in a lower FoM.

V. Conclusion

This paper presents a 6-b, 5.5-GHz ERBW subsampling T/H for UWB applications achieving a FoM of 178 fJ/conv-step. For reliability purposes, a bulk switching technique is applied using non-overlapping clock signals and the hold capacitor is precharged before the track phase. Using the bootstrapping technique, a high bandwidth of 5.5-GHz is maintained for large input signals enabling a high dynamic range for the UWB receiver. Exploiting the subsampling principle, the T/H core and clock generator consume only 1.4 mW. It proves that the chip samples a particular gaussian UWB pulse with a high fidelity of 99.5%.

TABLE I
Performance summary and comparison to prior work

Reference	[4]	[5]	[6]	This work
Tech.	0.18 μm CMOS	0.13 μm CMOS	45-GHz BiCMOS	40 nm CMOS
Conv. rate	32 MS/s	84.4 MS/s	4 GS/s	100 MS/s
SNDR ENOB @f_{in}	31.2 dB 4.9 b 1 GHz	43 dB 6.9 b 4 GHz	30 dB$_{SFDR}$ - 8.05 GHz	36.6 dB 5.8 b 5.5 GHz
ERBW	1 GHz	2 GHz[a]	-	5.5 GHz
V_{supply}	1.8 V	1.2 V	5.2 V	0.9 V
P_{dis}	1.6 mW[b]	4.63 mW[a]	550 mW[c]	0.2 mW (T/H) 1.2 mW (clk)
FoM	1.1 pJ/conv	214 fJ/conv	-	178 fJ/conv

[a] Approximated for one channel
[b] Analog part only for fair comparison
[c] Including output buffer

Acknowledgment

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