Reduced Modular Multilevel Converter Model to Evaluate Fault Transients in DC Grids

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Abstract

This paper proposes a reduced model for a modular multilevel converter (MMC) that can be used to evaluate the first transient after a short circuit fault in a DC grid. Detailed modelling of an MMC involves a large number of electrical nodes, hence requiring high computational effort. Reduced converter models have been proposed in the literature. However, calculation times can still be high for large grids. The reduced model proposed in this paper is based on an RLC-circuit that models the capacitive discharge phase of the MMC during DC faults. Therefore, it can be used to efficiently evaluate fault detection criteria that must act within the first transient. By performing transient simulations for a pole-to-pole fault at the converter terminals, the suitability of the model to represent the MMC during faults is demonstrated. Furthermore, it is shown by transient simulations that the model can adequately represent the reflection of travelling waves due to faults in a multiterminal system.

Keywords: Fault Transient, HVDC, Modular Multilevel Converter

1 Introduction

For the bulk transport of power over large distances, high voltage direct current (HVDC) technology is preferred over HVAC technology. Currently, mostly point-to-point HVDC connections are used. To enable the mass introduction of renewable energy into the power system, HVDC grids based on voltage source converter (VSC) technology are considered [1].

In contrast to point-to-point schemes, immediate location and isolation of a fault at the DC side is needed for selective protection. However, due to the high rate-of-rise and high steady-state value of the fault current, the protection system must be able to detect and isolate the fault within milliseconds [2]. For the evaluation of fault transients on this timescale, EMTF-software is used to provide a solution in the time domain [3, 4]. Simulation of large DC grids using EMTF-software can however be cumbersome due to large simulation time.

Detailed modelling of modular multilevel converters (MMC) in EMTF-software involves a high computational burden because of the large number of electrical nodes combined with short timesteps [5]. Therefore, models that reduce the calculation time have been proposed in the literature. In [6], a Thévenin-model is proposed to represent each converter arm. A continuous model

Figure 1: MMC converter leg.

representation of the converter arms is presented in [7]. This model has been extended in [8] to provide blocking capability.

Although these models reduce computational complexity of the converter, the simulation time for these models can still be significant for large DC grids. Moreover, EMTF-software is not very flexible for simulating a large number of fault situations. Therefore, a reduced converter model for the half-bridge MMC based on an RLC-circuit is proposed in this paper. The aim of the model is to represent the behaviour of the converter for the first milliseconds of a fault transient. As fault detection must occur within this timeframe, the model can be used to efficiently investigate fault detection criteria for a variety of fault situations.

The paper is structured as follows. In Section 2, the fault behaviour of the MMC is introduced. Section 3 treats the derivation of the parameters for the reduced model. In Section 4, the model is validated by performing transient simulations in PSCAD/EMTDC [9]. The model is tested for pole-to-pole faults at its terminals and for transient response when a pole-to-ground fault occurs on a cable.

2 MMC fault behaviour

In VSC HVDC, the response of a converter to a DC fault can generally be split up into a passive discharge phase of the capacitors followed by uncontrolled infeed by the AC side (as discussed in [10] for a two-level topology). For the MMC topology, two aspects are of main importance for the fault behaviour.

Figure 2: Half-bridge submodule.

Figure 3: Fault currents in case of a pole-to-pole fault at converter terminals. (Thick solid line: DC current, dashed lines: upper- and lower arm currents, solid line: AC current)

First, the DC capacitor is distributed into different submodules that are connected in series. An example of a half-bridge submodule is shown in Fig. 2. By blocking the IGBTs of the submodules, further discharge of capacitors is prevented. Depending on the submodule topology, the fault current is fed by the AC side (e.g. half-bridge topology) or can be permanently blocked (e.g. full-bridge topology). Second, reactors are included in each converter arm to diminish circulating currents (Fig. 1) [11]. During short circuit faults, these reactors limit the rate of rise of the fault current during the discharge of the submodule capacitors [12].

Fig. 3 shows the DC fault current, arm currents and AC current for one converter leg of a half-bridge MMC for a pole-to-pole fault applied directly at converter terminals. For this figure, the parameters of the converter have been taken from [7]. The fault starts at 10 ms and the IGBTs are not blocked. It can be seen that the upper- and lower arm currents are initially equal. During this phase, the current is only supplied by the submodule capacitors. After about 2 ms, the AC current starts to feed in.

3 RLC-model

In this section, the parameters for the reduced model for the DC side of the converter are derived. The purpose of the model is to account for the capacitive discharge phase during faults. Therefore, an equivalent RLC-model, depicted in Fig. 4, is proposed. Expressions for the model parameters (C_{eq} , R_{eq} and L_{eq}) are first derived.

3.1 Model parameters

When considering the discharge of the capacitors of the MMC submodules, a valid approach is to look at the decrease of the total voltage available in one arm (u^Σ). In [7], a converter arm is approximated as a continuous voltage source. The maximum

Figure 4: RLC-model to represent the MMC during the capacitive discharge phase in case of faults.

amplitude of the voltage injected by one converter arm is determined by the total voltage available in that arm, i.e. the sum of the voltage on all submodule capacitors. The total voltage available for the top and bottom arm, u_u^Σ and u_l^Σ , change with the arm currents i_u and i_l as [7]:

$$\begin{aligned} \frac{du_u^\Sigma}{dt} &= \frac{n_u i_u}{C_{arm}}, \\ \frac{du_l^\Sigma}{dt} &= \frac{n_l i_l}{C_{arm}}. \end{aligned} \quad (1)$$

In (1), n_u and n_l are the number of inserted submodules in the upper and lower arm and C_{arm} is the equivalent series capacitance of the capacitors of all submodules in one arm. This equivalent capacitor can be calculated as C/N , in which C is the capacitor in each submodule and N is the number of submodules per arm.

By summation of the voltages of the lower and upper arm, the voltage of one leg is obtained:

$$u_{leg} = u_u^\Sigma + u_l^\Sigma. \quad (2)$$

Taking the derivative of (2) with respect to time and filling in (1) leads to

$$\frac{du_{leg}}{dt} = \frac{n_u i_u}{C_{arm}} + \frac{n_l i_l}{C_{arm}}. \quad (3)$$

In normal operation, the sum of the insertion indices n_u and n_l equals to one in case of purely sinusoidal control. In case of faults, it can be noted from Fig. 3 that the upper and lower arm current, i_u and i_l are equal during the capacitive discharge phase. Using this knowledge and replacing the arm currents i_u and i_l by i_{leg} to indicate the current in the converter leg, (3) can be simplified to

$$\frac{du_{leg}}{dt} = \frac{i_{leg}}{C_{arm}}. \quad (4)$$

In (4), the AC current is assumed to be zero. As there are three parallel legs in one converter, the capacitance for the total converter in case of faults becomes

$$C_{eq} = 3C_{arm}. \quad (5)$$

To complete the model, the value for L_{eq} and R_{eq} are derived. L_{eq} can be obtained by taking into account that there are two arm reactors in series in each leg and three legs in parallel:

$$L_{eq} = \frac{2}{3}L_{arm}. \quad (6)$$

The equivalent resistance can be obtained from the sum of resistances of all components that are present in the leg during the discharge phase. For a submodule that is switched on, this is the resistance of the upper IGBT (R_{IGBT}). For the other submodules, this is the resistance of the lower diode (R_d). The

equivalent resistance of a converter leg can hence be obtained by:

$$R_{eq,leg} = n_u \cdot R_{IGBT} + (N - n_u) \cdot R_d + n_l \cdot R_{IGBT} + (N - n_l) \cdot R_d. \quad (7)$$

The equivalent converter resistance is the parallel resistance of three converter legs:

$$R_{eq} = R_{eq,leg}/3. \quad (8)$$

3.2 Energy consideration

Another way of deriving the model parameters is by looking at the stored energy from the converter that is released during a fault.

The total stored energy of the converter, $E_{MMC,tot}$, can be calculated as [13]

$$E_{MMC,tot} = 6 \frac{1}{2} \sum_{i=1}^N C_{SM,i} (u_{SM,i})^2, \quad (9)$$

where $u_{SM,i}$ is the voltage on one submodule. However, this stored energy cannot be released directly into the fault, as only N submodules per leg are inserted at once. The energy of a converter upper arm that is released during the capacitive discharge phase of the fault can thus be described as

$$E_{arm,u} = \frac{1}{2} \sum_{i=1}^{n_u} C_{SM,i} (u_{SM,i})^2. \quad (10)$$

Assuming equal submodule capacitances (equal to C) and an equal voltage over each capacitor, (10) can be simplified to:

$$E_{arm,u} = \frac{1}{2} N C_{arm} n_u \left(\frac{u_u^\Sigma}{N} \right)^2, \quad (11)$$

in which u_u^Σ/N is the voltage over one submodule capacitor. An identical derivation can be made for the released energy of the lower arm. The total energy released per leg in case of a fault is thus

$$E_{leg} = E_{arm,u} + E_{arm,l}, \quad (12)$$

$$= \frac{1}{2} C_{arm} (u^\Sigma)^2 \frac{n_u + n_l}{N}, \quad (13)$$

Assuming u^Σ is approximately equal to u_{dc} and $\frac{n_u + n_l}{N}$ is equal to one, the released energy per leg is

$$E_{leg} = \frac{1}{2} C_{arm} (u_{dc})^2. \quad (14)$$

The released energy for a converter is three times the stored energy per leg. The equivalent capacitance needed is thus $3C_{arm}$, which is consistent with (5).

From this derivation, a main assumption for the model becomes clear. It is assumed that the main release of energy into the fault is due to the discharge of capacitors of the inserted submodules at the moment of the fault. The released energy by inserting extra submodules is neglected.

4 Validation of the model for DC transients

In this section, the suitability of the RLC-model to represent fault transients in DC grids is investigated by performing transient simulations in PSCAD/EMTDC [9]. First, the proposed model is benchmarked against a detailed model for a pole-to-pole fault at the converter terminals. Second, a pole-to-ground fault on a cable close to a converter is considered. In this case,

the validity of the RLC-model to represent reflection of travelling waves at the converter terminal is investigated. Third, the RLC-model is used in a multiterminal system to check the validity of the RLC-model for remote converters during fault transients.

4.1 Comparison with detailed model

To validate the RLC-model for a pole-to-pole fault at the converter terminals, it is compared with a detailed converter model. For the detailed model, every submodule is modelled separately as a half-bridge module as shown in Fig. 2. In the detailed model, IGBTs and diodes are modelled by linear switches. Converter parameters have been taken from [7]. Based on these values, the parameters for the proposed RLC-model are 1500 μ F, 0.033 Ω and 2 mH for respectively C_{eq} , R_{eq} and L_{eq} .

Fig. 5 shows the fault current for the detailed model and the RLC-model if a pole-to-pole fault occurs at 10 ms. It can be seen that the RLC-model approximates the fault current well for the first two milliseconds after the fault. This is the timeframe within which the capacitive discharge dominates. After two milliseconds, the fault current is also fed by the AC side. This behaviour cannot longer be explained by the RLC-model.

Figure 5: Comparison of fault current for detailed model and RLC-model for a pole-to-pole fault at the converter terminals.

4.2 Pole-to-ground fault on a cable

In this section, the RLC-model is compared with a continuous converter model for a solid pole-to-ground fault at the end of a 50 km cable. Converter and cable parameters are shown in Tables 1 and 2. The converter configuration is asymmetric and solid grounding of the converters is assumed. For demonstration purposes, IGBTs are not blocked during fault transients. Table 3 contains the derived parameters for the RLC-model. For the cables, the frequency dependent model available in PSCAD/EMTDC is used [9].

The fault starts at 0 ms. Two cases are considered, one case without series inductor between converter and cable and one case with an inductor of 100 mH.

Figs. 6 and 7 show the voltage and the current measured at the converter terminal for the case without a series inductor. It can be seen that the first travelling wave reaches the terminal after about 300 μ s, causing a large voltage drop. The wave is reflected at the terminal in a time-varying manner. The second

AC Primary Voltage	400 kV
AC Reactance	0.1367 H
AC Resistance	3.78 Ω
AC Secondary Voltage	185 kV
Transformer Leakage Reactance	0.15 p.u.
DC Voltage	320 kV
Converter rated power	500 MW
Converter Reactor	32 mH
Arm Resistance	0.5 Ω
Number of Submodules	100
Submodule Capacitance	6.5 mF

Table 1: Converter and AC grid parameters.

	Outer radius [mm]
Copper Core	21,1
XLPE Insulation	37
Copper Screen	40
PE Insulation	48
Characteristic impedance*	18.9 Ω
Travelling wave speed*	167 km/ms

* At high frequencies

Table 2: Cable parameters.

Equivalent capacitance C_{eq}	195 μ F
Equivalent resistance R_{eq}	0.33 Ω
Equivalent inductance L_{eq}	21.3 mH

Table 3: Converter RLC-model parameters

surge is 600 μ s later, causing a voltage increase due to inversion of the voltage wave at the short circuit.

The RLC-model initially approximates the shape of the transient well. It can hence be used to explain the time dependent reflection for the first incident wave. After 1 ms, the RLC-model underestimates the fault current because insertion of extra submodules and infeed from the AC-side are neglected. After two milliseconds, the absolute error on the current is 1 kA, implying a relative error of 5%.

In Figs. 8 and 9, the voltage and current at the faulted cable are shown for the case with a series inductor of 100 mH. The voltage and current are measured at the cable end of the inductor. Due to the series inductor, the current increases slower compared to Fig. 7. The initial voltage drop is almost the same, but the voltage increase after the initial reflection is lower. The error of the RLC-model on the voltage and current is lower than the previous case for the time period shown.

4.3 Pole-to-ground fault in a multiterminal system

The multiterminal system considered is depicted in Fig. 10. This system can be considered as a subsection of a larger DC grid. A solid pole-to-ground fault is located 50 km away from

Figure 6: Fault voltage for continuous model (solid line) and RLC-model (dashed line) for a fault located at 50 km from the converter.

Figure 7: Fault current and for continuous model (solid line) and RLC-model (dashed line) for a fault located at 50 km from the converter.

Figure 8: Fault voltage for continuous model (solid line) and RLC-model (dashed line) for a fault located at 50 km from the converter and 100 mH series inductor.

converter A. The cable length between converter A and B is 150 km. Series inductors can be included at each cable end. The current and voltage to ground are measured at the cable ends at converters A and B. Converter C is not modelled as the solid pole-to-ground fault forms a barrier for travelling waves, prohibiting the converter to influence the voltage and current

Figure 9: Fault current for continuous model (solid line) and RLC-model (dashed line) for a fault located at 50 km from the converter and 100 mH series inductor.

at the side of converter A. The fault transient is simulated with the RLC-model for both converters. The results are benchmarked against the results obtained with continuous models for converters A and B.

First, a case without series inductors is considered. In Fig. 11, the voltages during the fault at the indicated measurements in the network are shown. In this case, u_{1f} and u_{12} , are equal as they are measured at the same bus. These voltages drop to a near-zero value, indicating that the wave is initially not reflected. This can be explained by the fact that both cables have the same characteristic impedance. The wave reaches converter B after 1.3 ms causing the voltage u_{21} to drop. The reflection of the wave at converter B can also be noted in u_{1f} and u_{12} two milliseconds after fault inception. For u_{1f} and u_{12} , the RLC-model performs well until two milliseconds after fault inception. For this period, the relative error on the voltage remains within 5%. At converter B, the voltage u_{21} is initially approximated well by the RLC-model. After three milliseconds after fault inception, the relative error on the voltage exceeds 5%.

The fault voltages for the first four milliseconds after a fault for the case in which series inductors of 100 mH at the end of each cable are included, are shown in Fig. 12. By comparing Fig. 12 (a) and (b), it can be noted that the travelling wave from the fault transient is largely reflected by the series inductors. Similar to the case with one converter, the error at the voltages of the faulted cable is lower compared to the case without series inductors. For the voltages u_{12} and u_{21} , the relative error of the RLC-model compared to the continuous model is limited to 2% within the first four milliseconds after fault inception.

5 Conclusion

In this paper, a reduced model based on an RLC-circuit is proposed to model the response of the half-bridge MMC during fault transients. The parameters for the RLC-model can readily be derived from basic converter parameters. Compared to existing converter models, the proposed model is less detailed leading to a largely reduced simulation time. The RLC-model

Figure 10: Multiterminal system with solid pole-to-ground fault.

Figure 11: Voltages after solid pole-to-ground fault in the multiterminal system. (Solid line: continuous models, dashed line: RLC-models)

does not strictly need to be implemented in EMTF-software, hence flexibility for simulating different fault situations is increased.

By comparison with a detailed converter model, it is shown that the RLC-model can adequately represent the behaviour of the MMC for the first milliseconds of a fault transient. Furthermore, by benchmarking against the continuous converter model, it is shown that the time-varying reflection at the converter terminal of a travelling wave emanating from a fault on a transmission line can be approximated well by the RLC-model. In a multi-terminal system, the RLC-model can be used as well to model converters remote from the fault.

The applicability of the proposed model is limited to only the first milliseconds of a fault transient. However, this is also

Figure 12: Voltages after solid pole-to-ground fault in the multiterminal system including 100 mH series inductors in the cables. (Solid line: continuous models, dashed line: RLC-models)

expected to be the timeframe within which fault detection and location must occur. Therefore, the RLC-model can be used to assess fault detection criteria for a variety of fault situations. The main limitation of the model is the inability to model converters in blocked state. This restricts the validity of the RLC-model to the part of the fault transient between fault incidence at the terminal and converter blocking.

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