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Heteroepitaxy of InP on Si(001) by selective-area metal organic vapor-phase epitaxy in sub-50 nm width trenches: The role of the nucleation layer and the recess engineering

C. Merckling,^{1,a)} N. Waldron,¹ S. Jiang,^{1,2} W. Guo,¹ N. Collaert,¹ M. Caymax,¹ E. Vancoille,¹ K. Barla,¹ A. Thean,¹ M. Heyns,^{1,2} and W. Vandervorst^{1,2}

¹IMEC, Kapeldreef 75, 3001 Leuven, Belgium

²Katholieke Universiteit Leuven, Celestijnenlaan 200D, 3001 Leuven, Belgium

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This study relates to the heteroepitaxy of InP on patterned Si substrates using the defect trapping technique. We carefully investigated the growth mechanism in shallow trench isolation trenches to optimize the nucleation layer. By comparing different recess engineering options: rounded-Ge versus V-grooved, we could show a strong enhancement of the crystalline quality and growth uniformity of the InP semiconductor. The demonstration of III-V heteroepitaxy at scaled dimensions opens the possibility for new applications integrated on Silicon. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4862044>]

Driven by fabrication cost reduction and device performance improvement, the Silicon semiconductor ICT industry continues its never-ending pursuit of new approaches for fabricating integrated circuits.¹ In that context, the heterogeneous integration of III-V high mobility semiconductors² on a Si platform in a 3D architecture such as Fin-Field-Effect-Transistor (FinFET) is a winning combination to further boost the performance of future CMOS generations. The indium gallium arsenide compound semiconductor, with high Indium concentration has been considered as a candidate for n-channel MOS devices beyond 10 nm node technology due to its intrinsically superior electron mobility, high saturation velocity and proper optical bandgap.^{3–5} The best option for the growth of such a complex ternary compound would be to make use of InP binary compounds as a buffer for the lattice matched In_{0.53}Ga_{0.47}As channel.^{6–8} Nevertheless, for the integration of III-V compounds on Si substrates, many issues still need to be overcome such as the lattice mismatch ($f_{\text{InP/Si}} = 8.06\%$) as well as the polar/non-polar interfaces resulting in the generation of crystalline defects in high density: misfit and threading dislocations, twins, stacking faults, anti-phase boundaries, which would strongly degrade the device performances. Several options have been considered to obtain high quality single crystal III-V compounds on Si with low defect density: strain relaxed buffers,^{9,10} epitaxial lateral overgrowth,¹¹ rapid melt growth,¹² and the defect confinement technique.^{13,14} Further improvements are still required to reduce the too high defect density in the III-V layers.

The defect confinement technique has recently attracted great interest due to the possibility of obtaining high quality III-V based active regions using nanometer scale trenches with high aspect ratio (>2) (Ref. 15) in order to eliminate (111)-oriented defects (such as threading dislocations, twins, or stacking faults) on the sidewalls. The III-V compound semiconductor is grown selectively on a Si substrate in

shallow trench isolation (STI) structures¹⁶ as shown in Figure 1(a). While (111)-oriented defects are efficiently trapped perpendicularly to the trench, the weakness of this method resides in the impossibility to trap the (111)-oriented defects along the parallel direction of the trench.

The III-V heteroepitaxy has been performed in a 300 mm production AIXTRON Crius MOVPE reactor, equipped with a vertical showerhead injector. The group-III precursor used was trimethylindium (TMIn), and the group-V sources are tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP). During the growth, the reactor pressure can vary from 50 millibars to 500 millibars with a H₂ total flow of 48 slm as carrier gas. Standard SiO₂ STI patterning was applied on 300 mm on-axis Si(001) substrates to realize 250 nm deep trenches with widths ranging from 20 nm to 500 nm. The average active area exposed to the III-V layers deposition was kept constant at 10% of the total Si wafer surface. The trenches are aligned along the [110] and orthogonal $[-110]$ directions. Two different recess engineering have been studied: “rounded-Ge” buffer layer obtained by vapour HCl etching of Si followed by *in-situ* Ge buffer epitaxy and the V-grooved enclosure obtained by wet Si etching using tetramethylammonium hydroxide (TMAH) (5% @ 80 °C) stabilizing the {111} planes of Si in the bottom of the trenches.

We report here on the Selective Area Metal Organic Vapor Phase Epitaxy (SA-MOVPE) growth of InP on STI patterned Si wafers using the defect confinement technique focusing on scaled trench widths ($W < 50$ nm). Moreover, we study the impact of the crystalline alignment of the InP layer with the underlying substrate by exploring as starting geometry at the bottom STI, i.e., rounded etch with Ge buffer^{14,17} versus a crystalline $\langle 111 \rangle$ V-groove structure in the Si (Ref. 18) as shown in Figure 1(a). The basic approach of our SA-MOVPE growth of InP on pre-patterned Si(001) relies on a two-step InP growth as depicted in Figure 1(b). First, the native oxide from the bottom STI surface is thermally desorbed by a high temperature bake above 800 °C in H₂ at 50 millibars. Then, the substrate temperature was

^{a)}Author to whom correspondence should be addressed. Electronic mail: clement.merckling@imec.be.

FIG. 1. (a) Schematics of the III-V on Si heterostructure with high aspect ratio STI trenches. The AFM analysis of the rounded-Ge and V-grooved starting surfaces is presented in the inset. (b) Time sequence of substrate temperature (T) and precursors flows (TBAs, TBP, TMIn) during SA-MOVPE of InP.

cooled down to a low temperature ($<450^{\circ}\text{C}$) to grow the nucleation layer. Below 550°C , the surface is exposed to Arsenic at high pressure to form one monolayer of As-terminated surface which will promote the InP wetting. After the nucleation step, the temperature was ramped up to 550°C to obtain a high crystalline quality InP layer.

Recently, we could demonstrate a great improvement in SA-MOVPE of InP by a systematic analysis of the influence of the growth parameters on the crystal quality.¹⁹ Our study was based on the “rounded-Ge” buffer approach and led to substantial progress for the growth of high quality InP, using the process depicted above, with a uniform growth and a low defect density along the trenches as shown in the transmission electron microscopy (TEM) image in Figure 2((a)-(i)) of a 150-nm-trench width. However, the InP layer growth in a sub-50 nm trench width (same sample, with same epitaxial

conditions) is far more defective as shown in the parallel view TEM image in Figure 2((b)-(i)). In fact in these narrow trenches, the InP layer is very defective, with an extremely rough and discontinuous surface. As the surface treatment for wide and narrow trenches is identical, we must conclude that the geometrical confinement within the narrow trenches induces a transition from 2D to 3D growth. Evidence for this model can be derived from the observation of the morphology of the initial InP nucleation layer (which is grown at $T_G = 425^{\circ}\text{C}$ & $R_{V/III} > 700$). In Figure 2, we provide the topography as measured with AFM for a growth time sufficient for a full coverage surface in the wide trenches. In order to enable access for the AFM tip to the bottom of the trench, the sample was treated in a 2% hydrofluoric acid solution in order to etch away the STI film. Figures 2((a)-(ii)) and 2((b)-(ii)) show, respectively, the topography images

FIG. 2. (a) Cross-sectional TEM image in parallel view of InP (i) of $W = 150\text{ nm}$ and (ii) of $W = 50\text{ nm}$ trenches. (b) Tapping mode AFM images of InP nucleation layer showing (i) islands in high density in wide trenches and (ii) islands in low density in narrow trenches. (c) Schematic illustrations of growth mechanisms during InP SA-MOVPE for (i) wide trenches and (ii) for narrow trenches.

acquired in a wide 150-nm-width trench and narrow 50-nm-width trench. As observed in the AFM images, the nucleation layer consists of a 3D layer with an average island size of ~ 50 nm in the wide trench. In the narrow trenches the geometrical confinement limits the size of the islands to the trench width thereby leading to a smaller island density coverage per trench for the same growth time. Based on these differences in island density surface coverage, a growth model can now be derived to explain the difference in crystal quality observed previously. In the case of wide trenches, Figure 2(a)-(iii): initially, after the nucleation layer, 50-nm-size islands are formed in high density on the surface. The subsequent InP growth at high temperature will lead to their further growth leading, thereby, to a fast coalescence process. The crystal will then grow in 3D mode and finally a 2D growth mode for the III-V in trenches is reached. This growth behaviour leads to high quality epitaxial growth of InP in STI with low defect density along the trenches. On the other hand, in the case of narrow trenches (< 50 nm), Figure 2(b)-(iii), after the nucleation layer ~ 50 -nm-size islands are formed in much lower density. The subsequent epitaxy of InP at high temperature therefore implies a further island growth mode before reaching the expected coalescence process. In that scenario, the InP film coalesced into a continuous layer too late and the growth mode will remain 3D.

Based on this model, it is clear that to improve the epitaxial quality of InP in sub-50-nm trench widths, the key is to find growth conditions, which enhances higher density of the small islands in order to accelerate the coalescence process. This was achieved by lowering the growth temperature of the nucleation layer ($T_G = 370^\circ\text{C}$) together with using a very high V/III ratio ($R_{V/III} > 2000$). At these low temperatures, the cracking efficiency of the TBP precursors is strongly reduced and increasing the $R_{V/III}$ during the nucleation process would still allow the growth of the InP crystal in these extreme conditions. Figure 3(a) shows a tilted SEM image of the InP/Ge/Si heterostructure in narrow trenches ($W = 50$ nm), whereby the optimal nucleation conditions

were used. The uniformity along the trench is strongly improved, but the discontinuities indicate that defects are still present. TEM analysis was carried out to evaluate the morphological and structural properties of the InP/Ge/Si heterostructure in 50-nm-trenches. Figures 3(b) and 3(c) show, respectively, the perpendicular and parallel view TEM images (2 beams bright field 220 conditions) of one of these 50-nm-width lines in which the different regions: Si, Ge, InP, and STI are identified on the patterns. Compared to Figure 2(b), the InP/Ge/Si heterostructure in narrow trenches is improved which demonstrates the strong impact of the optimized nucleation layer. The misfit dislocation network is clearly visible at the InP/Ge interface, leading to the generation of threading dislocations but also additional planar defects (111)-oriented such as nanotwins or stacking faults are present. From Figure 3(b) in perpendicular view, most of the defects are localized in the bottom part of the trench. The $\{111\}$ crystallographic plane defects are either trapped on the side walls or annihilated when crossing with other defects, emphasizing the efficiency of the ART concept. Moreover, as seen in the perpendicular view, the defective region in the InP layer is only located in the bottom part of the trench and only few of these defects are crossing the full stack (Figure 3(c)). We can conclude from this that the highly defective bottom part of the trench is the signature of the islanding—coalescence—3D growth steps as discussed in the growth model.

But as still too high defects propagate throughout the film, based on the tilted view SEM and parallel view TEM images, a second step in improving the III-V crystal quality further is the transition from the initial rounded-Ge shape towards a silicon V-groove STI-pattern. The fundamental advantage of this approach is that, instead of starting from a rounded-Ge surface showing different types of facets such as $\{111\}$, $\{113\}$, and $\{001\}$, initiating the growth from a pre-defined Si $\{111\}$ enclosure will provide a surface with a unique polarity. Obviously one expects that the optimized nucleation layer growth would also here lead to better film quality in narrow trenches due to a better nucleation uniformity.

To quantitatively compare both recess engineering options, X-ray diffraction was performed on both InP/Ge/Si and InP/Si heterostructures using the same XRD characterization method as in Ref. 19. Figure 4(a) is the ω - 2θ scan recorded along the sample normal. The X-ray spectra of the InP/Ge/Si sample present an intense peak centred at $\omega = 34.56^\circ$ for the (0 0 4) Bragg reflections of the Si(001) substrate and two other peaks centred at $\omega = 33.0^\circ$ and $\omega = 31.58^\circ$ corresponding, respectively, to the diffraction of the (0 0 4) planes of the 50-nm-thick Ge buffer layer and the 250-nm-thick InP layer with a low intensity ratio: $I_{\text{InP}}/I_{\text{Si}} = 3 \cdot 10^{-4}$. On the other hand for the InP/Si sample, besides the Si substrate diffraction peak, only an intense and thin diffraction peak for the 250-nm-thick InP layer centred at $\omega = 31.58^\circ$ is observable with a higher peak intensity ratio: $I_{\text{InP}}/I_{\text{Si}} = 3 \cdot 10^{-3}$ for an equivalent thickness range. Furthermore, the ω -scans of the InP (0 0 4) Bragg reflections, used as a quality criterion for the InP crystalline perfection, are presented in Figure 4(b). The extracted FWHM

FIG. 3. InP/Ge/Si heterostructure grown in “rounded-Ge” 50-nm-width trenches with optimized nucleation conditions: (a) tilted view SEM, cross-sectional TEM image (b) in perpendicular view showing misfit dislocation network at the InP/Ge interface and (c) in parallel view showing a more uniform growth with the optimized nucleation layer.

FIG. 4. (a) X-ray diffraction ω - 2θ scans along the Si (0 0 4) Bragg reflection and (b) X-ray rocking curve (ω -scans) along the InP (0 0 4) Bragg reflection of both InP/Ge/Si and InP/Si heterostructures in patterned Si wafer. Reciprocal lattice maps of the (2 2 4) reflections from InP of (c) InP/Ge/Si and (d) InP/Si heterostructures.

value of the broad diffraction peak from InP grown on Ge/Si is $\text{FWHM}_{\text{InP/Ge/Si}} = 1690$ arc sec. While the InP grown directly on Si presents a much narrower diffraction peak with $\text{FWHM}_{\text{InP/Si}} = 540$ arc sec. Finally, in order to investigate the relaxation properties on InP, reciprocal space mapping (RSM) around the asymmetric (2 2 4) Bragg reflections was performed on both heterostructures. These cartographies confirmed that InP is fully relaxed (more than 99.5% relaxation rate), as expected with the high lattice mismatch between the Si substrate and the InP epilayer. A zoom on the (2 2 4) InP Bragg reflection of InP/Ge/Si (Figure 4(c)) presents a particular shape with an anisotropic elongation in the orthogonal directions, which is evidence once more of a strong mosaicity in the layer. This mosaicity is clearly reduced in the case of InP/Si heterostructure (Figure 4(d)) with a higher (2 2 4) InP Bragg reflection intensity.

The improved InP epitaxial quality for the V-groove wafers relative to the rounded-Ge wafer was not only observed by XRD but also confirmed by SEM and TEM analysis. The tilted SEM view (Figure 5(a)) of InP in 50-nm-width trenches displays a uniform growth of the III-V layer with both (111)A and (111)B facets clearly visible above the STI level.²⁰ The cross view TEM image in perpendicular view (Figure 5(b)) reveals a very sharp interface between the Si substrate and the InP layer. This interface exhibits a complex network of twins which are formed at the two InP(111)//Si(111) interfaces because the (111)-oriented surface of Si allows with the same probability the growth of both un-twinned and twinned (111)-oriented InP surface.²¹ Beyond the twinned region, corresponding to the first 10 nm, the InP planes are perfectly aligned with the ones of the silicon substrate. Finally, Figure 5(c) depicts the parallel view TEM image and reveals a perfect InP epitaxy in the upper

region with an extremely low density of defects along the trenches. A Moiré region (in inset) is observed at the bottom of the trench and results from the interference between the electrons beams diffracted by the Si substrate and by the InP layer. The homogeneity of the Moiré fringes network attests the uniform plastic relaxation process of InP at the earliest stage of the growth. Moreover, no vertical defects, like anti-phase boundaries, are observed.

FIG. 5. InP/Si heterostructure grown in "V-grooved" 50-nm-width trenches with optimized nucleation conditions: (a) tilted view SEM, cross-sectional TEM images (b) in perpendicular view showing a twinned region at the InP/Si interface and (c) in parallel view showing a very uniform growth and low defect density InP layer with the Moiré fringes at the InP/Si bottom interface in inset.

The local electrical resistance of InP in 80-nm-width trenches was measured by scanning spreading resistance microscopy (SSRM) at room temperature. Fig. 6 shows the SSRM cross section images of the InP heterostructures grown either on rounded-Ge (a) either on V-groove (b) starting surfaces, respectively. On the three SSRM images the high spreading resistance area corresponds to the STI oxide on both sides and to air at the top. In Fig. 6(a), the Ge buffer region is clearly observed in the bottom of the trench corresponding to a highly conductive layer, which is attributed to the diffusion of group-V elements (As or P) used during InP selective epitaxial growth process in the epitaxial Ge buffer layer. In Fig. 6(b), the InP/Si interface is also noticeable but is much thinner and is presenting a higher resistance than the Ge/InP interface. Moreover, the impact of the recess engineering on the local spreading resistance for the two InP samples is clearly evidenced by these SSRM studies. As seen in Fig. 6(a), the sample grown on a rounded-Ge surface exhibits a low resistance (high conductivity) in the $\sim 10^6$ ohms range, while the resistance is clearly improved by using a V-groove starting surface (Fig. 6(b)) where the sample shows a uniformly increased spreading resistance in the $\sim 5 \times 10^7$ ohms range.

FIG. 6. Room temperature SSRM patterns in $W = 80$ nm trenches of InP epitaxially grown on (a) rounded-Ge and (b) Si V-groove starting surface, respectively.

We revealed here the strong impact of the low temperature nucleation layer on the InP selective area epitaxy and highlighted differences on the growth mechanism between wide and narrow trench widths. The key feature to improve the heteroepitaxy is to reduce the diffusion length of the adatoms in order to increase the islands density per trenches. This has been achieved by further lowering the growth temperature together with increasing the V/III ratio during the nucleation step. On rounded-Ge buffer, the use of this optimized nucleation layer radically improves the growth of InP in sub-50-nm trench widths but the overall epitaxial quality is not increased. This has been confirmed by XRD giving a FWHM value of the InP rocking curve around 1690 arc sec, similar to the FWHM value extracted on the InP heteroepitaxy using a non-optimized nucleation layer grown at higher temperature reported here.¹⁹ This can be explained by the use of a Ge buffer with a Si/Ge interface periodically decorated with misfit dislocations generating high density of threading dislocations in Ge. In addition to the misfit dislocations network formed at the InP/Ge interface, all defects from the Ge buffer will propagate in the III-V layer. In contrast to the Ge/Si case using identical InP process conditions on a V-groove Si surface presented a clear reduction of the FWHM value of the (0 0 4) InP rocking curve down to 540 arc sec as well as a strong increase in the peak ratio. Considering the InP thickness in the trench (~ 250 nm) and the active area on the mask (10%), the XRD signal is equivalent to a 25-nm-thick blanket layer, meaning that the extracted FWHM value on InP/Si is extremely low. Moreover, as the rocking curve FWHM is proportional to the square root of the dislocation density, this corresponds to an order of magnitude reduction of the defect density level. This is undoubtedly linked to the different relaxation mechanism of InP: misfit dislocations network on Ge versus a twins network on $\{111\}_{\text{Si}}$ -enclosure. Next, on the V-grooved surface, the parallel view of the InP layer is almost defect free in the top part of the trench and defects are only visible in the bottom part of the trench originating from the different growth steps: islanding—coalescence—3D growth before reaching the high quality 2D growth of InP. Despite a larger mismatch ($f_{\text{InP/Si}} = 8.06\%$ vs. $f_{\text{InP/Ge}} = 4.03\%$), a clear enhancement in InP crystalline quality is obtained by using optimal nucleation growth conditions starting from a $\{111\}$ -faceted Si surface. Finally, the recess engineering approach also impact the final intrinsic spreading resistance of the InP semiconductor. In the case of the rounded-Ge buffer, the InP presents a much lower spreading resistance compared to the use of the V-groove Si surface. This can be explained first by a higher crystalline quality of the InP when grown directly on Si but more likely due to the absence of Ge up-diffusion in InP which was measured by SIMS around 0.1%.¹⁹

In conclusion, we have reported here on the use of defect confinement technique to integrate the mismatched InP compound semiconductor on a large scale STI patterned Si(001) substrate. In this study, we demonstrated the importance of the initial nucleation process and its impact on the growth mode. Moreover, great improvement in the InP epitaxial quality has been achieved by the use of a V-grooved

Si starting surface. To the best of our knowledge, this is the first report on the monolithic integration of III-V semiconductor on Si in scaled dimensions using the defect confinement technique. With this approach, such virtual III-V substrates can be used to integrate InGaAs high mobility channels in a regular CMOS process line.

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