A Low-Noise High-Frame-Rate 1D-Decoding Readout Architecture for Stacked Image Sensors

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***Abstract*—The continuously increasing array resolution of CMOS imagers poses a great challenge in combining high frame rate and low-light detection in the same sensor. To cope with this, parallel readout architectures are needed. This paper proposes a readout architecture for 8K stacked image sensors which uses a novel 1D-decoding readout based on Block-of-Pixels and Incremental-Sigma-Delta ADCs. The proposed 1D decoding system reduces the control lines of the pixels and allows a simpler decoding, an increased parallelism and an improved robustness over process yield. The experimental results from a test chip implemented in a standard CIS technology show that at 10μm pixel pitch, the proposed readout architecture can achieve a high frame rate of 730fps and a low read noise of 1.4e^-. In a real stacked implementation, the frame rate can further increase to about 960fps at 8K resolution, at the cost of a slight increase in thermal noise by 14μV.**

***Index Terms*—image sensor, UHDTV, dynamic range, low noise, high frame rate, 3D integration, stacked, high resolution, ADC, Incremental $\Sigma\Delta$**

I. Introduction

CMOS image sensors have seen a huge increase in demand over the past years due to the massive implementation of cameras in many consumer applications such as mobile phones, mp3 players, tablets, digital still cameras, etc. The research in the field is typically focused on improving the image quality, on increasing the frame rate, and on reducing the chip cost and power consumption, etc.[1]. Consumers often identify the image quality with the array resolution. This perception gave rise to the pixel race [2] where the pixel pitch continuously reduces and the pixel count increases. 4K TVs are available today and will be followed by 8K UHDTV (7680 x 4320 pixels) in the coming years [3]. Together with the spatial resolution increase, there is also need for low-light detection and high frame rate.

Good low-light detection capability increases the usability of the sensor in poorly illuminated areas. In order to improve the low-light performance of a sensor, methods to lower the noise floor of the pixel and that of the readout circuitry are needed. Dynamic range extension realized by lowering the noise floor is preferable.

Another important specification of imagers is the frame rate. High frame rate is required in an increasing number of fields such as scientific applications, robotics, security, video documentaries, automotive, etc [4][5]. In consumer applications, high frame rate is often used for capturing fast moving scenes (e.g. animals in video documentaries). Frame rates of about 120fps are now available in high-end smartphones.

Combining high frame rate with low-light-detection characteristics in a single sensor becomes challenging when the sensor resolution increases. As the noise floor is largely contributed by the thermal noise, reducing its effect requires low-pass filtering and/or multiple sampling [6] which contrasts the high bandwidth required by high-speed imagers. For instance, the column-parallel architecture of [7] can reach a very low noise of 0.95e^- but with a low frame rate of 4fps. A new parallel readout architecture is therefore needed to combine high readout speed and low noise in large-resolution arrays. While current-mode pixels and readout [8] can be used for increasing the readout speed, their noise performance is worst than the mainstream voltage mode pinned photodiodes and are not considered in this work.

To increase the parallelism of standard column-level readout circuitry, parallel readout architectures through stacking multiple silicon tiers have been proposed in previous works (e.g. [9] [10]). Those architectures are mainly based on sub-array of pixels parallel readout circuitry which remain constant at the increase of the sensor resolution. In a dual-tier stacked architecture, a sub-array of pixels in the top tier is connected through a micro-bump to its own ADC in the bottom tier. In contrast with column-level-readout-based imagers, a 2D decoding is required to control the pixel operation, as the sub-array is composed of multiple rows and columns. The pixel architecture has to be modified to accommodate 2D decoding. [9] proposes a 2D-decoding pixel with an impressive value of 2.5 transistors (Fig. 1 a)). This solution, however, increases the number of control lines and transistors per pixel and adds extra select transistors per sub-row. This option may corrupt the uniform pixel distribution, possibly causing an increase of the fixed pattern noise. Another problem of 2D-decoding parallel readout architectures is the yield of the ADCs at the second tier. In case a single ADC fails, a group of pixels cannot be converted and their information cannot be reconstructed through interpolating techniques. This is due to the rectangular shape of the grouping.

In order to solve the complexity of the decoding and the yield problem, in this paper we propose and analyze a new parallel readout architecture for stacked image sensors based on 1D decoding and Incremental-Sigma-Delta ADCs for low-noise and high-speed UHDTV-resolution imagers. To verify the theoretical analysis, we designed a test chip in a standard CIS technology emulating the readout path of the stacked architecture.

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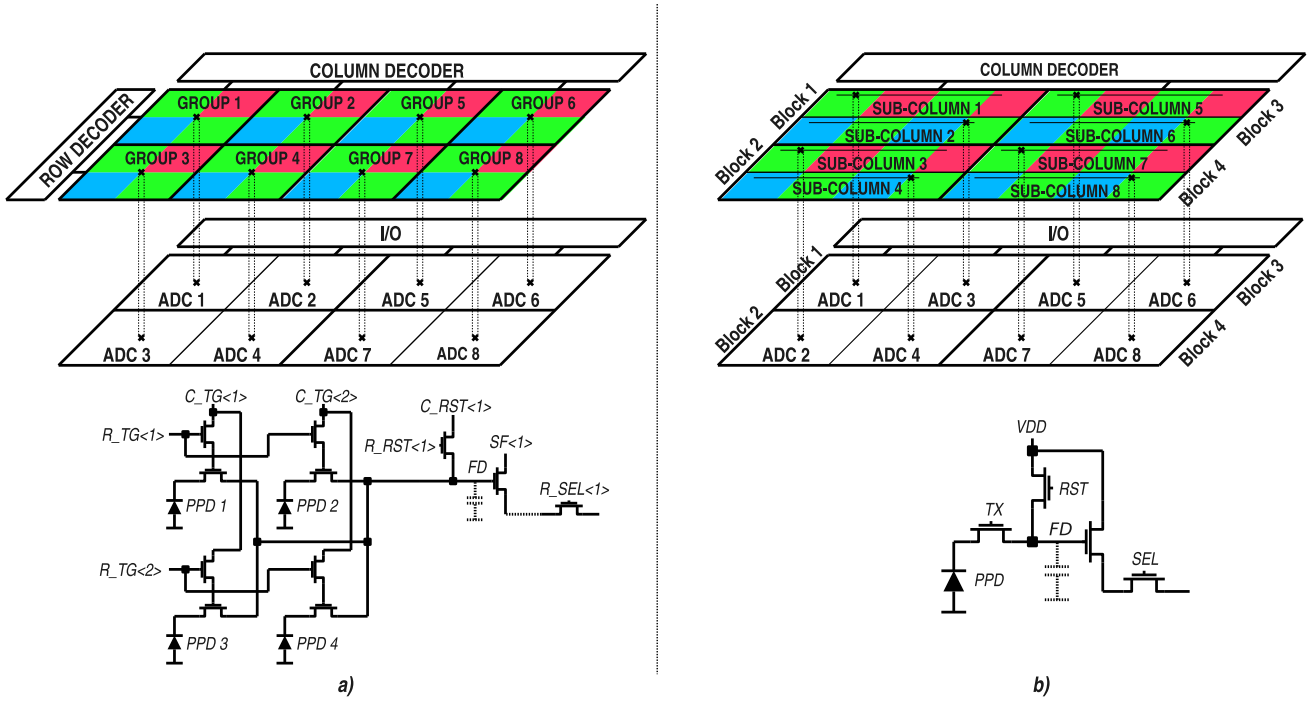

Fig. 1. Dual-tier stacked image sensor concept: (a) Group of pixels parallel readout and relative 2D decoding pixel [9]. (b) Proposed Block-of-Pixels parallel readout with one ADC per sub-column and relative pixel. As only 1D decoding is required, the conventional 4T pinned-photodiode pixel can be used in the proposed architecture.

This paper is organized as follows. Section II describes the stacked readout architecture based on 1D-decoding Block-of-Pixels. Section III introduces the ISD ADC used in this work to achieve low noise and low area while Section IV presents design issues, analysis and measurement results of the test chip. Finally, conclusions are drawn in section V.

II. Stacked Architecture

Fig. 1 (b) shows the proposed imager architecture in a dual tier stacked technology: the top silicon layer (tier 0) implements the 4T-pixels array based on the mainstream backside-illuminated [11] technology, while the second layer (tier 1) implements the readout circuitry. By using BSI at the top, the two tiers can be face-to-face connected through micro-bumps [12], avoiding the need for Through-Silicon-Vias (TSV). Compared to standard CIS-technology readout architectures, the dual-tier stacked implementations have several advantages, namely:

a) *Decoupling the optical from analog/digital performance*

The top tier can be optimized for optical performance (low dark current, high quantum efficiency etc.), whereas the bottom tier can be optimized for analog/digital performance. This is a powerful feature as it allows the technology scaling of the second tier, without impacting the optical performance, potentially increasing the digital I/O speed and reducing the power consumption of the digital blocks.

b) *Decreased imager chip area*

Placing the readout circuitry at the bottom tier instead of laterally to the pixel array decreases the total footprint [11].

c) *Parallel readout*

Each bump can connect a sub-array of pixels of tier 0 to its own readout block at tier 1, allowing a parallel readout which can be kept constant at variable resolutions. It follows that, ideally, the frame rate of the stacked sensor remains constant when varying the spatial resolution.

The main drawbacks include the increased cost, the micro-bump yield and the possible alteration of the photodiode characteristics due to the silicon stress caused by the bump-bonding process.

The stacked imager architecture proposed in this work is based on 1D decoding. The implementation uses sub-column addressing + sub-column ADC as seen in Fig. 1 (b). Tier 0 is divided into blocks of pixels (BOP). For convenience, each BOP is composed of N columns and N^2 rows of pixels where N represents an integer number as shown in Fig. 2. Each BOP has N micro-bumps placed at regular positions and each column of the BOP is connected to its own micro-bump as shown in Fig. 2. Tier 1 is divided into Blocks of ADCs (BOA) having the same area size as the BOPs. N ADCs are included in each BOA and each ADC is connected to its own micro-bump. It follows that each column of a BOP is connected to its own ADC at a BOA.

This architecture has several advantages compared to [9]. Only a row decoder or a simple shift register is needed to control the pixel operation. Each output of the decoder is replicated to all the BOPs as shown in Fig. 3. Using 1D decoding like in the conventional CIS imagers allows the use of 4T pinned-photodiode pixels which can scale down to 1.5T/pixel instead of the 2.5T of [9]. Furthermore, no added select switch per group of pixels is needed. Other advantages include the improved yield: for some applications, the sub-

column of a faulty ADC can be digitally reconstructed through interpolating techniques using the information from the pixels of the neighboring sub-columns [13].

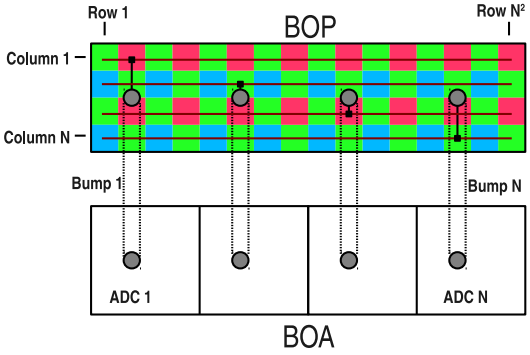

Fig. 2. Each block of pixels at tier 0 contains N columns and N^2 rows. Each column is connected to its own ADC at the block of ADCs through its own micro-bump requiring a simple 1D decoding.

The number of pixels to be processed by one ADC which is equivalent to the number of rows of the BOP, is a function of the ADC area (A_{ADC}) and of the pixel area(A_{pixel}):

$$N_{rows} = N^2_{columns} = \frac{A_{ADC}}{A_{pixel}} \tag{1}$$

The micro-bump pitch of this architecture does not limit the pixel pitch as the micro-bump is shared by multiple pixels. Its pitch can be as large as the ADC pitch in the proposed implementation. The technological limitations in pixel pitch and micro-bump pitch are, therefore, decoupled.

Although recent papers have shown that the micro-bump pitch has fallen below 10μm [14], such size would compromise the pixel pitch in case compact, per-pixel ADCs [15] are used at the second tier. However, given their small size, those ADCs can achieve only about 8bit resolution. Therefore, they are not suitable for low-light detection and they are not considered in this work.

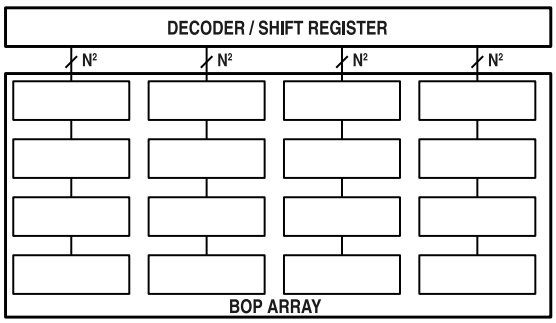

Fig. 3. The proposed BOP based architectures simplifies the decoding system. The output of a single decoder or shift register is sent parallel to all the BOPs.

An important issue in designing a stacked imager is the yield of the bump-bonding process. Robust design is required to cope with this. The proposed architecture allows the placement of multiple micro-bumps per ADC connection. In case of a uniformly distributed micro-bump yield of 99.7%, using 4 micro-bumps per connection would lower the failure rate of the connection between the BOP columns and the BOA ADCs to 0.081ppb. Using more micro-bumps per connection, however, slightly increases the sub-column settling time. Fig. 4 shows a possible positioning of the micro-bumps in case four of them are used for each sub-column.

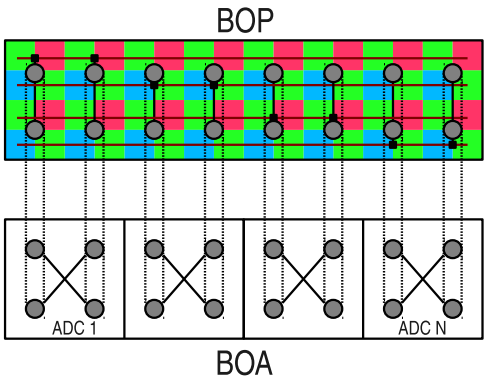

Fig. 4. In this analysis, each row of pixels of the BOP is connected to its own ADC at BOA through 4 micro-bumps, improving the yield of the connection.

III. A/D CONVERTER

According to (1), the parallelism of the proposed stacked architecture is directly proportional to the ADC area. Readout circuits using Nyquist rate ADCs require high gain amplifiers in front to achieve low noise [6]. Given their large area, the use of gain amplifiers would decrease the parallelism and therefore, reduce the frame rate.

Incremental-Sigma-Delta (ISD) ADCs are known for their capability to provide high resolution with low-precision, therefore low-area analog building blocks [16]. Furthermore, given the intrinsic oversampling, they lower the thermal noise of the pixel source follower (SF) without the need of a gain amplifier or multiple A/D conversions [17]. This ADC topology is therefore an ideal candidate for our stacked readout architecture.

The simplest ISD converter consists of a first order modulator and a first order digital filter (counter). Similarly to the single-slope ADCs [1], the first order ISD ADC has a resolution in bits equivalent to log_2M with M representing the clock cycles used for the conversion of the input signal. These samples are effective in averaging the pixel source follower thermal noise. Requiring one clock cycle for each quantization step, the first-order modulator is not suitable for high frame rate.

A second-order ISD (Fig. 5), on the other hand, has a resolution D measured in bits:

$$D = \log_2 M(M+1) - 1 \tag{2}$$

As seen in Fig. 6, the number of clock cycles for the required resolution are drastically reduced when compared to a first-order modulator. For instance, for a DR of 16 bits, the second-order ISD requires only 360 clocks instead of 65536 of the first order modulator. Due to the cycle-dependent weight coefficients [16], the noise averaging effect of the second order ISD is slightly reduced compared to the first order one.

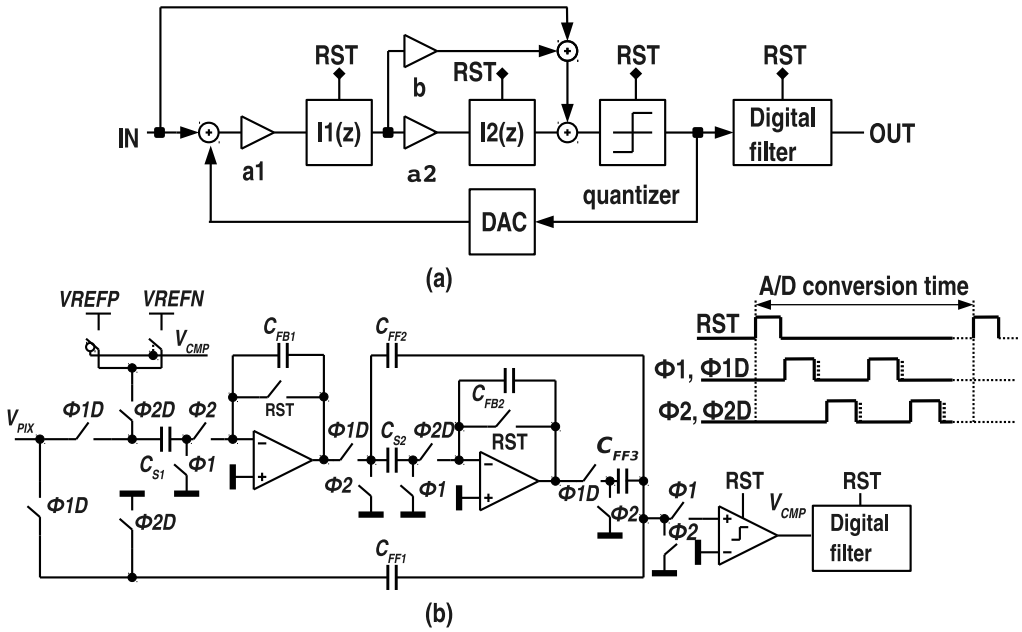

Fig. 5. Second-order feed-forward Incremental-Sigma-Delta ADC. (a) Block diagram. (b) Circuit schematic and correspondent timing.

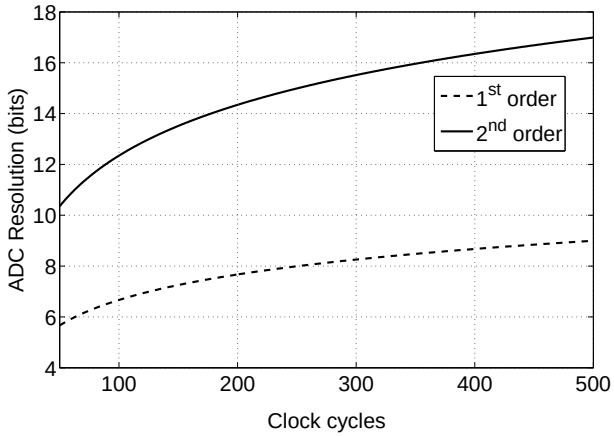

Fig. 6. 1^{st} and 2^{nd}-order ISD ADC resolution as a function of the number of clock cycles.

To further decrease the number of clock cycles for a given resolution in bits, a higher-order ISD can be used. This, however, increases the area and the complexity of the digital filter and of the modulator and introduces stability concerns [18]. Therefore, we opt for a second-order ISD ADC. The schematic of the proposed ISD ADC is shown in Fig. 5 (b) and is based on a Feed-Forward modulator [19].

IV. Analysis and Experimental Results

A study has been carried out in order to investigate the capabilities of the stacked imager readout circuitry based on second-order ISD ADC to achieve low noise and high frame rate when applied to an 8K image sensor.

The readout path from a pixel at the BOP to its own ISD ADC at the BOA and the relative timing diagram are shown in Fig. 7. For simplicity, we show here only the first stage of the modulator of the ISD ADC. The capacitive load of the pixel SF is composed of the sub-column parasitic capacitance C_p, of the parasitic capacitance of the micro-bumps C_{bump} and of the sampling capacitor C_s of the ISD ADC. The sub-column

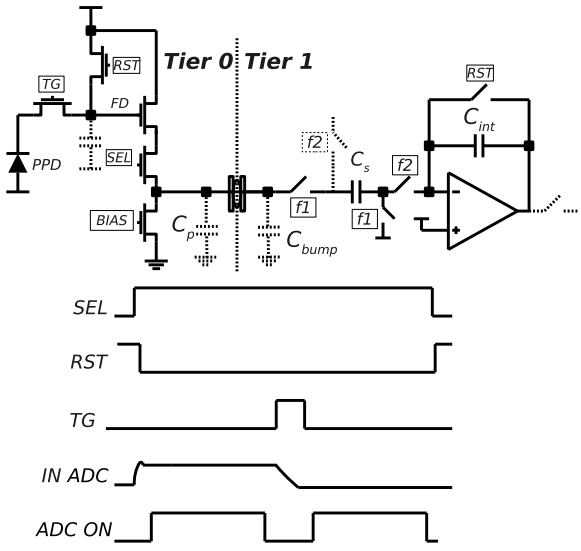

Fig. 7. Processing path from the pixel to the first stage of the ISD ADC and its corresponding timing diagram.

capacitance C_p is dependent on the sub-column resolution and on the pixel pitch and is expressed as:

$$C_p = (C_{SW} + \frac{C_u \cdot P_{pitch}}{10^{-6}}) \cdot N_{rows} \quad (3)$$

where C_u represent the capacitance of a metal connection with 1μm length, P_{pitch} represents the pixel pitch and C_{SW} represents the parasitic capacitance of the pixel select switch. Assuming a pixel pitch of 10μm and an ADC area of 4000μm^2, a parallelism of 49 pixels per ADC can be

achieved according to (1) with 7 columns per BOP. We assume 4 micro-bumps per sub-column-to-ADC connection, each having a parasitic capacitance of 20fF. The parasitic capacitance contribution of each pixel to C_p is 2.5fF (post-layout parasitic extraction). Therefore, the capacitive load of the pixel SF corresponds to 200fF in the stacked architecture and 10.8pF in the CIS architecture with 8K resolution. This load capacitance impacts both the noise and the frame-rate performance of the imager as will be shown in the following sub-sections.

A. Noise analysis

The noise analysis of the stacked readout architecture is simalar to that of a CIS readout with column-parallel ADC with the main difference residing on the capacitive load of the pixel SF. Digital-Correlated-Double-Sampling (DCDS) is used for decreasing the pixel reset and fixed-pattern noise (FPN). Requiring 2 A/D conversions per pixel, the DCDS is slower than the analog CDS (ACDS). However, we opted for the DCDS for the following reasons. The addition of an ACDS block in front of the ADC consumes large area [6], therefore, it reduces the parallelism of the stacked architecture (see (1)). The ACDS adds FPN due to its offset, its gain variation etc. [20] and requires calibration. Furthermore, since in the ACDS operation the A/D conversion is typically performed in the subtracted signal, the effect of the oversampling is reduced, lowering the capability to achieve low noise [17].

The total thermal noise at the output of the pixel SF in DCDS mode is expressed as ([6]):

$$\overline{n^2} \simeq \left(\frac{F_{SF}^2 \xi_{SF} K_B T}{C_p + 4 \cdot C_{bump} + C_s} + \frac{K_B T}{C_s} + \overline{V_n^2}_{,ADC} + \right. \\ \left. + \frac{1}{4M(M+1)^2} \right) \cdot \frac{8}{3M} \quad (4)$$

where F_{SF} and ξ_{SF} indicate the closed-loop gain and the noise excess factor of the pixel source follower [6], C_p and C_s represent the column parasitic capacitance and the sampling capacitance of the first stage of the ADC. The second, the third and the fourth terms of the equation respectively indicate the thermal noise of the ADC sampling switch, the thermal noise of the ADC building blocks and the quantization noise. A simulation of the temporal noise of the stacked and CIS architectures at 8K resolution (4320 pixels/column) is shown in Fig. 8. The parameters F_{SF} and ξ_{SF} are respectively 1.8 and 2 while the ADC is designed such that the $\overline{V_n^2}_{,ADC}$ is negligible. Due to the large capacitive load as the result of 4320 pixels sharing the same column bus, according to (4) the CIS architecture has a lower thermal noise. At 200 ADC clock cycles, the temporal noise of the stacked architecture is 74μV, about 22μV higher than that of the CIS. This noise difference can be reduced by increasing the number of clock cycles in the stacked implementation or by adding extra capacitive load at the second tier.

B. Frame rate analysis

Although it increases the thermal noise, the low sub-column capacitance is very useful for increasing the frame rate of the stacked architecture. A simplification of the total pixel readout time with DCDS, its settling time and the correspondent imager frame rate are expressed as:

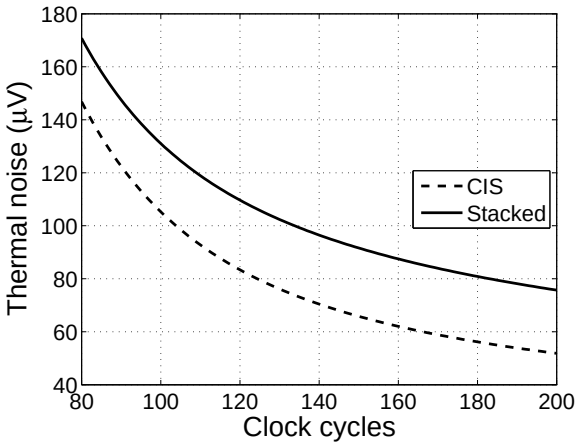

Fig. 8. Simulated temporal noise at the output of the pixel SF as a function of the number of clock cycles of the ISD ADC at 8K resolution. The noise is about 22μV lower in the CIS case due to the filtering effect of the large parasitic capacitance of 4320 pixels sharing the same column.

$$T_{row} \simeq T_{reset} + T_{TG} + 2 \cdot T_{sett} + 2 \cdot T_{ADC} \quad (5)$$

$$T_{sett} \simeq \frac{(C_p + 4 \cdot C_{bump}) \cdot \triangle V}{I_{bias}} \quad (6)$$

$$FR = \frac{1}{T_{row} \cdot N_{rows}} \quad (7)$$

where T_{reset} and T_{TG} indicate the time needed to reset the pixel floating diffusion node and the transfer gate time, respectively. $\triangle$V represents the pixel output voltage swing, I_{bias} represents the current biasing the pixel SF and FR represents the frame rate. In this analysis $\triangle$V is 1.6V, I_{bias} is 5μA, T_{reset} and T_{TG} are both 0.5μs while the clock speed of the ISD ADC is 20MHz and 200 clock cycles are used per conversion.

According to (5), the pixel readout time depends on both the settling time of the source follower and on the A/D conversion time. The stacked architecture allows both the reduction of N_{rows} and of T_{sett} due to the increased parallelism. Fig. 9 shows the simulation of the frame rate of a standard column parallel CIS and the proposed Stacked architecture at 33MPixel resolution and at variable pixel pitch. Both use the same ISD-ADC-based readout. According to (3) and (6), the settling time of a standard CIS architecture increases as the pixel pitch increases, reducing its frame rate. In contrast, the frame rate of the stacked architecture improves with the increase of the pixel pitch as the parallelism improves as well. From about 9μm pixel pitch, the frame rate of the stacked architecture is more than 2 orders of magnitude higher than the frame rate of the CIS architecture.

Ideally, even higher frame rates are achievable by the stacked architecture with smaller ADC area such as the 2700μm^2 of [16] and by increasing the clock speed (e.g. 50MHz). In practice, in the 8K resolution imager, the uppermost frame rate would be limited by the power consumption

and by the digital-data-rate speed. Readout architectures based on address event imaging (AER) [21] [22] can be used for reducing the data rate.

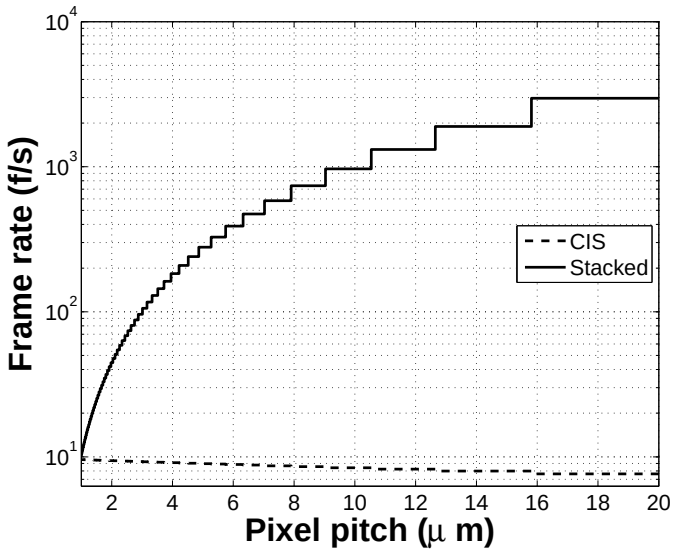

Fig. 9. Simulated frame rate of an 8K resolution sensor using the ISD-ADC-based readout at variable pixel pitch.

C. Experimental results

An image sensor test chip in a standard 180nm CIS technology has been designed and fabricated in order to verify the low-noise and the high-frame-rate capability of the proposed readout scheme based on ISD ADCs. The chip includes 10μm pitch pixels with pinned photodiodes and second-order FF ISD ADCs. A micro-photograph of the chip is shown in Fig. 10. Given the tolerance of the FF modulator towards coefficient variations, we used an ADC sampling capacitance as low as 50fF to achieve a compact size of the ADC for a higher parallelism. The total capacitance of the ADC is 500fF. The ADC area is 4000μm^2 which, combined with the 10μm pixel pitch, translates into 49 pixels/ADC (see (1)). Note that for sake of easy decoding, in this test chip we increased the number of pixels/ADC to 64 units.

The resolution of the designed imager is 128 x 256 pixels and corresponds to 16 x 4 BOPs, each having 8 sub-columns and 64 rows (see Fig. 10). As the imager is implemented in a single tier CIS technology, the ADCs are placed at column level and their number is limited to 128. In a stacked implementation (Fig. 2) and with the same resolution, the number of ADCs can increase to 512 since each BOP has 8 sub-columns and each sub-column has its own ADC. Furthermore, in the stacked implementation, the ADC at tier 1 would lie in a rectangular shape area, simplifying and potentially reducing the layout area.

The digital signals used to control the chip are generated externally through FPGA for flexibility and for implementing different testing options. The chip contains 97 pads and the clock speed is 20MHz. Each A/D conversion uses 200 clock cycles in order to achieve low noise and requires 10μs per conversion consuming 200μW per ADC. Fig. 11 shows the INL and the DNL of the ADC. The DNL is within -0.6/0.8 LSB while the maximum INL value reaches 6 LSB and corresponds to 0.05% ADC non-linearity.

Fig. 12 shows a picture taken by the implemented imager in low-light conditions with the ADC using 50 and 200 clock cycles per conversion. The averaging effect of the ISD ADC is clearly seen at higher clock cycles numbers.

The measured read noise of the designed imager is 70μV which, with a pixel conversion gain of 50μV/e^- translate into 1.4e$^-$ and is slightly higher than the value derived by (4). A possible explanation of the difference in noise performance is the increased contribution of the 1/f noise of the pixel SF. In a real stacked implementation, as only 49 pixels instead of 256 would contribute to the load capacitance, the thermal noise component is expected to increase by about 14μV according to (4).

The row readout time is 21.4μs. Since each sub-column of the BOP has 64 rows, the frame rate of the parallel BOP architecture corresponds to 730fps. In the real stacked implementation the frame rate can further increase. As explained above, the parallelism can increase up to 49 pixel/ADC, therefore the frame rate is expected to become 960fps.

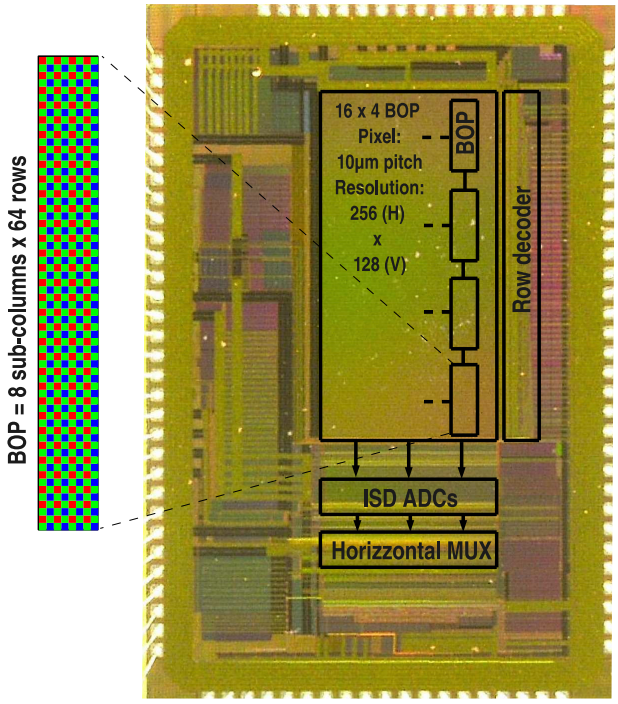

Fig. 10. Micro-photograph of the designed chip. The 128 x 256 pixel array is divided into 16 x 4 BOP each containing 8 sub-columns and 64 rows.

A comparison of this work to another readout architecture for stacked imagers, also validated through a conventional CIS technology [9], and two works representing the state of the art in CIS technology with column parallel F-I/Cyclic ADC [23] and ISD ADC [16] is shown in Table I. Improvements of this work include the parallelism, the read noise and the frame rate.

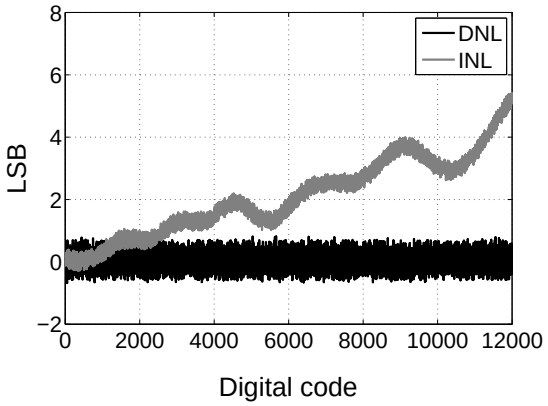

Fig. 11. The DNL is within -0.6/0.8 LSB while the INL max is 6 LSB.

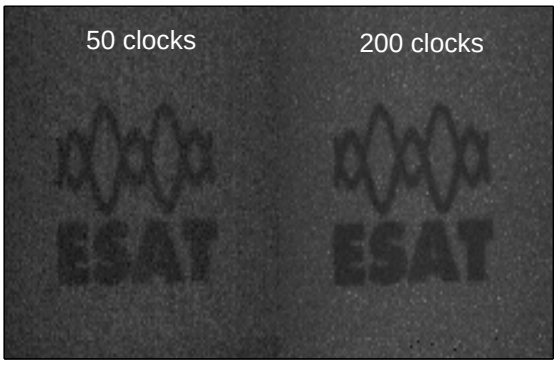

Fig. 12. Low light sample image taken at 180fps with 50 and 200 clock cycles per ADC.

TABLE I
PERFORMANCE COMPARISON

Parameter	**Value**			
	This work	**[9]**	**[23]**	**[16]**
Architecture	**Stacked**	Stacked	CIS	CIS
Decoding type	**1D**	2D	1D	1D
Resolution (Mpixel)	**indep.**[1]	indep.[1]	2.5	2.1
Parallelism (pixels/ADC)	**64**	24576	1028	1212
Pixel	**4T**	2.5T, 2D	4T	4T
Pixel pitch (μm)	**10**	2.8	7.1	2.25
Conversion gain ($\mu V/e^-$)	**50**	37	22.8[2]	80
Frame rate max. (fps)	**730**	100	30	120
DR (dB)	**80**	52	87.5[2]	75
Read noise (e^-)	**1.4**	15.6	3.7[2]	1.9
Voltage (V)	**3.3**	-	3.3V(A) 1.8V(D)	2.8V(A) 1.2V(D)
ADC architecture	**ISD**	-	F-I/ Cyclic	ISD
ADC res. (bit)	**13.5**	-	17	13
Power (mW)	**40**	19[3]	466	180

[1]constant parallelism hence, ideally, constant noise and FR at any resolution
[2]WDR type pixels
[3]w/o analog buffer and w/o ADCs

V. CONCLUSION

In this paper we presented a low-noise, high-frame-rate parallel readout architecture for 8K stacked image sensors based on block-of-pixels and blocks-of-ADCs processing. In contrast with the state-of-the-art of stacked technology concepts which employ 2D-pixel decoding, we have proposed a novel decoding system which allows a simple 1D decoding. Transitioning from 2D decoding to 1D decoding not only lowers the complexity of the imager but also ensures a uniform pixel distribution and reduces the pixel control lines and the minimum number of transistors per pixel by 1 unit.

Moreover, we have addressed the ADC and bump-bonding yield issue. The proposed architecture allows the placement of multiple micro-bumps per ADC reducing the micro-bump yield impact. Furthermore, as each ADC converts a sub-column of pixels of the BOP, its failure can be compensated by interpolating the pixels form the neighboring sub-columns.

Our analysis showed that the proposed stacked architecture can achieve low noise and high frame rate when combined with incremental-sigma-delta ADCs. To verify the low-noise and high-frame-rate capabilities, we implemented a test chip including 16 x 4 BOP array and ISD ADCs in a standard 180nm CIS technology. We measured a read noise of 1.4e- at a pixel readout time of 21.4μs. As each block-of-pixels is composed of 64 rows, the equivalent frame rate is as high as 730fps. In a real stacked implementation with 8K resolution, the frame rate is expected to further increase to about 960fps, at the cost of a slight increase in thermal noise by 14μV due to the reduced sub-column parasitic capacitance.

We conclude that the use of a stacked technology together with ISD ADCs is a powerful combination which can achieve high frame rate and low noise at large-spatial-resolution imagers.

ACKNOWLEDGEMENTS

The authors would like to thank T. Geurts, G. Chapinal and J. Compiet from ON Semiconductor for the valuable discussions and for the help in the design.

The authors acknowledge the financial support of the IWT SBO project 3SIS.

REFERENCES

[1] A. Theuwissen, "Cmos image sensors: State-of-the-art and future perspectives," in *Solid State Circuits Conference, 2007. ESSCIRC 2007. 33rd European*, sept. 2007, pp. 21 –27.
[2] I. Takayanagi and J. Nakamura, "High-resolution cmos video image sensors," *Proceedings of the IEEE*, vol. 101, no. 1, pp. 61–73, 2013.

[3] T. Watabe, K. Kitamura, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33mpixel 120fps cmos image sensor using 12b column-parallel pipelined cyclic adcs," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 388–390.

[4] Ishikawa, "New application areas made possible by high speed vision," in *International Image Sensors Workshop*, 2011.

[5] B. Cremers, M. Innocent, C. Luypaert, J. Compiet, I. C. Mudegowdar, C. Esquenet, G. Chapinal, W. Vroom, T. Blanchaert, T. Cools, J. Decupere, R. Aerts, P. Deruytere, and T. Geurts, "A 5 megapixel, 1000fps cmos image sensor with high dynamic range and 14-bit a/d converters," in *IISW*, 2013.

[6] S. Kawahito, "Signal processing architectures for low-noise high-resolution cmos image sensors," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, 2007, pp. 695–702.

[7] M.-W. Seo, S.-H. Suh, T. Iida, T. Takasawa, K. Isobe, T. Watanabe, S. Itoh, K. Yasutomi, and S. Kawahito, "A low-noise high intrascene dynamic range cmos image sensor with a 13 to 19b variable-resolution column-parallel folding-integration/cyclic adc," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 1, pp. 272–283, 2012.

[8] R. Njuguna and V. Gruev, "Low power programmable current mode computational imaging sensor," *Sensors Journal, IEEE*, vol. 12, no. 4, pp. 727–736, 2012.

[9] S.-F. Yeh, C.-C. Hsieh, and K.-Y. Yeh, "A 3 megapixel 100 fps 2.8μm pixel pitch cmos image sensor layer with built-in self-test for 3d integrated imagers," *Solid-State Circuits, IEEE Journal of*, vol. 48, no. 3, pp. 839–849, 2013.

[10] K. Kiyoyama, K. W. Lee, T. Fukushima, H. Naganuma, H. Kobayashi, T. Tanaka, and M. Koyanagi, "A block-parallel signal processing system for cmos image sensor with three-dimensional structure," in *3D Systems Integration Conference (3DIC), 2010 IEEE International*, 2010, pp. 1–4.

[11] S. Sukegawa, T. Umebayashi, T. Nakajima, H. Kawanobe, K. Koseki, I. Hirota, T. Haruta, M. Kasai, K. Fukumoto, T. Wakano, K. Inoue, H. Takahashi, T. Nagano, Y. Nitta, T. Hirayama, and N. Fukushima, "A 1/4-inch 8mpixel back-illuminated stacked cmos image sensor," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 484–485.

[12] A. Xhakoni, D. San Segundo Bello, and G. Gielen, "Impact of tsv area on the dynamic range and frame rate performance of 3d-integrated image sensors," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2012*, 2012, pp. 836–839.

[13] T. Toyama, K. Mishima, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, and N. Fukushima, "A 17.7mpixel 120fps cmos image sensor with 34.8gb/s readout," in *IISW*, 2011.

[14] J. Aoki, Y. Takemoto, K. Kobayashi, N. Sakaguchi, M. Tsukimura, N. Takazawa, H. Kato, T. Kondo, H. Saito, Y. Gomi, and Y. Tadaki, "A rolling-shutter distortion-free 3d stacked image sensor with -160db parasitic light sensitivity in-pixel storage node," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 482–483.

[15] S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10000 frames/s cmos digital pixel sensor," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 12, pp. 2049 –2059, dec 2001.

[16] Y. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 m pixels, 120 frame/s cmos image sensor with column-parallel delta sigma adc architecture," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 1, pp. 236 –247, jan. 2011.

[17] Y. Chen, Y. Xu, A. Mierop, and A. Theuwissen, "Column-parallel digital correlated multiple sampling for low-noise cmos image sensors," *Sensors Journal, IEEE*, vol. 12, no. 4, pp. 793–799, 2012.

[18] L. Yao, M. S. J. Steyaert, and W. Sansen, "A 1-v 140- mu;w 88-db audio sigma-delta modulator in 90-nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 11, pp. 1809–1818, 2004.

[19] J. Markus, J. Silva, and G. Temes, "Theory and applications of incremental delta; sigma; converters," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 51, no. 4, pp. 678 – 690, april 2004.

[20] S. Matsuo, T. Bales, M. Shoda, S. Osawa, K. Kawamura, A. Andersson, M. Haque, H. Honda, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi, "8.9-megapixel video image sensor with 14-b column-parallel sa-adc," *Electron Devices, IEEE Transactions on*, vol. 56, no. 11, pp. 2380–2389, Nov 2009.

[21] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128 128 120 db 15 s latency asynchronous temporal contrast vision sensor," *Solid-State Circuits, IEEE Journal of*, no. 2, pp. 566–576.

[22] J. Leero-Bardallo, T. Serrano-Gotarredona, and B. Linares-Barranco, "A 3.6 μ s latency asynchronous frame-free event-driven dynamic-vision-sensor," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 6, pp. 1443–1455, 2011.

[23] M.-W. Seo, T. Sawamoto, T. Akahori, T. Iida, T. Takasawa, K. Yasutomi, and S. Kawahito, "A low noise wide dynamic range cmos image sensor with low-noise transistors and 17b column-parallel adcs," *Sensors Journal, IEEE*, vol. 13, no. 8, pp. 2922–2929, 2013.