A Stacked Full-Bridge Topology for High Voltage DC-AC Conversion in Standard CMOS Technology

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***Abstract*—A monolithic DC-AC converter is realized in a $130\ \mathrm{nm}$ $1.2\mathrm{V}$ CMOS technology using a Class-D half-bridge topology. Several dies are combined to achieve a full-bridge topology, realizing a bipolar output voltage. Using a stacking technique, this output voltage can be increased. This yields AC output voltages up to $4\mathrm{V}$, which is more than three times the nominal $1.2\mathrm{V}$ supply voltage of the technology. The passives are integrated on-chip. Consequently, the bill of materials (BOM) is heavily reduced. In a standard half-bridge topology, bulky external capacitors are needed to filter out the DC offset. This main obstacle of an off-chip capacitor is alleviated in the full-bridge topology, reducing the BOM even more. An output peak-to-peak voltage of $3.8\mathrm{V}$ is achieved at a maximal efficiency of 58.3%. A total output power of $56\mathrm{mW}$ is obtained.**

I. Introduction

On-chip power conversion techniques are used more and more since they enable a reduced bill of materials and increase the flexibility for the system design. Recent research results have shown the feasibility of fully-integrated DC-DC converters in standard CMOS technologies [1]. A following gap to bridge is the integration of DC-AC conversion. DC-AC converters, also known as power inverters, are extensively used nowadays. Typical applications are inverters used in photovoltaic panels, cold cathode fluorescent lamps (CCFL), motor drivers and uninterruptible power supplies. In all these applications, industry strives towards more low-cost solutions. The DC-AC converter is typically a bulky block which is a barrier to go towards smaller and cheaper systems. The ability to integrate this block is thus gaining more and more interest. Moreover, even higher output frequencies can be generated with an on-chip solution, enabling the control of micro scale piezoelectric motors and magnetic machines which require driving frequencies up to and above 100kHz.

The biggest challenge in this integration is the limit imposed by the low supply voltages in standard CMOS technologies. These constrain the output voltage to be within the defined supply voltage. At higher voltages outside of the nominal range, breakdown mechanisms and hot carrier effects will be present. Non-standard CMOS technologies can be used [2] to solve this, but introduce an extra cost.

In this paper, a monolithic full-bridge topology is proposed and designed in a standard 130 nm CMOS technology. The topology enables a high output voltage by the combination of two separate stacked half-bridges, as depicted in Figure 1. Every half-bridge consists of two series-stacked dies to increase the output voltage. The generated output swing is more than three times the nominal supply voltage, without exceeding the nominal operating conditions of the devices in the separate dies. By combining two half-bridges, there will be no DC-offset present in the output voltage. Moreover, this method enables the elimination of the output LC low-pass filter that is needed otherwise [3]. Removing these external components for the LC filter decreases the volume so that the complete DC-AC converter can be smaller and cheaper.

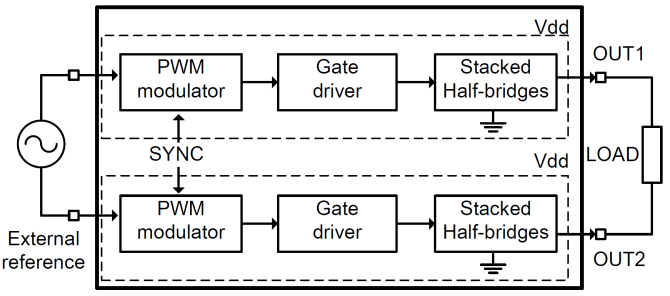

Fig. 1. System overview for the full-bridge high voltage DC-AC converter.

The system is described in section II, the implementation of the circuits is discussed in section III. The measurement results are presented in section IV. Finally, conclusions are drawn in section V.

II. System description

A. Half-bridge Class-D inverter

The basic building block for the proposed full-bridge system is the half-bridge class-D inverter topology. This topology is depicted in Figure 2. This circuit consists of two large power switches SW_p and SW_n, an on-chip inductor L_S and a combined MOS and MIM capacitor C_{out}. The class-D inverter is fed by a supply voltage V_{DD}. The gate drive circuit is controlling the switches using non-overlapping control signals. The high frequency control signal is generated in the pulse width modulation (PWM) block. For the PWM-generation, an off-chip reference signal is compared to an on-chip generated sawtooth waveform. This comparison is made in the on-chip OTA. The on-chip sawtooth is generated at a frequency of 80 MHz. An external low-voltage input reference waveform is applied to the half-bridge. This can be a low-frequency signal, such as a 50 Hz sine. In this case, the

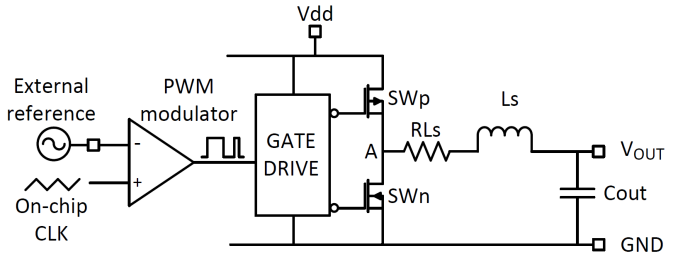

Fig. 2. Topology for the half-bridge class-D inverter.

output of the OTA is a pulse-width modulated signal at 80 MHz carrier frequency with a 50Hz modulation superposed on the carrier, which is needed to drive the power switches.

At node A, a modulated high-frequency carrier is now generated. Since the frequency of this signal is much higher than the input reference signal, the low-pass filter constituted of the on-chip inductor L_S and capacitor C_{out} has a low cutoff frequency compared to the switching frequency. A Fourier analysis indicates that these higher order harmonics can now be neglected [4]. The resulting output signal V_{OUT} is a sine wave with a peak-to-peak voltage equal to the supply voltage V_{DD}, a DC-offset equal to $V_{DD}/2$ and a frequency equal to the input reference in an ideal class-D amplifier [5].

B. Combination towards full-bridge

A half-bridge produces a unipolar output voltage with a DC-offset. For inverter applications, one is interested in bipolar output voltages without DC-offset. A technique to achieve this is the differential connection of a load over two half-bridge converters. Two half-bridge blocks can now be combined into a full-bridge. This system is depicted in Figure 1 and Figure 3. By variation of the duty cycle, a sinusoidal output voltage can be obtained. If half-bridge 1 produces an output voltage $V_{OUT,1}$ and half-bridge 2 produces an output voltage $V_{OUT,2}$, then the voltage V_{load} over the load is given by:

$$V_{load} = V_{OUT,1} - V_{OUT,2} \tag{1}$$

The output voltages $V_{OUT,1}$ and $V_{OUT,2}$ are both positive voltages. They are the output waveforms of two half-bridges with a supply of $V_{DD} = 1.2V$. These waveforms are depicted in Figure 3. Both half-bridges are synchronized at $180°$ out of phase. The PWM duty cycle of both half-bridges needs to be complementary for this. This means that if $V_{OUT,1}$ increases, $V_{OUT,2}$ will decrease and vice versa. Both output waveforms have a DC-offset of $0.6V$. From equation (1) follows that the load voltage V_{load} can either be positive or negative. There is no DC offset voltage in V_{load} which allows to eliminate an external capacitor to filter off this offset.

The circuit in Figure 3 can now be simplified. The capacitors can be combined over the load and the two series inductors can be lumped. This is done in Figure 4. The current through the load Z_{load} switches direction every cycle. One can now conclude that the combination of two half-bridges is the equivalent of a full-bridge topology [6]. In this way, it would be possible to combine more than two half-bridges and derive multi-phase systems as well.

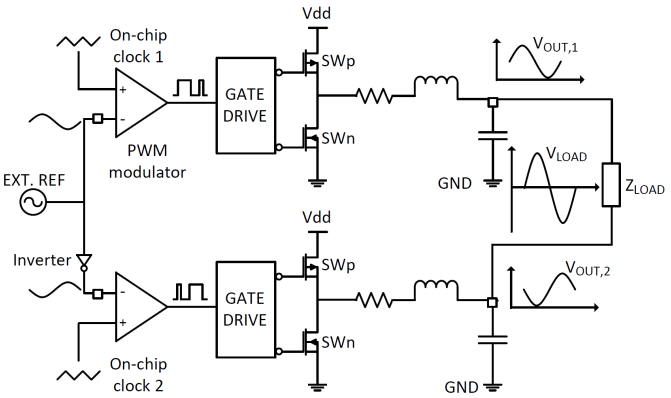

Fig. 3. Two combined half-bridges.

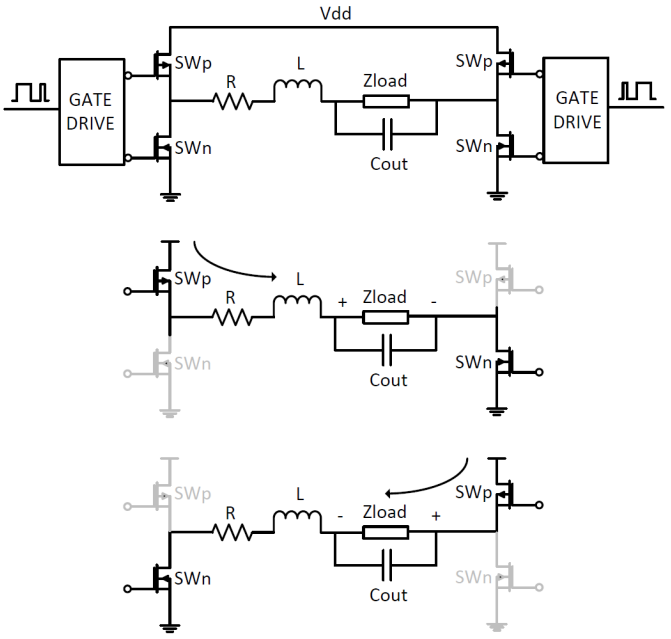

Fig. 4. Full-bridge as an equivalent circuit for two combined half-bridges.

C. Series stacking for higher output voltage

In this work, the implementation of the half-bridge class-D inverter enables series stacking using a dedicated on-chip level shifter. This provides the possibility to serialize different dies into a multi-stage stacked class-D system [7]. It is now possible to achieve higher output voltages than the nominal supply voltage, while still operating within the nominal voltage limits for the CMOS technology on every single die. This principle is explained in Figure 5 for two series-stacked dies.

Stage 0 is the first die. An external low-voltage reference waveform (e.g. a 50 Hz sine wave) is applied to this half-bridge class-D inverter. The PWM control signal is generated on-chip and applied to the switches. This results in an output signal $V_{STAGE,0}$ with a peak-to-peak voltage equal to the supply voltage V_{DD} as explained in section II-A. This first die has a stand-alone voltage supply $V_{S,0}$. The control signal is buffered and brought off-chip as drive signal $V_{DRIVE,0}$. The output signal $V_{STAGE,0}$ is now used as a ground reference

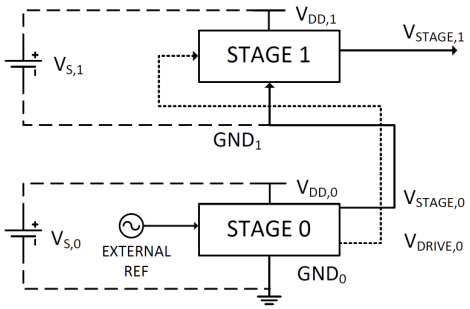

Fig. 5. Series stacking of two half-bridge class-D inverters.

for the second die, *Stage 1*. The signal can be described as follows:

$$V_{STAGE,0} = \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S,0} \tag{2}$$

The second die is exactly the same half-bridge topology as the first die. The control signal used in this second stage is $V_{DRIVE,0}$. It can be applied to the second stage using the on-chip level shifter on the second die. A separate supply, $V_{S,1}$ is used for Stage 1. The drive signal is level-shifted to be between $V_{DD,1}$ and GND_1, where $V_{DD,1} - GND_1 = V_{S,1}$. Since the ground-reference for Stage 1 is equal to $V_{STAGE,0}$, the output voltage of Stage 1 can now be derived:

$$\begin{aligned} V_{STAGE,1} &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S1} + GND_1 \\ &= \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_{S1} + V_{STAGE,0} \end{aligned} \tag{3}$$

Since the separate voltage sources $V_{S,0}$ and $V_{S,1}$ have the same DC voltage V_S, one can now derive the following expression by substituting equation (2) in (3):

$$\begin{aligned} V_{STAGE,1} &= 2 * \frac{1}{2}(1 + sin(2\pi f_{ref} t)) * V_S \\ &= 2 * V_{STAGE,0} \end{aligned} \tag{4}$$

By stacking two half-bridges in series, the output voltage for a combined load over the two stages is now doubled. This can also be extrapolated for a combination of more than two stages.

D. Stacked class-D full-bridge

The series stacked half-bridges can now be combined into a full-bridge topology as described in section II-B. This combination is schematically depicted in Figure 6, with the according output waveforms for every half-bridge and the output voltage. Since the upper and lower half-bridges in Figure 3 are now replaced by series stacked half-bridges, the output voltage over the common load now rises from V_{load}, cf. equation (1), to $2 * V_{load}$. In this way, the total peak-to-peak voltage over the load can rise up to four times the supply voltage while still respecting the nominal voltage limits in every single die.

III. Circuit Implementation

A. On-chip components

The on-chip output capacitor C_{out} is a combination of MOS and MIM capacitors. In this way, the highest possible

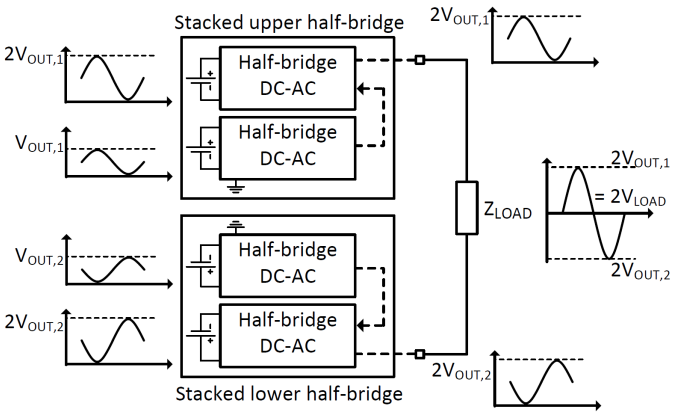

Fig. 6. System overview of the stacked class-D full-bridge. Left-hand side plots indicate output waveforms of the four separate half-bridges. Right-hand side plots indicate output waveforms over the load Z_{LOAD}.

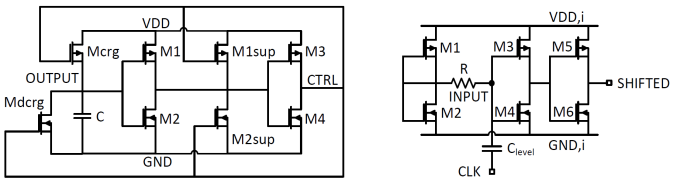

Fig. 7. Circuit implementation for the Schmitt-trigger based sawtooth generator (left) and the level shifter (right).

density can be achieved. This combined total output capacitance is $2.5nF$. The MIMCAP blocks are visible on the die photograph in Figure 8. The on-chip inductor L_S is designed as an octagonal metal track hollow spiral inductor. It has a total inductance of $10nH$. The series resistance is 2Ω at a switching frequency of 100MHz. The total area used by the inductor is $430\mu m$ x $430\mu m$. The inductor is visible in Figure 8 in the top left-hand side. The power switches SWp and SWn are implemented using a fingered layout. The width of these switches is $3.6mm$ and $1.4mm$, the on-resistance is 0.5Ω. A buffer train is used to apply the non-overlapping clock to the switches.

B. PWM generation

Due to the limited sizes of the on-chip passives, a high on-chip switching frequency will be needed to achieve high-efficiency power conversion. As already indicated in section II, an on-chip sawtooth waveform is needed to generate a high frequency PWM control signal for the switches. This is achieved using a Schmitt-trigger circuit in combination with an on-chip MIMCAP C of $1pF$. The circuit is given in Figure 7 on the left-hand side. The size of the capacitor C determines the frequency of the sawtooth.

C. Level shifter

The circuit of the level shifter is given in Figure 7 on the right-hand side. Using an on-chip MIM-capacitor C_{level}, the external drive signal CLK can be delivered to the chip. In this way, it can be shifted and used as a control signal for the switches. The size of the capacitor is $5pF$. The GND_i signal will be a sinusoidal output waveform of a previous die which

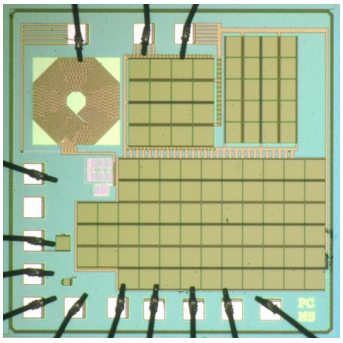

Fig. 8. Die photograph of the half-bridge inverter.

TABLE I. PERFORMANCE CHARACTERISTICS

Parameter	Value
Output power	$56\ mW$
Efficiency	58.3%
Peak-to-peak output voltage	$3.8V$
THD+Noise	15% at $56\ mW$
R_{ON} mosfets	0.5Ω
On-chip passives	$L = 10nH, C = 2.5nF$
Die size	$2.25mm^2$
$R_{load} = 30\Omega$, $f_{REF} = 440Hz$, $V_{DD} = 1.2V$	

yields a sinusoidal $V_{DD,i}$ as well. The on-chip poly resistor R in the level-shifter circuit will ensure that the DC voltage of the input node is always exactly between $V_{DD,i}$ and GND_i.

D. Combination of four dies

Two PCB's were made, one for every half-bridge. On every PCB, two dies are combined into a series stacked half-bridge as described in section II. The common load is connected between the outputs of both PCB's. Figure 1 depicts how both PCB's are connected. The upper dashed area can be seen as one PCB, the lower dashed area as a second PCB. A resistive load of 30Ω is connected over the outputs of both PCB's.

IV. MEASUREMENTS

A monolithic half-bridge class-D inverter is implemented in a $130\ nm$ $1.2\ V$ CMOS technology. It measures $1.5\ mm$ x $1.5\ mm$. Figure 8 shows a die photograph of the half-bridge DC-AC converter. Four of these dies are combined to achieve the full-bridge topology, as described in section II. This topology is realized using two PCB's, each containing two series stacked half-bridges using inter-die bonding. Four separate voltage supplies are used, generating a stand-alone $1.2\ V$ supply for the separate dies. Figure 9 shows the output waveform when an input reference sine is applied at 440Hz with a $200\ mV$ peak-to-peak voltage. The system works for references up to 100kHz. The output waveform is applied to a load of $30\ \Omega$, yielding a peak-to-peak amplitude of $3.8V$. This yields a total measured output power of $56\ mW$ at a maximum efficiency of 58.3%. The total harmonic distortion (THD+N) of the output waveform is 15% at this maximum output load. The efficiency of the complete full-bridge converter in function of the output current is given in Figure 10. The maximum efficiency is reached at a measured output current of $42\ mA$, which corresponds to a resistive output load of $30\ \Omega$. The performance characteristics are summarized in Table I.

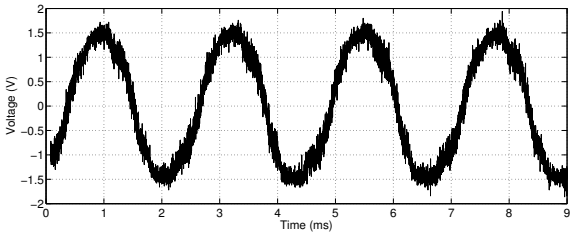

Fig. 9. Output waveform for the full-bridge topology.

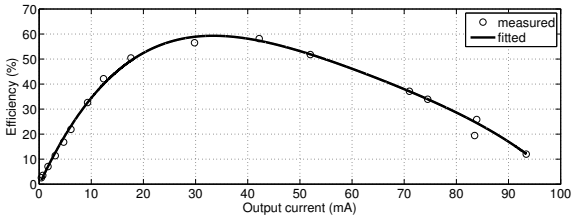

Fig. 10. Efficiency versus output load current.

V. CONCLUSION

A monolithic DC-AC converter is realized in a $130\ nm$ $1.2V$ CMOS technology using a class-D half-bridge topology. The passives are integrated on-chip. Four dies are combined to achieve a full-bridge topology, using a series stacking technique in the upper and lower half-bridges. This enables a higher AC output amplitude, more than three times the nominal supply voltage. By integrating the passives on-chip, the bill of materials (BOM) is heavily reduced. No bulky external capacitors are needed anymore to filter out the DC offset, reducing the BOM even more. An output peak-to-peak voltage of $3.8\ V$ is achieved at a maximal efficiency of 58.3%. A total output power of $56\ mW$ is obtained.

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