A 265V_{RMS} Mains Interface Integrated in 0.35μm CMOS

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***Abstract*—A fully integrated 265V_{RMS} input AC-DC interface is demonstrated in a 0.35μm CMOS technology, requiring only 1 optional external low voltage SMD capacitor for improved performance. The converter can directly interface the universal line voltage (50-60Hz) and converts this into a regulated DC voltage of 3.3V. High input voltage operation is made possible through separation of the mains input from the active circuits by custom layout high voltage capable passive components in between. A compact model of an ideal AC-DC capacitive step-down converter is presented and the proposed circuit architecture is designed to mimic ideal operation and approach the maximum attainable power throughput accordingly. The prototype converter demonstrates a maximum output power of 12.7μW on a die area of 6mm^2 and enables integrated circuits to be supplied straight from the ubiquitous mains voltage, hereby circumventing the need for traditional converters using expensive and bulky high voltage discrete components.**

***Index Terms*—Fully integrated converter, capacitive, step-down, AC-DC converter**

I. Introduction

IN everyday integrated circuits a DC supply voltage is assumed to be available to power the IC. But where does it come from? Commonly used power sources have their origin in either harvested power or the mains grid, as the also often used batteries in mobile applications are just energy carriers and need to be recharged.

For the first option it is possible to harvest energy from various sources that are present in the surroundings. RF radiation, kinetical, thermal or solar energy can be harnessed using the appropriate harvester into an electrical output. This output can then be further converted and regulated by integrated power management circuits. However, the power output of a harvester is related to the power available in its environment and therefore is subjected to uncertainty. System down times may occur consequently which can last for extended periods of time.

Alternatively the mains grid proves to be a very reliable source of power with blackouts occuring less than once a year [1]. It is also widely available through an extensive infrastructure already in place. Unfortunately for integrated circuits the mains grid distributes power in the form of a high voltage low frequency sine wave, specified in regional standards. This generally requires converters employing costly high voltage discrete components such as a rectifier and a transformer [2], taking up significant PCB area.

In this work an integrated mains interface is proposed, eliminating the need for high voltage rated external components, drastically reducing the footprint. This approach encompasses the monolithic integration of a capacitive step-down interface that separates the active circuit from the high voltage input, enabling integrated circuits to operate straight from the mains as supply voltage. This feature opens up the mains as possible power source for application domains where the otherwise necessary discrete converter makes the solution infeasible or too expensive. Possible example applications are physically small low power systems that can not consider the mains as power source if it requires a bulky converter and consequently are limited to battery power and/or energy scavenging operation. The mains as power source implies in return that the system is stationary, for example to be used for in-building sensor applications.

Previous research in the area concentrated on the feasibility of a high voltage input integrated power supply by using the high voltage capability of a silicon on sapphire (SOS) technology [3] to implement circuits capable of interfacing the mains input. To circumvent the need for high voltage active circuits, a capacitive division of the input voltage has been presented by [4] to reduce the required voltage rating of the subsequent power management circuits. However, this capacitive division of the AC input voltage considerably lowers the total system power throughput due to limited rectifier diode on times, because the voltage division occurs before rectification. This work aims to combine the efficiency benefit of a capacitive step-down with a maximal power throughput by maximizing the rectifier diode on times. To that end the operation of a capacitive AC-DC step-down stage is examined, offering the benefit of decreased voltage rating for the subsequent active circuits, but with a maximal power throughput by eliminating the capacitive division before the rectification. The resulting demonstrator was measured for line input voltages from 85V_{RMS} up to 265V_{RMS} for both 50Hz and 60Hz and was able to supply a load current of 1.93μA and 2.87μA at 3.3V for the US and EU mains standards respectively.

This paper is organized as follows. Section II discusses the challenges of handling the mains as input voltage in an integrated circuit. The system architecture and operation are proposed in Section III. Section IV presents a model for an ideal capacitive AC-DC step-down converter, followed by the prototype implementation details in Section V. Measurements

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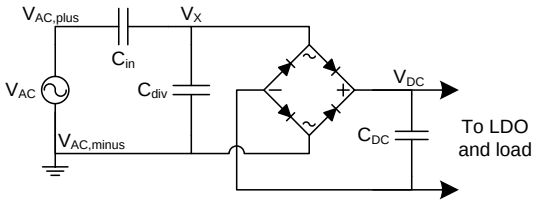
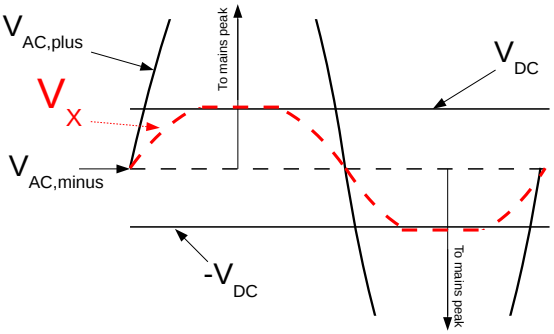
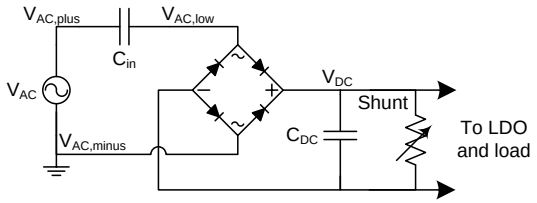


(a) Capacitive division topology: the mains amplitude is decreased by a capacitive division before rectification.

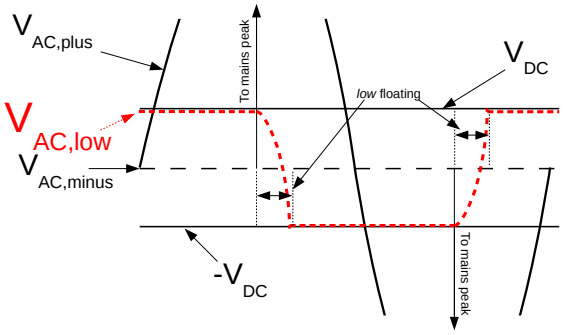


(b) Waveforms of the capacitive divider operation: limited power throughput due to V_X only surpassing V_{DC} near its peak.

Fig. 1.



(a) Proposed capacitve step-down: the step-down is set by the load and shunt current.



(b) Capacitive step-down operational waveforms.

Fig. 2.

results are reported in Section VI and final conclusions are drawn in Section VII.

II. High input voltage architecures

Interfacing voltages beyond the nominal rated device voltage generally requires special circuit techniques to prevent overvoltage from destroying the devices. Succesful techniques to do so include device stacking [5] [6], where cascoded devices each share a portion of the total voltage, and voltage domain stacking [7] in which multiple nominal voltage rails are serialized. However, even with these techniques the maximal achievable interface voltage is still limited to a few times the nominal rated supply voltage as the complexity to implement these techniques increases substantially for each added level of stacking.

When considering the mains voltage with a nominal peak voltages of $375V$ in the $265V_{RMS}$ case, it is clear that these techniques are inadequate and alternative approaches are needed. With the mains voltage input exceeding the rated voltage of the active circuitry by two orders of magnitude, it is required to create a voltage gap between the mains input and the active circuit. This can be achieved by placing a series impedance [3] over which the voltage is dropped. As discussed in [3], it is possible to use a resistor. Such an approach would have a very low efficiency due to the very large voltage drop and is therefore undesirable. On the other hand the possibility to use a capacitor is also discussed, which in the ideal case is lossless and thus a better choice.

Such a series capacitor approach is taken in the work of [4] in the form of a capacitive voltage divider, as shown in Fig. $1(a)$. The mains input voltage V_{AC} is divided by the combination of capacitors C_{in} and C_{div} to a safe lower value V_X, which can be handled by the rectifier and the rest of the active circuit. The divided voltage V_X is then rectified onto a smoothing capacitor C_{DC} and supplies current to a load. The maximal operation value for V_{DC} is found to be $\sqrt{2}V_{X,RMS}$, occuring when the load current is absent. Therefore it is required that the capacitive voltage division ratio r_{div} is chosen to fulfill $r_{div}\sqrt{2}V_{AC,RMS} < V_{rated}$ in order to guarantee that no overvoltage will take place at V_{DC} at the worst case condition when the load current is zero. Consequently, this necessary division ratio r_{div} reduces power throughput in all other load conditions as the rectifier diodes are only turned on when $V_X > V_{DC}$, which only occurs for a short time near the peak of V_X. When V_X decreases below V_{DC}, the rectifier diodes turn off until V_X goes below $-V_{DC}$. During this time C_{DC} buffers V_{DC}.

This work proposes to use a series capacitor as a capacitve step-down due to its interaction with the load and the power management regulation circuits located behind the rectifier, showing similarity to [3]. But other than in [3] however, this work targets the use of a CMOS technology by moving the high voltage towards the integrated passive components. And unlike [4] which guarantees safe operation at the worst case load by reducing the rectifier input voltage V_X, overvoltage is avoided by providing a proper current sinking capability after rectification by a shunt regulation path. This approach maximizes the rectifier diode on time as $V_{AC,low}$ floats at the rate of the mains when the rectifier is off, keeping t_{off} to a minimum. Hereby power throughput is optimal for a given amount of series capacitance, reducing the necessary capacitor size and cost in comparison to other approaches such as the capacitive division. Fig. 2(a) and 2(b) demonstrate the proposed concept.

III. Proposed system architecture and operation

The converter topology, shown in Fig. 3, combines an AC-DC step-down stage and DC post regulation stage. The first

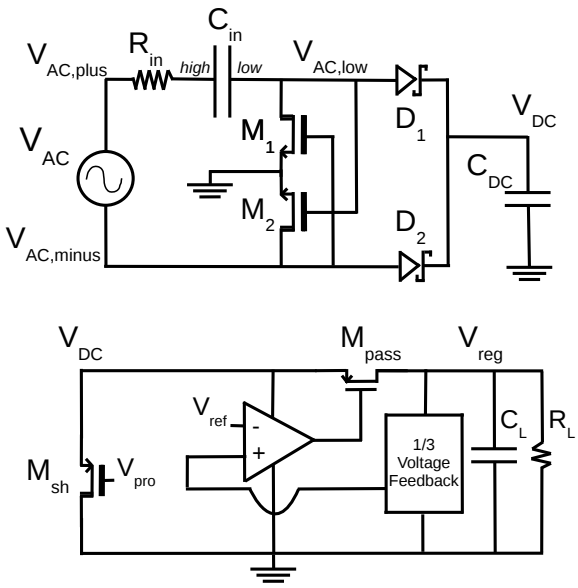


Fig. 3. System architecture of the proposed AC-DC converter.

stage consists of 2 high voltage capable passive components R_{in}, C_{in} and a full wave rectifier [8] forming the capacitive step-down. The output voltage of the AC-DC stage is determined by the combination of the load current and the post regulation stage, which is composed of a shunt path and a series regulator. While the shunt path ensures that V_{DC} is limited to a safe value, the series regulator removes any remaining ripple from V_{DC} into the regulated output voltage V_{reg}.

A. Capacitive AC-DC step-down

To understand the operation it is assumed for the sake of simplicity that $R_{in} = 0$, the rectifier is ideal ($V_{th,M1-M2} = 0, V_{D,D1-D2} = 0$), C_{DC} is infinite and charged to a voltage V_{DC}. With a mains RMS voltage (Fig. 2(b)) V_{AC} present at the input terminals ($V_{C_{in}} = 0$) and $V_{AC,plus}$ referred to $V_{AC,minus}$ increases from $0V$ up to V_{DC} devices $M1$, $D1$ and $D2$ remain off while $M2$ is on. Next for $V_{DC} \leq V_{AC,plus} \leq \sqrt{2}V_{AC}$, $D1$ turns on and current flows to C_{DC}. Immediately after the mains peak, $D1$ turns off followed soon after by $M2$ since the low terminal of C_{in} starts to float and decreases at the same rate as $V_{AC,plus}$ until a drop of $2V_{DC}$ has taken place. At that time $V_{AC,minus} - V_{AC,plus} = V_{DC}$ and $D2$ turns on, while $M1$ has already turned on just before, providing another current towards C_{DC}. This continues until the negative peak at which $D2$ turns off. The above operation continues to alternate.

Input series capacitor C_{in} separates the active circuit from the high input mains voltage. While the $high$ terminal of C_{in} is subjected to the full mains voltage, meaning a peak-to-peak voltage $V_{ptp,high}$ of $2\sqrt{2}V_{AC}$, this is not true for the low terminal ($V_{AC,low}$). The low terminal is bound by the rectified voltage V_{DC} resulting in a $V_{ptp,low} = V_{DC}$. An input series resistor is added, in addition to C_{in}, to protect the circuit against inrush current that occurs when the system is connected to the mains at the time of a high voltage or peak

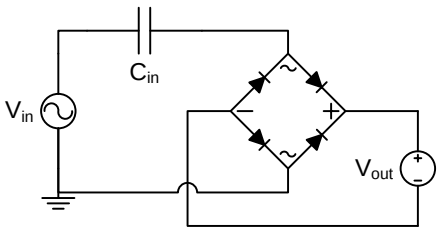


Fig. 4. Schematical representation of the ideal model with AC input voltage, a capacitor over which a voltage is dropped, an ideal rectification and a DC output voltage.

while C_{in} in not charged. Without resistor R_{in} a potentially destructive current charges C_{in}, only limited by the parasitic series resistance located between $V_{AC,plus}$ and $V_{AC,minus}$.

B. Shunt overvoltage protection and series regulation

Until now it was assumed that C_{DC} was infinite and fixed at V_{DC}, limiting $V_{AC,low}$ with respect to ground during both positive and negative mains half cycle. In practice this is guaranteed by the parallel combination of the shunt path and a low dropout (LDO) series regulator passing the current to the load. At nominal load the shunt path is inactive and all power passing the rectifier is consumed by the load, satisfying both $< |i_{C_{in,nom}}| > = i_{load,nom}$ and $V_{DC,nom} = V_{reg}$ (aside from the minimal dropout voltage). The resulting equilibrium of $V_{DC,nom}$ is given by V_{out} of Eq. (7), in which $< |i_{C_{in,nom}}| >$ equals the load current $i_{load,nom}$ for that nominal case.

When load power decreases to a lower level $i_{load,low}$, V_{reg} will be kept constant by the series regulator. This is not true for V_{DC} which will settle at a new equilibrium $V_{DC,low}$ in order to satisfy $< |i_{C_{in,low}}| > = i_{load,low}$. From Eq. (7) it can be seen that, for a given set of fixed parameters V_{in}, C_{in} and f_{mains}, this can only occur by increasing V_{out} (i.e. V_{DC}). The new $V_{DC,low}$ equilibrium can be calculated according to Eqs. (1)-(2). In conclusion this means that for a lower than nominal load current V_{DC} will easily exceed the safe operation voltage limit. For this reason a shunt path was included through M_{sh} in parrallel with the series regulator in order to limit V_{DC} to a maximum of $V_{pro} + V_{th,M_{sh}}$ at less than nominal loads as it allows $< |i_{C_{in}}| >$ to remain constant throughout any load current variation.

$$\frac{< |i_{C_{in,low}}| >}{< |i_{C_{in,nom}}| >} = \frac{4f_{mains}C_{in}(\sqrt{2}V_{in} - V_{DC,low})}{4f_{mains}C_{in}(\sqrt{2}V_{in} - V_{reg})} \quad (1)$$

$$V_{DC,low} = \sqrt{2}V_{in} - \frac{< |i_{C_{in,low}}| >}{< |i_{C_{in,nom}}| >}(\sqrt{2}V_{in} - V_{reg}) \quad (2)$$

IV. Converter model

This Section analyses the power throughput of a capacitive step-down stage in the ideal case, which is depicted in Fig. 4 and consists of an AC voltage source which is capacitively stepped down and ideally rectified to a DC output voltage. A compact calculation model is presented in Eq. (3) to (8).

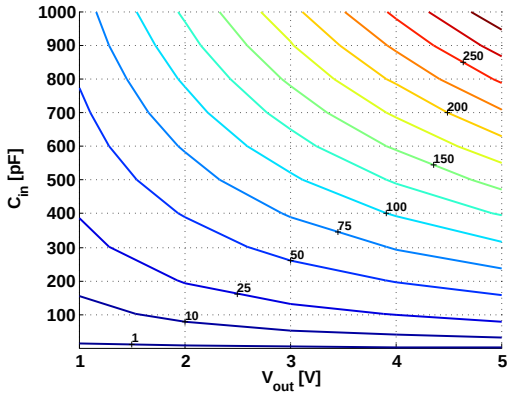


Fig. 5. Trade-off in achievable output power $[\mu W]$ as function of parameters C_{in} and V_{DC} for $V_{in,RMS} = 230V$ and $f_{mains} = 50$Hz.

The capacitive step-down introduces an impedance bottleneck as result of the low mains frequency and a low capacitance value for C_{in}. The latter is caused by the high voltage nature of capacitor C_{in} leading to a low capacitance density. Given the ideal representation in Fig. 4, it is now investigated what maximum attainable power throughput can be expected for an ideal AC-DC step-down. The power throughput is analyzed for the following set of system parameters: the mains amplitude V_{AC}, the mains frequency f_{mains}, the amount of series input capacitance C_{in} and the output voltage V_{out}.

$$V_{in}(t) = \sqrt{2}V_{in}sin(2\pi f_{mains}t) \tag{3}$$

$$V_{C_{in}}(t) \approx (\sqrt{2}V_{in} - V_{out})sin(2\pi f_{mains}t) \tag{4}$$

$$i_{C_{in}}(t) = C_{in}\frac{dV_{C_{in}}}{dt} \tag{5}$$

$$= C_{in}(\sqrt{2}V_{in} - V_{out})cos((2\pi f_{mains}t)) \tag{6}$$

$$2\pi f_{mains}$$

$$< |i_{C_{in}}| > = 4f_{mains}C_{in}(\sqrt{2}V_{in} - V_{out}) \tag{7}$$

$$P_{out} = < |i_{C_{in}}| > V_{out} \tag{8}$$

On one hand Eq. (3) represents the input voltage as function of time present at the high terminal of the capacitor C_{in}. On the other hand the low terminal of C_{in} exhibits a square wave pattern with amplitude V_{DC}. As a result of these voltages present at the capacitor terminals, the voltage over C_{in} can be approximated by Eq. (4). The capacitor current as function of time is then given by Eqs. (5)-(6). Averaging this over time consequently leads to the average capacitor current $< |i_{C_{in}}| >$ in Eq. (7), which can be combined with the ouput voltage V_{out} to calculate the output power P_{out} according to Eq. (8).

It can be seen in Fig. 2(b) that the proposed architecture operation constitutes voltages $V_{AC,low}$ and $V_{AC,minus}$ to exhibit block pulse like behaviour approaching the ideal case, i.e. an AC square wave output of the capacitive AC-DC step-down topology that is fed into the rectifier. This is opposed to previous work [4], in which the capacitive divided voltage V_X still looks like a sine wave. This results in suboptimal power throughput due to the fact that power is only transferred when the rectifier diodes turn on ($V_X > V_{rectified}$) which is limited by the slower voltage variation of V_X. Alternatively for this

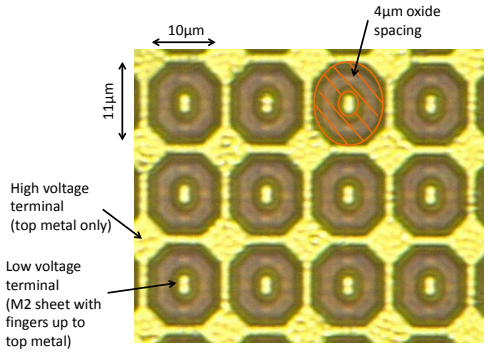


Fig. 6. Top view of high voltage fringe capacitor custom layout representation.

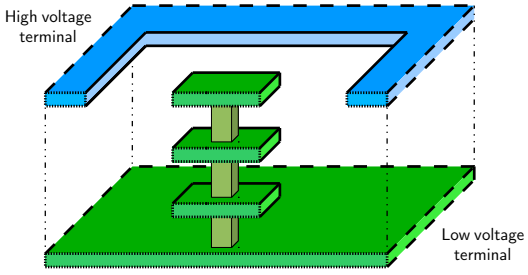


Fig. 7. Half unit cell of high voltage fringe capacitor conceptual crossection.

proposed architecture with its block pulse like rectifier input, the rectifier diode on times are significantly longer than for the sine wave rectifier input of [4], hence improving power throughput. A diode on time of 91% and 93% were achieved in this demonstrator for the US and EU mains cases respectively.

Since the mains voltage is already standardized, both system parameters V_{AC} and f_{mains} are fixed. Fig. 5 shows the output power capability of an ideal AC-DC stage as function of the two remaining degrees of freedom. A trade-off between input capacitance C_{in} and the ouput voltage V_{out} is observed.

On one hand when V_{out} is fixed, the average capacitor current $< |i_{C_{in}}| >$ of Eq. (7) is linearly influenced by the input capacitor C_{in} and consequently the output power given by Eq. (8) also scales linearly.

Alternatively, when keeping the series input capacitor constant, a higher output voltage V_{out} results in a lower average input capacitor current as can be seen in Eq. (7). However this effect is negligable for voltage values of V_{out} values below $50V$ and therefore the ouput power relation as function of V_{out} scales linearly in this region.

V. Implementation

A. High voltage passive components

Capacitor C_{in} bridges the high voltage gap between the high voltage mains input and the low voltages on-chip, as discussed in Section III. While the active circuits do not come in contact with high voltage, the input capacitor C_{in} and input resistor R_{in} are subjected to a maximum voltage of $\sqrt{2}V_{AC}$, up to $375V$ in the case of $V_{AC,RMS} = 265V$. With the oxide in the metal stack having a breakdown of at least $1\frac{MV}{cm}$ [9], a minimal spacing of $3.75\mu m$ in needed to ensure breakdown

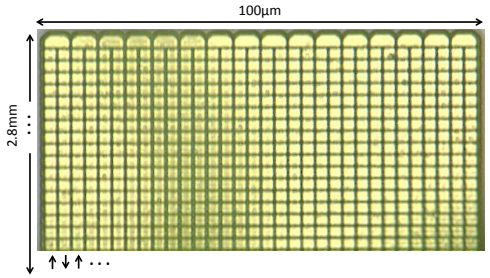


Fig. 8. High voltage resistor composed of meandering top metals and vias.

will not occur. To this end the input capacitor was implemented as a metal-metal fringe capacitor with at least $4\mu m$ of oxide between the capacitor plates. On top of that, metal corners were rounded to avoid the point effect. In Fig. 6 a top view of the custom layout of the capacitor is depicted and Fig. 7 shows a cross section of C_{in}. The half unit cell of Fig. 7 must first be mirrored over its front plane. The resulting unit cell can then be expanded to obtain the total capacitor. The high voltage plate is located solely in the top metal as to ensure sufficient spacing ($> 4\mu m$) to the low voltage terminal and the substrate. Voids are left in this high voltage plate through which the low voltage plate, mainly located lower in the metal stack, rises up to the top metal. This structure was found to maximize fringing while considering metal density reliability rules. Nevertheless capacitance density suffers from the widely spaced capacitor plates and 12.5 pF/mm^2 is achieved for this structure, resulting in a total of 50pF.

The input resistor is implemented using a series connection of vias and the top two metals in the stack, ensuring a large spacing to the substrate. Oxide spacing exceeds $6\mu m$ to ground to be able to withstand even higher voltages such as short spikes in the mains input. These result into additional inrush current events and consequently cause voltage drops across R_{in}, attenuating the voltage spike and relieving C_{in} in part. R_{in} was designed to be $32k\Omega$, with typical values after processing around $36k\Omega$.

B. Regulation circuits

A desired regulated output voltage V_{reg} of $3.3V$ after linear regulation of the rectified voltage V_{DC} superposed by an LDO dropout voltage V_{LDO} sets the minimum allowed value of V_{DC}. Achieving this headroom for series regulation while keeping $V_{DC,max}$ constrained to a safe operation value requires sufficient decoupling after the rectifier. The area underneath C_{in} therefore implements more than $10nF$ of NMOS capacitors. Besides its necessity for safe operation it also increases system efficiency as less noise needs to be regulated by the LDO. For these reasons the prototype converter can optionally be decoupled with an external low voltage $1\mu F$ SMD capacitor. Transistors $M1$ and $M2$ are implemented with available thick oxide DMOS devices, as part of a set smart power devices rated up to $25V$ available in the technology, to ensure safe rectifier operation while Schottky diodes $D1$ and $D2$ do not cause overvoltage issues towards substrate.

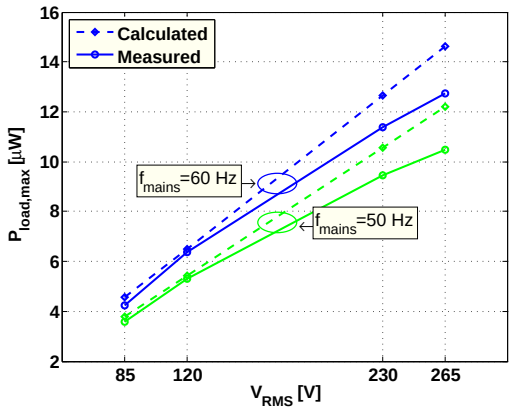


Fig. 9. Measured maximum output power for a regulated 3.3V output as function of mains specification, for a C_{in} of 50pF.

The post regulation stage has a dual function as previously mentioned. First, it is responsible for limiting the active circuit operation voltage by means of the shunt path. Secondly a series regulator chops off any noise that remains after the previous rectification.

1) Shunt path: Transistor M_{sh} is a thick oxide PDMOS device biased with an overvoltage protection control signal V_{pro}. When load power is decreased and V_{DC} increases above $V_{pro}+V_{th,M_{sh}}$ the PDMOS will start to conduct and will limit the maximum of the rectified voltage to a safe value.

Alternatively this shunt path can be adressed to shut down the converter. From Fig. 5 it follows that setting V_{DC} towards zero makes the output power P_{out} also collapse towards zero, achieving shutdown.

2) Low dropout Regulator: The LDO regulates the rectified voltage into a noise free output voltage V_{reg}. Considering the limited power budget available at the output from the AC-DC stage, it is imperative that power consumption of this regulator is low compared to the full budget in order to minimize the impact on system efficiency. Thus static currents in the error amplifier and feedback path were chosen to be $100nA$ and $50nA$ respectively. A Gain-bandwidth of 100kHz was achieved when loaded by the gate capacitance of M_{pass}, which can be sized relatively small due to the low current levels to be expected. The feedback path was chosen to be implemented by a diode connected stack of 6 subtreshold biased PMOS devices in order to create a high Ohmic $1/3$ voltage divider on a small chip area.

VI. Chip measurements

The converter prototype was measured for various mains voltage, frequency specifications. Fig. 9 shows the maximum achievable output power as function of the input mains RMS voltage ranging from $85V$, $120V$, $230V$ up to $265V$ and this for both 50Hz and 60Hz cases. It can be seen that the achievable load power scales linearly with the input RMS voltage, but does not reach its full calculated potential. This is due to the limited amount of buffer capacitor C_{DC} available

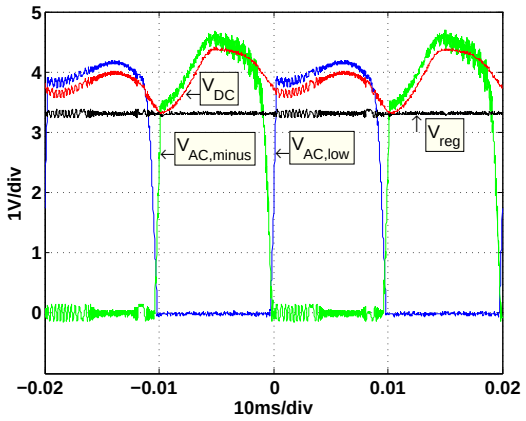


Fig. 10. Converter output waveforms for $V_{RMS} = 230V$, $f_{mains} = 50Hz$ input and $3.3V$ output, for a C_{in} of 50pF.

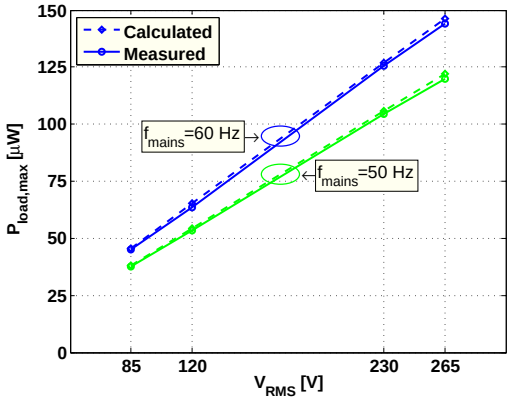


Fig. 11. Measured maximum output power for a regulated 3.3V output as function of mains specification, for two external C_{in} capacitors of each 1nF.

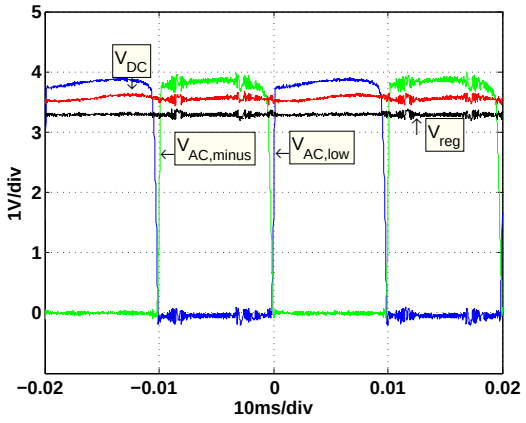


Fig. 12. Converter output waveforms for $V_{RMS} = 230V$, $f_{mains} = 50Hz$ input and $3.3V$ output for the external C_{in} capacitors of each 1nF.

on chip. An external low voltage SMD can optionally be used to alleviate this. When the input voltage frequency is 50Hz, the load power scales from $3.6\mu W$ for a $85V$ input up to a maximum of $10.5\mu W$ at $265V$. Similarly with a 60Hz frequency input the load power varies from $4.2\mu W$ up to $12.7\mu W$.

Fig. 10 shows the system voltage waveforms of both rectifier inputs, the rectifier output V_{DC} and the regulated output voltage V_{reg} for the typical EU mains input case. For an input voltage and frequency of $230V_{RMS}$ and 50Hz the converter supplies $9.5\mu W$. After series regulation of the ripple clearly visible in V_{DC} the regulated output voltage V_{reg} exhibits a noise of less than $150mV$ peak-to-peak, which is below 5% of V_{reg}. The waveform inputs of the rectifier show the presence of a parasitic coupling in the measurement setup. Signal $V_{AC,minus}$ contributes more input current than its complementary signal $V_{AC,low}$. This imbalance is due to the fact that the generated mains signal in the test setup is not solely AC coupled as it should be, but also exhibits some DC coupling to ground. Since the proposed topology of Fig. 3 only employs one series capacitor, the parasitic DC coupling to ground can propagate into the measurement via the path with no series capacitor. To avoid this, another measurement was performed with 2 external 1nF high voltage capacitors. Both mains connections to chip than contained a 1nF capacitor which were fed to the rectifier inputs. The according power is shown in Fig. 11 for the different mains input possibilities. In Fig. 12 it is now clear that the input power contribution of both mains half cycles are balanced, as would be expected of the topology.

For all tested input cases the output voltage V_{reg} can be regulated at a fixed $3.3V$ over the full load power range from zero up to the maximum achievable load power P_{load} as presented in Fig. 9 and Fig. 11. This proves the functionality of the shunt path provided by M_{sh}, allowing for overvoltage free and stable operation over the full load power range, and the series LDO regulator.

A chip microphotograph is shown in Fig. 13 and shows the die measuring $6mm^2$. Most of the area is occupied by the integrated high voltage capable passive components C_{in} and R_{in}. For area efficiency the NMOS capacitor decoupling device routed up to metal 1 is located underneath the actual high voltage series input capacitor C_{in}, which itself is fabricated using metals M2 and above. The stacking of these devices is possible without oxide breakdown because only the $high$ terminal of C_{in} is subjected to high voltage and is confined to the top metal.

Finally a comparison of the proposed converter with a prior state-of-the-art integrated AC-DC converter is given in Table I. The measurement results of this converter show increased power density, demonstrating the enhanced converter architecture proposed in this work. On top of that the input voltage range has been extended from $120V_{RMS}$ up to the a maximum of $265V_{RMS}$.

VII. Conclusion

In this work a high voltage capable capacitive AC-DC step-down interface is fully integrated in $0.35\mu m$ CMOS,

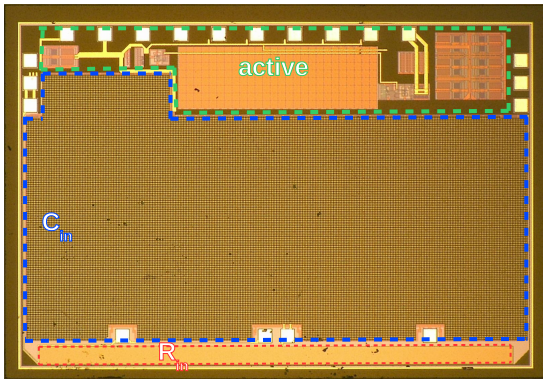


Fig. 13. Chip microphotograph

TABLE I
SPECIFICATION COMPARISON TO PRIOR ART.

Reference	[4]	This work	This work
Tech node	0.13μm	0.35μm	0.35μm
V_{RMS}	120V	120V	230V
f_{mains}	60Hz	60Hz	50Hz
Power/area	$0.43\mu W/mm^2$	$1.06\mu W/mm^2$	$1.58\mu W/mm^2$
V_{reg}	$4V$	$3.3V$	$3.3V$
$t_{on,diode}$	48%	91%	93.5%
$P_{out,max}$	$1.5\mu W$	$6.4\mu W$	$9.5\mu W$

altering the external components requirement from multiple high voltage devices to a single optional low voltage SMD for improved performance. The presented converter architecture ensures an optimal operation because voltages $V_{AC,low}$ and $V_{AC,minus}$ approach the AC square wave behaviour, as is the case of the ideal model, enabling maximal rectifier diode on times and hence maximal power throughput. The prototype measurements show achievable load powers of $6.4\mu W$ and $9.5\mu W$ in the most typical cases of $120V_{RMS}$, 60Hz and $230V_{RMS}$, 50Hz respectively. This while a fixed $3.3V$ regulated output can be supplied with a peak-to-peak voltage ripple of less than 5% over the full output power range.

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