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Monolithic Power Management Front End with High Voltage Dense Energy Storage for Wireless Powering

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Abstract—A monolithic power management system is proposed, enabling an energy storage density improvement of more than an order of magnitude with respect to the current state of the art. This is made possible by increasing the storage voltage V_{bat} towards 10V. A proof of concept prototype was designed in a 90nm bulk CMOS technology with an integrated 1.8mm dipole antenna using the surrounding energy available in the 5.8GHz ISM band. In order to achieve the large voltage conversion under aim of less than 100mV to 10V, a two stage approach is found necessary as the input impedance mismatch of a single stage passive voltage multiplier with the antenna would render the solution infeasible. First, the antenna voltage is passively rectified and multiplied to an intermediate system supply voltage V_{PMU} of 1.2V, after which this voltage is pumped up to the storage voltage level V_{bat} of 10V by an active DC-DC converter. This, for a minimal system startup voltage of 53mV.

Keywords—Wireless powering, on-chip antenna, AC-DC voltage multiplier, capacitive DC-DC converter, high voltage energy storage.

I. INTRODUCTION

Together with the increasing demand for radio frequency identification (RFID) and other stand-alone wireless systems such as in sensor networks, there is a growing need for custom power management units (PMUs) that enable proper operation of the load circuits for any given incident energy. The energy budget of wireless systems is typically low and the necessity to also wirelessly transfer data only complicates the use of this budget. It is therefore key to be able to store sufficient energy to sustain circuit operation until the end of an action, even when the incoming power level is low or zero.

This work investigates the issue of dense energy storage to enable improved performance in low cost, small size wireless powered circuits. Instead of storing the incident energy on a capacitor at less than 2V, this work proposes to use a much higher voltage to increase the stored energy by more than an order of magnitude. The storage density gained by such an approach can be valorised by having an increased energy budget for an identically sized system. Alternatively, the same energy budget can now be achieved with a relaxed specification for the storage capacitor. This can allow a previously external capacitor to be replaced by an integrated capacitor on chip, substantially decreasing the cost and size of the end solution.

Previously reported systems tackle the energy budget problem either using external components such as antennas to

Fig. 1. Block diagram of the proposed energy storage system.

boost the capture of incident power [1] and external storage capacitors to achieve a sufficient energy storage [2] or end up with a limited energy budget, but achieve full integration such as [3]. The integrated storage of [3] consists of a 6nF capacitor charged to 1.8V, which can be discharged down to 1.2V while a linear regulator provides a regulated supply voltage. If 10V instead of 1.8V was stored, then the useful energy would be increased by more than a factor 50. It is clear that even with step-down conversion efficiency loss, which is not yet taken into account, that there are substantial improvements to be achieved by going to higher storage voltages.

This paper is organised as follows. Section II introduces the proposed system architecture. The primary voltage conversion step from the incidental RF waves into a workable DC system supply voltage is discussed in Section III followed by Section IV, which continues with the secondary voltage conversion towards the final storage voltage. Both integration of these building blocks into an operational system and consequent simulation results are presented in Section V. Concluding remarks finish this work in Section VI.

II. SYSTEM ARCHITECTURE

This work targets to increase the energy storage density in wireless powered systems by increasing the voltage to which the storage capacitor C_{bat} is charged, as shown in the proposed system architecture of Fig. 1. Since the stored energy E_{bat} on a capacitor C_{bat} is proportional to square of the storage voltage V_{bat} (Eq. 1), this proves to be a very effective technique. However, not all energy in C_{bat} can be utilized to power a circuit as V_{bat} must remain higher than the nominal voltage V_{nom} , required by the circuit to operate. The usable stored energy E_{usable} is then given by Eq. 2 and Fig. 2 demonstrates this concept.

$$E_{bat} = \frac{C_{bat} V_{bat}^2}{2} \quad (1)$$

Fig. 2. Concept of the system: representation of additionally stored energy (per nF of C_{bat}) as function of V_{bat} for the ideal case of Eq. 2 (dash-dotted line) and other non ideal example cases.

$$E_{usable} = \frac{C_{bat}(V_{bat}^2 - V_{nom}^2)}{2} \quad (2)$$

Fig. 2 plots the ideal usable stored energy, of Eq. 2, per nF of storage capacitance C_{bat} as function of V_{bat} . More realistic results are also provided by the non ideal examples, incorporating the voltage conversion efficiency necessary before this energy can be used by the load. It can be seen in Fig. 2 that the energy budget increases to 15 times its original value if only simple linear regulation for step-down is considered. This factor can still be increased another 3 times with a DC-DC step-down converter at an efficiency of 70%, which is moderate in comparison to the similar voltage conversion ratio of [4].

The proposed architecture of Fig. 1 consists of two main voltage conversion blocks and a control block to ensure proper operation. The primary voltage conversion rectifies and steps up the voltage available at the antenna terminals to a system supply voltage V_{PMU} , which is used as a starting point for the second active step-up voltage conversion. Due to the wireless origin of the incident energy, very low power levels in the order of nA's can be expected and a major challenge in this design will be to minimize the overhead consumption of the PMU. Therefore, the first voltage conversion is implemented as a passive Greinacher multiplier. For the secondary step-up conversion, a Dickson DC-DC converter [5] is selected because of its robustness, low control complexity and resulting low power operation.

The target input frequency range is 5.8GHz to facilitate full integration of the antenna. For impedance matching to be feasible, the capacitive part of in voltage multiplier's input impedance is limited. This means that only a limited amount of multiplication cells can be cascaded, unable to generate the target V_{bat} voltage of 10V. Therefore a two stage voltage conversion approach is used offering the benefit of both relaxing the specification of first conversion stage as well as a higher conversion efficiency in the second converter due to the larger voltage increase per stage.

To cope for input power fluctuations, the system can automatically suspend the operation of the Dickson converter. While V_{PMU} is passively generated and requires no attention, the Dickson converter can be disconnected by the control circuitry when needed. If V_{PMU} has reached upper threshold value V_H , the DC-DC converter is switched in and pumps up

Fig. 3. The AC-DC voltage multiplier.

charge until intermediate buffer capacitor C_{PMU} reaches the lower threshold V_L . As such, the Dickson converter is only active when V_{PMU} is between V_L and V_H . A minimum AC voltage of 53mV is required out of the antenna in order for V_{PMU} to reach V_H and start up the system.

III. PASSIVE AC-DC VOLTAGE MULTICATION

The primary voltage conversion of this design consists of an on-chip antenna, an AC-DC multiplier and a matching circuit. The incident EM waves are converted into a DC voltage V_{PMU} of 1.2V, used as the global supply voltage of the PMU.

A. Antenna

Due to a die size limitation typical in monolithic integrated circuits, the implemented antenna is an electrically small dipole antenna. The open circuit voltage V_{ant} as function of the distance d , dipole antenna length l_{ant} , $\eta_{air} \approx \eta_{vacuum} = 377 \Omega$ and power of the transmitter P_t [2], is given in Eq. 3.

$$V_{ant} = \frac{l_{ant}}{2d} \sqrt{\frac{\eta_{air} P_t}{2\pi}} \quad (3)$$

For an antenna length of 1.8mm and a transmitted equivalent isotropically radiated power of 4W, the voltage V_{ant} is equal to 100mV at a distance of 13.9cm in open air. Integrating the antenna in the top layer of the metal stack reduces this distance by 37 % to 8.8cm due to reflection on the dielectric layers.

B. AC-DC multiplier

The topology of the voltage multiplier is given in Fig. 3. It is built up by a cascade of capacitive coupled rectifier stages, each increasing the voltage. In order to generate a target V_{PMU} in the range of 1.2V from an input voltage of 100mV, the number of cascaded stages and the size of its components need to be optimized. Also an output current $i_{AC-DC,out}$ of 50nA is assumed in the optimization of the AC-DC converter as this is an acceptable power budget to efficiently operate the rest of the system. An evolutionary algorithm is used to optimize this set of design variables, resulting in a V_{PMU} voltage of 1.22V at an $i_{AC-DC,out}$ of 50nA. The transistors are all equally sized with a W/L of 7.2/0.08 μ m. Each capacitor $C_{c,x}$ is equal to 4pF and each $C_{s,x}$ is equal to 300fF. In total 23 stages are cascaded and a power efficiency of 18% is reached.

Fig. 4. A three stage Dickson DC-DC converter with diode-connected transistors M_1 to M_4 and two clock buffers.

C. Matching circuit

A matching circuit is designed to boost the input voltage of the AC-DC multiplier. Because of the highly capacitive antenna impedance and the capacitive input impedance of the multiplier, the matching must be inductive. Due to the low quality factor and large area overhead [2] for inductors at the selected frequency of operation, practical inductance values are limited to 2.6nH in the used CMOS technology. This is too low to make a suitable power matching but voltage matching can still be performed with an integrated inductor of 1.6nH, placed in between the terminals of the antenna. This enables an input voltage again of around 100mV for the voltage multiplier at a powering distance of 8.8cm.

IV. ACTIVE STEP-UP DC-DC VOLTAGE CONVERTER

The second voltage conversion consists of a DC-DC converter and a low power clock generator to step up V_{PMU} to the level of the storage voltage V_{bat} . A Dickson DC-DC converter topology can perform DC-DC step-up with a minimum of necessary control inputs making it the perfect match given the design requirements. This converter can efficiently reach high voltages, only needing a complementary drive. The topology is shown in Fig. 4 for a three stage implementation. M_{1-4} are diode connected transistors and even though this causes threshold voltage V_{th} drops [6] as given by Eq. 4, the benefit of this switches being passive outweighs the otherwise necessary power consumption in level shifting and gate drive.

$$V_{out,N} = (N + 1)V_{in} - (N + 1)V_{th} \quad (4)$$

Control signals p_1 and p_2 are generated by a low power clock generator, implemented by a ring oscillator topology running at a frequency f_{osc} of around 20kHz. Multiple techniques are applied to suppress the power consumption in the ring oscillator. Stacked diode transistors reduce the voltage swing [7] in the 3-stage ring oscillator core as can be seen in Fig. 5. In the subsequent regeneration inverters leakage is lowered through implementing stacked LLHVT devices [8] and a non minimal gate length L decreases the short circuit current [9]. The resulting clock generator consumes 14nA at 1.2V to create a clock signal of 19kHz.

Fig. 4 shows the clock buffers and 3 stages of a Dickson converter. In the implemented design, 9 Dickson stages are necessary to generate a V_{bat} close to 10V. An output impedance minimization approach, as described in [10], is used to achieve the optimal switch $W_{switch,i}$ and flying capacitor C_i converter parameters. The diode connected transistors are sized with a W/L of 0.12/0.18 μm and flying capacitors are each 6.25pF.

Fig. 5. The low power clock generator with regenerated output signals p_1 and p_2 .

When supplying 4nA, an output voltage of 8.3V is generated from a 1.2V input at an efficiency of 75% and 60% respectively considering only the converter core and the converter core together with the clock generator. 10V is achieved when the output is open circuit.

V. SYSTEM INTEGRATION AND SIMULATION

A. System control

A robust design is realized due to the voltage detector [2], [3] control block that automatically turns on the secondary voltage conversion, only when the boundary conditions of correct and efficient operation are met. This is necessary because the Dickson converter, unlike the passive voltage multiplier, depends on the active clock drive to function. Two voltage thresholds $V_H = 1.24\text{V}$ and $V_L = 1.08\text{V}$ are implemented in the voltage detector to control the activity of the Dickson converter. When V_{PMU} reaches the upper threshold value V_H due to the passive voltage multiplier, the Dickson converter will transfer charge from C_{PMU} to C_{bat} . When V_{PMU} has discharged to lower threshold V_L , it is again disconnected in order to allow V_{PMU} to recharge. A robust system is achieved due to the fact the both voltage converters can retain their stored voltages even when they are not driven. This is due to the use of transistor diodes instead of active switches, which can lead to large reverse leakage if driven unproperly.

Fig. 6 shows the control circuit and consists of a voltage reference, a voltage divider and comparator. The reference voltage [11] is composed of 11 stages to generate a 500mV reference. Each transistor operates in weak inversion to reduce the power consumption. As long as $V_{div} < V_{ref}$, the comparator output equals zero. When the input voltage reaches V_H , V_{div} equals V_{ref} . The output voltage of the comparator will then be equal to the input voltage of the detector and the voltage division will be adapted in such a way that, if the detector input drops to V_L , V_{div} is again equal to V_{ref} . The bias currents in the detector are generated by a transistor with a V_{GS} of zero to limit the power consumption further. The control current consumption is limited to 3.8nA. Since V_H determines the activity of the Dickson converter, it also determines the total system startup voltage to be 53mV at the input of the voltage multiplier, translating in a maximum powering distance of 16.7 cm, given an isotropically radiated power of 4W according Eq. 3.

Fig. 6. The voltage detector control block.

Fig. 7. Simulation of the storage system at a powering distance of 8.8cm. If the output of the AC-DC multiplier V_{PMU} is higher than the threshold value V_H , the 19kHz clock generator V_{clock} is activated. If $V_{mult.}$ is lower than the threshold value V_L , the clock is disabled. V_{bat} is the target output storage voltage.

B. System simulation

Fig. 7 shows a simulation of the total system with its most important waveforms. At startup, the Dickson converter's capacitors are uncharged and a higher than 50nA current is drawn. As this can not be delivered continuously by the voltage multiplier, the voltage detector will control the clock generator to operate the DC-DC converter in short intervals, keeping V_{PMU} within V_L and the V_H threshold. A more detailed representation of this is given in zoom boxes of Fig 7. The DC-DC converter's input current is decreased after startup at 180ms and the clock can then operate continuously.

VI. CONCLUSION

A monolithic power management system is presented, enabling an energy storage density improvement of more than an order of magnitude. This is made possible by increasing the storage voltage towards 10V. To demonstrate this concept, a prototype was designed in a 90nm bulk CMOS technology with an integrated 1.8mm dipole antenna using the surrounding energy available in the 5.8GHz ISM band. In a first voltage conversion step, the antenna voltage is passively rectified and multiplied to an intermediate system supply voltage V_{PMU} of 1.2V. Subsequently this voltage is actively stepped up further to

the final storage voltage level V_{bat} of 10V. A low power voltage detector controls the system and ensures correct operation. By means of shifting a part of the total voltage conversion to a second active converter, the specifications on the passive voltage multiplier are kept feasible and a minimum startup voltage of 53mV is necessary for the output to be fully charged. The AC-DC multiplier and the DC-DC converter reach an efficiency of 18 % and 60 % respectively, controlled by a voltage detector circuit consuming 3.8nA and a 19kHz clock generator with a consumption of 14nA. The complete system enables dense energy storage at 10V up to a powering distance of 16.7cm, which is more than twice as large compared to previously reported [3] fully integrated systems at 5.8 GHz.

REFERENCES

- [1] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1287–1302, 2008.
- [2] C. De Roover and M. Steyaert, "Energy Supply and ULP Detection Circuits for an RFID Localization System in 130 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 7, pp. 1273–1285, july 2010.
- [3] S. Radiom, M. Baghaei-Nejad, K. Aghdam, G. Vandenbosch, L.-R. Zheng, and G. Gielen, "Far-Field On-Chip Antennas Monolithically Integrated in a Wireless-Powered 5.8-GHz Downlink/UWB Uplink RFID Tag in 0.18- μ m Standard CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 9, pp. 1746–1758, sept. 2010.
- [4] V. Ng and S. Sanders, "A High-Efficiency Wide-Input-Voltage Range Switched Capacitor Point-of-Load DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4335–4341, 2013.
- [5] J. F. Dickson, "On-Chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, 1976.
- [6] L. Pylarinos, "Charge Pumps: An Overview," Ph.D. dissertation, University of Toronto.
- [7] M. Azarmehr, R. Rashidzadeh, and M. Ahmadi, "Low-power oscillator for passive radio frequency identification transponders," *Circuits, Devices Systems, IET*, vol. 6, no. 2, pp. 79–84, march 2012.
- [8] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, feb 2003.
- [9] A. Morgenshtein, "Short-circuit power reduction by using high-threshold transistors," *Journal of Low Power Electronics and Applications*, vol. 2, no. 1, pp. 69–78, 2012.
- [10] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008.
- [11] E. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference," *Solid-State Circuits, IEEE Journal of*, vol. 14, no. 3, pp. 573–579, june 1979.