Design, implementation and measurement of a 120 GHz 10 Gb/s phase-modulating transmitter in 65 nm LP CMOS

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Abstract A novel mm-wave phase modulating transmit architecture, capable of achieving data rates as high as 10 Gb/s is presented at 120 GHz. The circuit operates at a frequency of 120 GHz. The modulator consists of a differential branchline coupler and a high speed 4-to-1 analog multiplexer with direct digital input. Both a QPSK as well as a 8QAM constellation are supported. To achieve high output power, a 9-stage power amplifier is designed and connected to the multiplexer output. The complete chip is integrated in a 65 nm low power CMOS technology. Capacitive neutralization is used to achieve high gain and good stability for the MOS devices. Also, various differential transmission line topologies are investigated to achieve high performance in terms of loss and area consumption.

Keywords Millimeter-wave · CMOS · RF front end · 65 nm · D-band

1 Introduction

Wireless data communication systems gained tremendously in importance over the last decades. For mass market consumer products, the cell phone and Wireless LAN are the most common examples. Both of these applications are operating in a frequency range from one to several GHz, and accordingly, have transmission bandwidths of several dozens of megahertz. Emerging consumer products like

Wireless HDMI or gigabit Wireless LAN however, require bandwidths in the order of several GHz. Existing standards, which are limited in bandwidth, are not able to achieve these high data rates. Therefore new frequency spectra at which the occupation is low and the available bandwidth is high have to be addressed. The mm-wave spectrum meets these requirements. Already, 60 GHz wireless HDMI and Gigabit WLAN applications, implemented in nanometer scale CMOS processes, were published [1–4], achieving data rates of several Gb/s. Even higher data rates were achieved at a carrier frequency of 120 GHz with the use of high RF performance technologies like InP [5, 6]. Also, the mm-wave spectrum can provide a good solution for short range chip to chip communication links [17]. The trend of an increasing demand for higher data rates is a fact, resulting in a need for wireless data rates in excess of tens of Gb/s in the near future.

If the target application is a mass market consumer product, production cost has to be kept as low as possible. The integration of the millimeter wave front end in a CMOS process creates the opportunity to meet these requirements. Of course, to be able to implement such a system in a CMOS process, the technology performance has to be high enough. Fortunately, the latest nanometer scale CMOS processes have an f_t and f_{max} as high as 200 and 300 GHz respectively [7], leading to mm-wave performance comparable to that of a SiGe process. The result is a high performance mm-wave front end integrated together with digital baseband processing circuits. Also, digital correction and monitoring circuits can be integrated on the same chip, leading to an even higher performance and better control of the RF behavior of the analog front end.

Both of the concepts mentioned above were adopted in the design of a fully integrated mm-wave phase modulating transmitter, introduced in [8]. A new digitally driven

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multiplexer architecture together with the high carrier frequency of 120 GHz has lead to very high performance. The circuit was designed in a 65 nm LP CMOS process with an $f_{\max}$ of approximately 190 GHz. Although the operation frequency is very close to the $f_{\max}$, transmitted data rates as high as 10 Gb/s were achieved with a power consumption of only 200 mW at a 1 V supply.

2 mm-wave CMOS circuit design techniques

2.1 High frequency NMOS behavior

The high frequency behavior of a transistor is best described by the maximum stable power gain (MSG) and maximum maximum achievable power gain (MAG). Figure 1 shows these curves for a typical 65 nm NMOS transistor. The point where the power gain becomes 0 dB is defined as the maximum frequency of oscillation or the maximum frequency at which the transistor can generate power gain ($f_{\max}$). From Fig. 1 it is clear that the finger width and thus the gate resistance has an enormous impact on the $f_{\max}$. For this particular technology an optimal $f_{\max}$ of 190 GHz was achieved with a gate finger width of 1 μm . In [9] the behavior of an NMOS at mm-wave frequencies is described in detail.

Although the gate resistance limits the $f_{\max}$, this is not the true limitation of the power gain. The power gain curve is split up into 2 different parts: the MSG and the MAG part. The MSG curve is the part of the curve at frequencies lower than the break point and expresses the maximum gain that a transistor can achieve without showing unstable behavior. In this region the transistor is conditionally stable which means that with improper load and source impedance the transistor can oscillate. This makes it very hard to design a robust circuit with high gain in this frequency band. The potentially

Fig. 1 Gain curves of a 20 μm 65 nm NMOS transistor

unstable behavior is caused by internal feedback in the transistor through the parasitic gate-drain capacitance. At higher frequencies however, the MAG curve expresses the maximum gain the transistor can achieve. In this frequency band the transistor is unconditionally stable which means that the load and source impedance cannot impede the stability of a single transistor. This is the desired operation region to come to a robust design.

Unfortunately, at 120 GHz the transistor is in the conditionally stable region. To solve this problem several techniques can be adopted to stabilize the transistor. Cascode transistors have proven to be very successful to achieve the unilateralization of a common source transistor [10]. Unfortunately, to achieve the same power gain at these high frequencies as from a common source transistor, the cascode supply voltage has to be increased which leads to an increase in DC power consumption. Another solution is to tune-out the feedback capacitor with an inductor. The disadvantage of this approach is that it only guarantees unconditional stability in a very narrow frequency band, making it more sensitive to process variations. Another approach is to use transformer feedback to neutralize the feedback capacitor. This technique results in an unconditionally stable behavior over a very wide frequency band. The problem is that an additional transformer is needed which will consume more area.

The solution that is proposed in this paper is based on capacitive neutralization by cross coupling additional compensation capacitors in a pseudo differential pair (Fig. 2) [9, 11]. The area overhead is very limited, there is no additional DC power consumption and the unconditionally stable region can be extended over a very wide frequency range. Figure 1 shows the effect on the MSG/MAG curve when this technique is applied to a regular pseudo differential common source stage. The operation frequency of 120 GHz is now located within the unconditionally stable frequency band which is extended to below 10 GHz. An additional advantage of this neutralization technique is the improvement of isolation between input and output. The impact of the load impedance on the input impedance is now only a fraction of what it normally is in a common source transistor. This facilitates design flow in terms of impedance matching severely. Figure 1 also shows that the maximum achievable gain of the neutralized NMOS transistor at 120 GHz will be 6 dB. To accomplish

Fig. 2 Schematic of a pseudo differential pair with capacitive neutralization

this, accurate matching networks have to be added which will be discussed in the next paragraph.

The neutralization capacitors in this work are parallel plate capacitors. Simulations in Agilent Momentum resulted in a very accurate value at 120 GHz. These MOM capacitors have a very high quality factor (180 at 120 GHz) so there is almost no loss associated with the addition of these capacitors. This high quality factor is essential in this design as the available gain at 120 GHz is only 6 dB. In terms of sensitivity to process corner variation a MOS capacitor will normally perform better but the lower quality factor (10 at 120 GHz) will result in gain loss which is detrimental for the circuit performance. Figure 3(a) shows the 3D view of a 7 fF parallel plate capacitor. The Q factor in function of frequency is depicted in Fig. 3(b).

The impact of the process corners on the input and output impedance of the pseudo differential pair at 120 GHz is depicted on a 50 Ω Smith Chart (Fig. 4). The impedance mismatch in the slow or fast corner is very limited so the shift of the tuning frequency will be negligible. Tables 5, 6 and 7 respectively summarize the impact of process corner variation, temperature variation and supply voltage variation on the input and output impedance at 115, 120 and 125 GHz.

Figure 5 shows the impact on the gain of the pseudo differential pair with capacitive neutralization. In the case of the slow corner the stability break point frequency is shifted to 32 GHz. The gate-drain capacitance, causing the potentially unstable behavior, is now smaller compared to the one in the typical case resulting in an overneutralization and therefore leading to a less stable device. In the case of the fast corner the opposite problem occurs. In this case the gate-drain capacitors are larger so that the stability break point shifts to 50 GHz. Fortunately, in both cases, there is still a large gap between the conditionally stable frequency

Fig. 4 Input (a) and output (b) conjugated impedances of the neutralized pseudo differential pair in function of the process corners on a 50 Ω Smith Chart

band and the 120 GHz carrier frequency, so that stable operation is still guaranteed. Of course, at lower frequencies, oscillation still can occur, but this is prevented by the matching networks which are highly frequency selective. Figures 6 and 7 respectively show the impact of the temperature and the supply voltages on the gain of the neutralized pseudo differential pair. The gain variation is quite limited and stability is always guaranteed in the desired frequency band.

2.2 Transmission lines

To achieve an overall gain as close as possible to the maximum gain of the NMOS, impedance matching has to be introduced. Traditionally in GaAs, this is carried out by standard single ended transmission lines. Due to the fact that the transmitter has a fully differential topology, the choice for differential lines was obvious. To optimize the performance of transmission line based matching networks, several transmission line topologies were designed and analyzed. The single ended microstrip line was extended to a differential one (Fig. 8(a)) and was compared to a high

Fig. 3 3D view of a 7 fF MOMCAP (a) and Q factor of the MOMCAP and MOSCAP (b)

Fig. 5 Gain curves of a 20 μm 65 nm NMOS transistor for different process corners

characteristic impedance transmission line (High Z_c TL) (Fig. 8(b)) and a slow wave transmission line (SWTL) (Fig. 8(c)). Table 1 gives an overview of the dimensions of the lines. Only metals at the bottom of the 9-metal metal-stack are used as the purpose of the transmission lines is to make short distance connections. The use of higher metals, which have typically lower attenuation as they are thicker, is not recommended for short distance connections because the relative loss of the vias to go up to these higher metals becomes dominant. Figure 9 shows that bridging a 30 μm distance (separation between 2 stages of the PA which will

be discussed in sect. 3) is more efficient at lower metals so that large via stacks can be omitted. Of course, the same comparison can be made for transmission lines designed in top metal layers. In the context of these short distance connections, the goal is to achieve an impedance transformation ratio as high as possible with low loss and very low area consumption. The comparison between the three different line types was based on their input impedance when loaded with an open and a short, together with the overall loss of the line. The lines were characterized up to 200 GHz. The simulations were performed with Agilent Momentum. [12] has also investigated the behavior of these lines at frequencies up to 67 GHz.

Equations 1 and 2 give an expression for the input impedance when the line is loaded respectively with a short and an open.

$$Z_{in,short} = j \cdot Z_c \cdot \tan(\beta \cdot l) \quad (1)$$

$$Z_{in,open} = -j \cdot Z_c \cdot \cot(\beta \cdot l) \quad (2)$$

If the goal of the line is to achieve a high impedance transformation ratio, than $|Z_{in,short}|$ should be as high as possible, whereas $|Z_{in,open}|$ should be as low as possible. To make a fair comparison between the lines, the length (l) of the lines is fixed at 25 μm . This means that there are only two variables which can change the input impedance of the lines: the characteristic impedance (Z_c) and the phase constant (β). Figures 10 and 11 denote these parameters in function of frequency for the three different lines.

$$Z_c = \sqrt{\frac{L}{C}} \quad (3)$$

Fig. 6 Gain curves of a 20 μm 65 nm NMOS transistor for different temperatures

Fig. 7 Gain curves of a 20 μm 65 nm NMOS transistor for different supply voltages

Fig. 8 Regular differential TL (a), High Z_c TL (b) and SWTL (c)

Table 1 Transmission line dimensions

Parameters	TL 50 Ω	SWTL 50 Ω	High Z_c TL 175 Ω
Signal line metals	Me3,4,5	Me4,5	Me3,4,5
Shield metal	Me2	Me3	–
Signal line width (μm)	3	5	3
Signal line spacing (μm)	22	10	22

Fig. 9 Comparison between lower metal and higher metal connections over a distance of 30 μm

Fig. 10 Z_c in function of frequency

$$v = \frac{1}{\sqrt{L \cdot C}} \quad (4)$$

$$\beta = \frac{2\pi \cdot f}{v} \quad (5)$$

On the one hand, the High Z_c TL has of course the highest Z_c and this is achieved by reducing the capacitance per unit length by removing the shield of the line. Equation 3 gives Z_c in function of the inductance and capacitance per unit length for high frequencies. This explains the increase in Z_c . The SWTL, on the other hand, has the highest β . This is achieved by reducing the wave velocity in the line. Compared to a regular line, the capacitance per unit length is increased by making the signal lines wider, and also, the inductance per unit length is increased by introducing slots in the shield. The result is a Z_c that resembles the one of the regular differential line but the wave velocity (expressed in Eq. 4) is decreased. From Eq. 5 it follows that the phase constant increases.

The simulation results of the input impedances of the three lines are given in Figs. 12 and 13 for an open and a short load respectively. As expected, both the High Z_c TL and the SWTL perform better than the regular line for transformation from a short. At 120 GHz, they behave very similar. For transformation from an open, the result is quite different. The best result is again achieved by the SWTL, but the High Z_c line has in this case the worst performance. To understand this, Eq. 2 has to be investigated more in detail. The goal in this case is to achieve a $|Z_{in,open}|$ as low as possible. As the cotan function from Eq. 2 is decreasing in function of its argument, a higher value is desired to get a low output value. Of course to get an overall low output value of Eq. 2, a low Z_c is also desired. The SWTL has a

Fig. 11 β in function of frequency

Z_c which is lower than that of the High Z_c line and a β which is much higher than the one of the High Z_c line, explaining the result in Fig. 13.

Although the High Z_c TL and SWTL line perform similar for an impedance transformation from a short, there is a slight advantage of choosing the High Z_c TL if the loss of the line is considered. This can be seen on Fig. 12 as the curve of input impedances of the SWTL rotates a bit more towards the center of the Smith Chart. This effect can be seen much more clear in Fig. 14 which shows the attenuation constant of the three lines. It should also be noted that the loss of the regular line is much higher than that of the other two lines. A more detailed analysis of the attenuation parameter is necessary to explain this behavior [13]. In Eq. 6 the different effects contributing to the attenuation are mentioned. α_C is the series resistive loss of the metal signal lines, α_D is the attenuation due to the dielectric loss tangent, α_G is the attenuation due to parallel conductivity and α_R is the radiation attenuation. The latter one can be

neglected in this analysis as the impact of the other contributors is much more pronounced.

$$\alpha = \alpha_C + \alpha_D + \alpha_G + \alpha_R \quad (6)$$

$$\alpha_C = \frac{R'}{2 \cdot Z_0} \quad (7)$$

$$\alpha_D = \tan(\delta) \cdot \frac{\omega \cdot C' \cdot Z_0}{2} \quad (8)$$

$$\alpha_G = \frac{G' \cdot Z_0}{2} \quad (9)$$

$$\alpha = \frac{R'}{2 \cdot Z_0} + \tan(\delta) \cdot \frac{\omega \cdot C' \cdot Z_0}{2} + \frac{G' \cdot Z_0}{2} \quad (10)$$

Equations 7, 8 and 9 give expressions for the different contributors in terms of the RLGC transmission line parameters. In these equations R' is the series resistance per unit length, C' is the parallel capacitance per unit length, G' is the parallel conductance per unit length, $\tan(\delta)$ is the loss tangent of the dielectricum, Z_0 is the characteristic impedance and ω is the angular frequency. Substitution of these expressions in Eq. 6 results in Eq. 10. From this equation it is clear that different parameters can influence the overall attenuation constant. For the High Z_c TL, α_C will be lower compared to a 50 Ω TL as R' of both lines is comparable but Z_0 clearly isn't. The impact on α_D and α_G however is less clear. To understand the effect on the overall attenuation the conductance of the substrate of the unshielded High Z_c TL was swept. Normally, a low conductance is desired in an unshielded transmission line. Figure 15 shows the attenuation in function of the substrate conductivity at 120 GHz. It seems that the attenuation also

Fig. 12 $Z_{in,short}$ in function of frequency on a 50 Ω Smith Chart for the regular TL (a), High Z_c TL (b) and the SWTL (c)

Fig. 13 $Z_{in,open}$ in function of frequency on a 50 Ω Smith Chart for the regular TL (a), High Z_c TL (b) and the SWTL (c)

Fig. 14 α in function of frequency

Fig. 15 α in function of the substrate conductivity

decreases in the case of a very high conductance. In this case the line behaves like a microstrip line with metal ground plane. So to achieve a low attenuation, both a very low parallel conductivity as a very high conductivity ground plane (or substrate) can be used. Of course, technology parameters will limit the performance for both scenarios. The substrate conductivity of this CMOS process is situated around 10 S/m which is still in the low loss region.

As will be discussed further on in the paper, most of the adopted matching networks are parallel shorted stub networks. This means that the transformation from a short should be considered rather than the one from an open. Due to its lower loss and good performance for transforming a short into a higher impedance, the High Z_c TL will be used in the part of the stub that will be loaded with a short. As the impedance transforms towards higher values in function of the distance from the short, there will be a point at 120 GHz for which the High Z_c TL and the SWTL will have the same impedance transformation ratio. From this point on the stub will be implemented by means of a SWTL rather than a High Z_c TL. By combining the two different lines high performance in terms of loss and area is achieved.

3 Transmitter architecture

3.1 Architecture description

The presented 120 GHz phase modulating transmitter front end has a multiplexer based architecture. The core idea is

Fig. 16 Multiplexer based mm-wave architecture

to generate four different phases on chip and select the wanted phase according to the digital input. The result is a phase modulated output signal. The four phases are generated by means of a differential slow wave branchline coupler (BLC). The phase selection is carried out by a high speed analog multiplexer (MUX). A block diagram of the front end is depicted in Fig. 16.

Compared to a more conventional RF architecture (Fig. 17) there are two fundamental changes applied in the presented 120 GHz front end. The first difference is that for the digital to analog conversion, the proposed architecture is not depending on high speed DACs, which are power hungry for the targetted high data rate. The second difference is that the wideband mixers to upconvert the baseband signal can be omitted. The complete functionality of modulation and upconversion is taken over by the hybrid and the multiplexer. This multiplexer based architecture has lead to data rates higher than 10 Gb/s.

A more detailed schematic is shown in Fig. 18. The 120 GHz carrier is brought on chip by means of a GSG probe with a 50 μm pitch. Subsequently, the signal is passed through a buffer and then enters the differential branchline coupler. The two outputs of the coupler are amplified by two 6 stage differential amplifiers to compensate the losses. The output of both amplifiers is then split up so that 4 differential signals with 4 different phases are present at the input of the multiplexer. The 4-to-1 high speed multiplexer (MUX) will select the correct phase according to the digital input. The output of the multiplexer

Fig. 17 Traditional RF architecture

Fig. 18 Schematic of the multiplexer based architecture

is amplified with a 9 stage power amplifier. The modulated 120 GHz output signal is measured with another 50 μm pitch GSG probe at the output.

Depending on which switches are opened and closed in the multiplexer, multiple constellation points can be generated. If the MUX is operated as a regular selector only one of the four phases is connected to the output at the same time. Switching between the 4 phases results in a QPSK output signal. However, when multiple switches are enabled at the same time, a vector sum is realized of the different enabled channels. The result is an 8QAM constellation of which an example is shown in Fig. 40.

3.2 Branchline coupler for phase generation

The presented differential branchline coupler (Fig. 20) has multiple advantages compared to a more traditional single ended design (Fig. 19). First of all, due to the differential nature of the circuit, four instead of two single ended phases are present at the output. In this way, the circuit to generate four differential signals from these outputs can be reduced to two splitters. The second advantage is the ease of implementing a SWTL in a differential topology, reducing the area significantly. The implementation and analysis of these lines is already explained in section II. The SWTL that was used resulted in an on chip wavelength reduction of a factor of 2, leading to an area reduction of a factor of 4. Total area occupied by the phase generation circuit is only 140 μm by 180 μm .

Fig. 19 Single ended branchline coupler

A typical branchline coupler is built out of 2 different transmission lines: one with characteristic impedance Z_c and another one with characteristic impedance $\frac{Z_c}{\sqrt{2}}$. In this implementation, the higher characteristic impedance is chosen to be 50 Ω as higher characteristic impedances are more difficult to achieve because of the high shunt

Fig. 20 Differential slow wave branchline coupler

capacitance of the SWTL. Lower characteristic impedances however can easily be achieved by adding an extra top shield in the SWTL structure. In that way a 35 Ω line was realized. The 3D layout view of the branchline coupler is depicted in Fig. 21.

To properly simulate the device in Agilent Momentum, the structure has to be split up in different parts as the computational load would be too high when simulating the structure as a whole. Figure 22 shows how the structure is divided in four smaller pieces. This is the best way to split up the coupler because of the fact that the electromagnetic field at this point of the transmission lines is the least prone to irregularities caused by surrounding structures like nearby metal of the other transmission lines or vias to connect to the other transmission lines. The simulated performance of the branchline coupler is shown in Fig. 23. An ideal branchline coupler splits the power in 2 equal power levels leading to power levels 3 dB lower than the input power level. Because of the resistive losses in the lines, the output levels of the proposed hybrid are 5 dB lower than the input level (instead of 3 dB) at the desired operation frequency. The bandwidth in which the 2 output levels differ no more than 1 dB is ranging from 111 GHz up to 127 GHz. Compared to other published hybrids this is rather low [14, 15] but it is still more than enough to ensure reliable operation at 120 GHz. The reason for this low bandwidth is the fact that the connection between the 4 SWTL's is not perfectly symmetrical, leading to varying impedances in function of frequency at the interface points. This also results in a variation of the angular difference between the two outputs. The maximum angular error of 13° in the 1 dB band occurs at 111 GHz.

Fig. 21 3D view of the differential slow wave branchline coupler

Fig. 22 Partition of the branchline coupler for finite element simulation in Agilent Momentum

Fig. 23 Simulated performance of the differential SW branchline coupler

3.3 4-to-1 analog multiplexer for modulation and upconversion

As explained in the previous section, the branchline coupler has 2 differential outputs, each 90° out of phase. Due to the differential topology, the inverse signals can easily be created by splitting the outputs and inverting the plus and minus signal lines of the transmission line. In this way 4 differential signals are obtained with relative phases of 0° , 90° , 180° and 270° . Each of these signals is connected to one of the inputs

Fig. 24 Schematic of a single branch of the MUX

of the MUX. Figure 24 shows the schematic of a single branch of the MUX. The incoming 120 GHz signal is first buffered by a pseudo differential pair in which the capacitive neutralization technique explained in section II is adopted. In this way the input impedance of the multiplexer is isolated from the input impedance of the switch, resulting in only a very small change in input impedance when the switch is toggled. The switch is implemented by means of a differential pair of which the tail current source is driven by a digital signal. This results in a different gain for the on and off state of the switch. Figure 25 shows the simulated switch behavior in function of time at a single channel data rate of 4 Gb/s. The ringing of the signal is caused by the limited number of harmonics that are used in the harmonic balance simulation. The small signal parameters are shown in Fig. 26. The isolation between the on and off state is 22 dB which is sufficient for a phase modulated signal in which the amplitude variation is of lower importance. The capacitive neutralization technique is also implemented in the switching differential pair, resulting in an isolation between input and output better than -20 dB, both in the on and off state.

To achieve the maximum gain of both the buffer and the switch, a series impedance matching network is added. Because of the fact that a certain distance has to be bridged between the buffer and the switch a High Z_c line is preferable because of its low loss. Of course, a parallel stub is also needed to connect the DC supply and biasing voltages. The differential stub is loaded with a short. It consists of a combination of a SWTL and a High Z_c line to get the optimal performance as explained in section II. The additional coplanar center line in this stub acts as a DC ground connection. The impact of this center line on the differential transmission line performance is very low as the electrical field is practically zero in the center of this symmetrical transmission line. Table 2 summarizes the impact of the center line on the different transmission line parameters. Figures 45, 46 and 47 give a more detailed overview.

To improve the common mode isolation between the buffer, the switch and other circuits connected to the same bias point, RF chokes are added in the common mode signal path. Figure 28 shows the inductance of these 1.5

Fig. 25 Simulated large signal behavior of a single switch of the MUX

Fig. 26 Simulated s-parameters of a single switch of the MUX

turn inductors with a diameter of $34\ \mu\text{m}$ over frequency. The impact of these RF-chokes is analyzed based on the performance of the 6-stage LO driver amplifier. Figure 27 shows the layout of the amplifier with RF-chokes. Imperfections in the differential load impedances and a common mode return path with low impedance in the amplifier without RF-chokes result in a decrease of the amplifier

Table 2 Transmission line parameter changes resulting from the addition of the center line

Parameter	SWTL $50\ \Omega$ (%)	High Z_c TL $175\ \Omega$ (%)
Z_c	1.5	2.5
β	1.0	0.6
α	12.3	21.1

Chokes

Differential
Stubs
Differential
Pairs

Fig. 27 Layout of the 6-stage LO driver amplifier with RF chokes

Fig. 28 Inductance of the 1.5 turn choke in function of frequency

performance. Figure 29 shows the impact when a 120 GHz differential input signal of $-30\ \text{dBm}$ is applied. An 11 mV common mode signal is generated at the output of the amplifier when the chokes are omitted. The differential voltage swing at the output is about 40 mV. When RF-chokes are added, the common mode output signal is reduced to 3 mV and the differential output voltage is increased to 120 mV. This means that a common mode return path with low impedance not only results in a bad common mode rejection ratio but also degrades the differential gain of the amplifier (Fig. 30).

Fig. 29 Common mode output swing of the 6-stage LO driver amplifier

Fig. 30 Gain loss as a result of a bad common mode rejection ratio

3.4 Power amplifier

The power amplifier is composed out of 2 building blocks: three 20 μm pseudo differential power stages to drive the output and a six stage driver amplifier. The driver amplifier is composed of five 12 μm pseudo differential pairs to provide gain and a scaled 16 μm pseudo differential pair to drive the 20 μm MOSFETs of the power amplifier. Again a common source topology is chosen because of its good efficiency and linearity properties. Also, the neutralization technique is adopted to ensure stable operation over a wide frequency range. Figure 31 shows the schematic of a single power stage.

Of course, in this building block not only gain is of importance, but also the maximization of the output power is essential. Loading the transistor pair with the conjugate impedance leads to the maximization of gain, but there is also an optimal load impedance for maximum output power. Unfortunately, both optimal impedances are not the same [16]. Figure 32 displays this trade-off. The Gp circles are presenting gain values of the same level, the power contours are presenting output power values of the same level. As both optima are not at the same point, a trade off emerges between output power and gain. When the transistors are loaded with the impedance for maximum output power, the gain drops with 1 dB. Because of the fact that the output power is already low due to the relative small size of the devices, this point is chosen in the design of the PA. To get to this optimal load impedance, matching networks are required. To reduce the area overhead, parallel differential matching stubs were chosen. Notice that for each stage, 2 stubs were added to increase the symmetry of the differential PA. Together with the addition of RF chokes in the common mode path, this leads to a vast reduction of the propagation of common mode signals and to an improvement of the common mode stability.

Fig. 31 Schematic of one of the power stages of the PA

The simulated performance of the full 9 stage PA is shown in Fig. 33. The first plot describes the large signal behavior of the PA over a frequency band ranging from 110 GHz up to 130 GHz. Peak gain is about 14 dB at 120 GHz. Peak saturated output power is very close to 0 dBm at 120 GHz. The second plot gives a more detailed description of the large signal behavior at 120 GHz. Because of the many stages needed to get to a reasonable gain, the PAE is rather low. The output power compression curves at 120 GHz are also plotted for different amplifier stages in function of the input power (Fig. 34). Table 3 summarizes the large signal performance of each of these stages. The complete PA is operating from a 1 V supply and draws a current of approximately 66 mA.

The amplified output signal is brought off chip by means of a single ended GSG probe. The power amplifier however, has a differential topology so a differential to single ended conversion is needed. This is achieved by designing the output matching network in such a way that the common mode return path impedance is maximized. [12] has

Fig. 32 Simulated operating power gain circles and load pull contours

Fig. 33 Simulated large signal behavior of the PA operating at 1V supply

Fig. 34 Simulated compression curves for the differential pairs in the 9 stage power amplifier

Table 3 Large signal performance of the differential pairs in the 9 stage power amplifier

Parameter	12 μm	16 μm	20 μm
Gain (dB)	5.21	5.02	4.35
Psat (dBm)	4.55	6.07	7.63
CP1dB (dBm)	-0.12	1.51	2.80

already proven that this technique works at 60 GHz with a GS probe. To investigate this approach more in detail, a model (Fig. 35) was composed to mimic the interaction between the differential transmission line and the GSG probe. L_{in} , C_{pad} and R_{subpad} are respectively the probe pin inductance, the probepad capacitance to the substrate and the substrate resistance between the pads and the common mode point of the differential transmission line. The transmission line is replaced by a lumped model (the series inductance L_{TL} , the mutual parallel capacitance C_{TL} , the parallel capacitance to the substrate C_{TLG} and the substrate

Fig. 35 Lumped model of the probetip, probepads and the GSG probe

Fig. 36 Real part of the impedance balancing error

resistance R_{subTL}). The last part of the structure that needs to be modeled is the interaction between the large probe ground shield and substrate, which is mainly capacitive coupling. This is modeled by means of a capacitor C_{probe} and a substrate resistor $R_{subprobe}$. Based on technology parameters and EM simulations estimations were made for these components. Based on this model, expressions were derived for the G (Eq. A-1) and S (Eq. A-2) input impedances, relative to the common mode point of the transmission line. In the case of a perfectly balanced structure, both impedances should be the same. Figures 36 and 37 respectively show the real and imaginary part of the balancing error in function of the substrate resistance for different probe capacitances. The real part of the error is always smaller than 3Ω . The imaginary part of the error converges to 7Ω for a larger substrate resistance. These errors will of course lead to small impedance mismatch errors at the input and output of the system. However, thanks to the good common mode rejection of the differential input and output amplifiers, these errors are tolerable.

Fig. 37 Imaginary part of the impedance balancing error

4 Measurements

4.1 Measurement setup

To measure the performance of the transmitter, the measurement setup which is depicted in Fig. 38 is used. The 120 GHz carrier is generated by an OML signal source with a 15 GHz LO signal. A 50 μm pitch GSG probe is used to bring the LO signal on chip. The digital signals are generated with a ParBERT and are brought on chip by bondwires. At the output there are 2 possible setups to measure the output signal, depending on whether the waveform or the spectrum of the signal is desired. To measure the waveform, the RF output is probed with the same GSG probe and the signal is downconverted with a wideband mixer to an IF carrier with a carrier frequency between 4 and 7 GHz. This signal is captured with a digital oscilloscope to perform the demodulation or to visualize the waveform. To measure the spectrum, the signal is downconverted with an harmonic mixer and the output is connected to a spectrum analyzer. The next paragraph will give a short explanation of the limitations of

Fig. 38 Measurement setup

this measurement setup and how it can influence the performance of the transmitter.

In a first step, a 7 GHz signal is generated and directly captured with the oscilloscope. The result of this test can be found in Fig. 39 (left). Already some small timing errors are present because of the phase noise on the 10 MHz reference signal. In a next step, the 7 GHz signal is increased to 15 GHz and fed into the OML source module which multiplies the signal to 120 GHz. Unfortunately, the phase noise is also multiplied resulting in a severe loss in SNR of the LO signal. This signal is then directly connected to the downconverting mixer. Of course, part of the extra noise is also generated by this downconverting mixer. Figure 39 (right) shows the signal after up- and down-conversion. It is clear that the measurement setup already generates some phase noise. Together with the bandwidth and gain variation of the downconverter mixer, this will have an impact on the measurement of the front end, limiting the measured performance.

4.2 Transmitter performance

As a result of the errors in the measurement setup, the measured performance of the transmitter will be degraded.

Fig. 39 7 GHz signal generated by the PSG (left) and 7 GHz signal after extracting the eight harmonic from a 15 GHz signal and downconversion with the wideband mixer (right)

Fig. 40 Normalized measured static constellation for a 116 GHz 8QAM signal

Nevertheless clear static and dynamic constellations are captured. The static behavior is captured by enabling the different paths of the multiplexer one by one. The result for an 8QAM signal is shown in Fig. 40. The LO input power is about -5 dBm and the carrier frequency is 116 GHz as the use of this carrier frequency resulted in the best performance in terms of constellation format and output power. The constellation is also measured at LO frequencies ranging from 115 up to 120 GHz. For the lower frequencies the IQ phase error increases whether for higher frequencies the IQ amplitude error increases. For higher frequencies the output power also decreases. The IQ phase error is probably caused by the branchline coupler which is running at a too low frequency resulting in a phase error between its two outputs (Fig. 23). The IQ amplitude error is most likely caused by different path lengths and geometry in the large combiner network of the multiplexer. These errors are static errors and could be solved

Fig. 41 Constellation, spectrum and waveform of the 5 GHz QPSK IF signal at a data rate of 4 Gb/s

Fig. 42 Constellation and spectrum of the 7.5 GHz QPSK IF signal at a data rate of 10 Gb/s (*left*) and of the 6 GHz 8QAM IF signal at a data rate of 6 Gb/s (*right*)

when an IQ correction circuit was added. Unfortunately, this is not implemented in this work.

The dynamic behavior of the front end is captured for different data rates and for different constellations. A 4, 10 and 12 Gb/s QPSK and a 6 and 12 Gb/s 8QAM modulated signal is measured. Figure 41 shows the constellation, waveform and spectrum of the 4 Gb/s modulated 5 GHz IF carrier. An offset corrected EVM of 9.5 % RMS was measured.

To increase the data rate, either the baudrate or the number of bits per symbol can be increased. The result of the first approach is shown in Fig. 42 (left). A data rate of 10 Gb/s is achieved for a QPSK signal. The measured EVM of this signal is 20 % RMS. In the second approach the symbol rate is the same as with the first 4 Gb/s QPSK signal. By increasing the number of bits per symbol, an 8QAM 6 Gb/s constellation is achieved. Figure 42 (right) shows the measured constellation and spectrum. An EVM of 9 % RMS is measured.

To increase the data rate even more, the bit rate is increased for the two constellations to achieve a data rate of 12 Gb/s in both cases (Fig. 43). Unfortunately, because of the previously mentioned measurement setup limitations, proper EVM numbers could not be measured because of the high phase noise.

In Table 4 a comparison is made between different state of the art CMOS mm-wave transmitters, all targeting

wireless data rates of several Gb/s. The presented front end has, with a carrier frequency from 116 GHz up to 120 GHz, the highest operation frequency. Furthermore, the digital baseband circuits are integrated on the same chip. The transmitter has a moderate power consumption of 200 mW at a supply voltage as low as 1 V. The chip photograph can be found in Fig. 44. Total area including bondpads, probepads, ESD protection and decouple capacitors is 1.55 mm².

5 Conclusion

A 120 GHz phase modulating transmitter was implemented in a 65 nm low power CMOS process. The introduction of a new multiplexer architecture allowed data rates as high as 10 Gb/s. Four different phases were generated on chip by means of a differential branchline coupler. A high speed analog multiplexer was used to compose a QPSK or 8QAM constellation. The output of the modulator was amplified by a 9 stage power amplifier.

The high performance of the front end could only be achieved by performing an accurate analysis of the different building blocks and introducing new design

Fig. 43 Constellation and spectrum of the 7.5 GHz QPSK IF signal at a data rate of 12 Gb/s (*left*) and of the 6 GHz 8QAM IF signal at a data rate of 12 Gb/s (*right*)

Table 4 Comparison

Parameters	Ref. [17]	Ref. [18]	Ref. [19]	Ref. [20]	This work
Technology	40 nm LP CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	65 nm LP CMOS
Carrier frequency (GHz)	58	85	77	60	116
Data rate (Gb/s)	>11	–	–implePara>	10	>10
Modulation	ASK	–	–	QPSK	BPSK/QPSK/8QAM
Direct digital input	no	no	–	yes	yes
VCO on chip	yes	no	yes	yes	no
Area (mm ²)	0.06	1.2	2.88 ^a	6.88 ^a	1.55
Power consumption (mW)	29	120	390	170	200
Supply voltage (V)	1.1	1.2	–	1.2	1

^a Area of complete transceivers (both transmitter and receiver are included)

techniques to boost their performance. For the transistors, capacitive neutralization was adopted to achieve high gain and very good stability properties over a large bandwidth. In the design of the matching networks and the branchline coupler the use of differential High Z_c transmission lines and differential Slow Wave transmission lines has lead to a reduction in area and power loss.

The measurement results demonstrate the use of CMOS for wireless mm-wave communication links at multi Gb/s data rates. This proves that the implementation of a fully integrated high performance single chip mm-wave communication module in CMOS is possible, enabling the development of new high performance wireless applications like wireless HDMI and Gb/s WLAN.

Fig. 44 Chip photograph

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Appendix

Tables 5, 6 and 7 respectively give an overview of the impact of process corners, temperature and supply variations on the input and output impedance of a neutralized pseudo differential pair.

Impact of adding a center line in a differential transmission line on Z_c , β and α are respectively depicted in Figs. 45, 46 and 47.

Equations that describe the G and S input impedance of the GSG probepad with balanced load.

Table 5 Impact of process variation on input and output impedance of the neutralized pseudo differential pair

	Slow	Typical	Fast
$Z_{in}(115\text{GHz}) [\Omega]$	16.81–95.11j	17.02–92.62j	16.32–89.21j
$Z_{out}(115\text{GHz}) [\Omega]$	31.57–102.82j	31.20–98.79j	28.06–93.29j
$Z_{in}(120\text{GHz}) [\Omega]$	16.79–91.16j	17.03–88.83j	16.48–85.63j
$Z_{out}(120\text{GHz}) [\Omega]$	30.11–99.21j	29.89–95.56j	27.27–90.49j
$Z_{in}(125\text{GHz}) [\Omega]$	16.77–87.78j	17.03–85.58j	16.59–82.57j
$Z_{out}(125\text{Hz}) [\Omega]$	28.85–96.07j	28.75–92.74j	26.52–88.04j

Table 6 Impact of temperature variation on input and output impedance of the neutralized pseudo differential pair

	–20 °C	27 °C	80 °C
$Z_{in}(115\text{GHz}) [\Omega]$	17.68–93.86j	17.02–92.62j	17.36–94.05j
$Z_{out}(115\text{GHz}) [\Omega]$	33.09–102.46j	31.20–98.79j	31.89–103.61j
$Z_{in}(120\text{GHz}) [\Omega]$	17.64–90.00j	17.03–88.83j	17.31–90.18j
$Z_{out}(120\text{GHz}) [\Omega]$	31.56–99.00j	29.89–95.56j	30.34–100.04j
$Z_{in}(125\text{GHz}) [\Omega]$	17.60–86.69j	17.03–85.58j	17.26–86.86j
$Z_{out}(125\text{Hz}) [\Omega]$	30.23–95.99j	28.75–92.74j	29.01–96.94j

Table 7 Impact of supply voltage variation on input and output impedance of the neutralized pseudo differential pair

	1,000 mV	1,200 mV	1,400 mV
$Z_{in}(115\text{GHz}) [\Omega]$	17.66–94.47j	17.02–92.62j	17.35–92.78j
$Z_{out}(115\text{GHz}) [\Omega]$	30.70–104.66j	31.20–98.79j	33.78–100.54j
$Z_{in}(120\text{GHz}) [\Omega]$	17.61–90.58j	17.03–88.83j	17.32–88.97j
$Z_{out}(120\text{GHz}) [\Omega]$	29.25–101.00j	29.89–95.56j	32.21–97.25j
$Z_{in}(125\text{GHz}) [\Omega]$	17.55–87.25j	17.03–85.58j	17.28–85.71j
$Z_{out}(125\text{Hz}) [\Omega]$	28.01–97.83j	28.75–92.74j	30.85–94.38j

Fig. 45 Impact of the center line on Z_c

$$Z_G = \left(s \cdot \frac{L_{in}}{2} + \frac{1}{\frac{R_{subpad}}{2} + \frac{1}{s \cdot C_{pad}} + \frac{1}{R_{subTL} + \frac{1}{s \cdot C_{TLG}}} + 2 \cdot s \cdot C_{TL} + \frac{1}{s \cdot L_{TL} + \frac{1}{2 \cdot s \cdot C_{TL}}}} \right) // \left(R_{subprobe} + \frac{1}{s \cdot C_{probe}} \right) \quad (A-1)$$

$$Z_S = s \cdot L_{in} + \frac{1}{\frac{1}{R_{subpad} + \frac{1}{s \cdot C_{pad}}} + \frac{1}{R_{subTL} + \frac{1}{s \cdot C_{TLG}}} + 2 \cdot s \cdot C_{TL} + \frac{1}{s \cdot L_{TL} + \frac{1}{2 \cdot s \cdot C_{TL}}}} \quad (A-2)$$

 Fig. 46 Impact of the center line on β

 Fig. 47 Impact of the center line on α

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