Offset Measurement Method for Accurate Characterization of BTI-induced Degradation in Opamps

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Abstract—Bias temperature instability (BTI) has become one of the major concerns in reliable circuit design in advanced CMOS nanometer technology. It can have a significant impact on the performance of analog building blocks. To understand the effect of BTI in analog circuits, an accurate measurement of circuit parameter degradation by BTI has become very necessary. This paper proposes a measurement scheme of the input offset degradation of an operational transconductance amplifier (OTA) due to the BTI effect. Conventional offset measurement techniques do not take into account the BTI recovery. Therefore, the proposed scheme is targeted to measure degradation during the stressing to avoid relaxation. The concept behind the scheme is to present the offset degradation as a function of the propagation delay degradation. Simulation results are shown for the measurement circuit.

Keywords—component: Bias Temperature Instability, OTA, Input offset degradation, Measurement technique.

I. INTRODUCTION

Technology scaling accelerates transistor degradation, especially due to the bias temperature instability (BTI). Degradation effects can no longer be solved at the technology level and risk to become a show-stopper for the development of novel electronic systems. Hence, it has become a serious issue that circuit designers need to take into account [1] [2]. In recent years, the focus of research is inclined to two aspects: (a) modeling and monitoring the BTI degradation and (b) design for reliability. In both domains, degradation measurements play a significant role. That can be done both at device level as well as at circuit level. So, all proposed measurement schemes classify the degradation in two ways i.e. transistor parameter degradation [3] and circuit parameter degradation [4]. A few BTI measurement techniques have been proposed in recent years [3-8]. Most of them require highly specialized equipment and very precise control during measurement, especially for the device-level measurements. At circuit level, the emphasis is mainly on monitoring digital circuits and digital building blocks, which have been shown to be very susceptible to BTI degradations [4-8]. However, no significant work addresses analog circuit performance degradation monitoring. An operational transconductance amplifier (OTA) is a very important analog building block in integrated circuit design. It has been understood

that the offset voltage of an OTA has a significant aging effect due to BTI degradation [9]. Recovery after BTI stress in MOSFETs has been a well addressed phenomenon of BTI degradation in the past decade. It is also understood how this recovery affects the reliability assessments [12]. Both overestimation and underestimation can occur due to BTI recovery. Very short recovery time constants [13, 14] make it hard to measure the BTI effect after stress without any recovery. Conventional offset measurement techniques are not very efficient to measure offset degradation as in most of the conventional techniques stress conditions need to be replaced by measurement conditions, which will introduce recovery. As such, we can not get an accurate measurement of BTI-induced offset degradation of an OTA. This paper proposes a measurement scheme of the input offset degradation which can efficiently avoid recovery to get more accurate measurement.

In this paper, section II briefly overviews the BTI degradation. Section III discusses why most conventional techniques are not suitable and an efficient offset degradation measurement concept, scheme and implementation of proposed circuit are presented. Simulation results are presented in section IV. Finally, section V concludes the paper.

II. BIAS TEMPERATURE INSTABILITY (BTI)

For sub-32nm CMOS process, BTI degradation has become the most dominant factor having an increasingly adverse impact on the analog circuit performance [9]. When subject to operating bias and temperature, transistors exhibit changes in their characteristics over time; this effect is termed as bias temperature instability (BTI). BTI is typically observed as a threshold voltage shift. In recent time, extensive efforts have been placed to understand and model the BTI. It has been found that during the AC stress BTI damage has a permanent (P) as well as a recovery component (R) [9][10]:

$$\Delta V_{TH} \sim \underbrace{\exp(\alpha_1 V_{GS}) t^{n_p}}_P + \underbrace{V_{GS}^{\alpha_2} (C_R + n_R \log_{10}(t))}_R \quad (1)$$

Here, α_1 and α_2 are voltage scaling factors. n_p and n_R are time components. All these components along with C_R are process dependent. This recovery component (R) characterizes the so called relaxation or recovery of BTI degradation immediately

after the stress voltage has been reduced [12-14]. This recovery behavior complicates the measurement of the BTI degradation. It can introduce overestimation or underestimation.

III. OFFSET DEGRADATION MEASUREMENT

This section discusses why conventional offset measurement techniques are not applicable to measure BTI-induced offset degradation of the OTA. It also includes the concept of the input offset degradation measurement of a symmetric OTA by using asymmetric stress and output transition time shift. Based on this concept, a measurement scheme is proposed here.

A. Conventional Offset Measurement Techniques

Fig.1(a) and Fig.1(b) depict conventional measurement techniques, that are mostly used to measure the input offset voltage of an OTA. In technique1 (Fig.1(a)) the offset voltage is quantified as the DC value of the non inverting input voltage (in SRC1), when the output of the OTA becomes zero. In technique2 (Fig.1(b)) the inverting input voltage (in SRC2) needs to be fixed as $V_{DD}/2$ and the non-inverting input voltage is ramped upward from V_{SS} to V_{DD} . When the output voltage changes from V_{SS} to V_{DD} , the differential input voltage ($V_{in}=|SRC2-SRC1|$) is measured as the input offset voltage [11].

Figure 1. (a) Conventional offset measurement technique1. (b) Conventional offset measurement technique2.

It is known that asymmetrical stress can introduce significant time-dependent mismatch in a circuit such as a symmetric OTA (comparator). Asymmetric stress can be realized as an AC signal applied to one of the input nodes and a fixed DC voltage to the other input node of an OTA. Due to the asymmetric stress at the inputs of an OTA, the V_{TH} of its input transistors will be degraded unequally. This will introduce the significant time-dependent mismatch in threshold voltage and its input offset increases over time (see Fig.2) [9].

The above measurement methods are not suitable to the measure offset degradation due to BTI under asymmetric stress. For offset voltage degradation measurement, these methods can not avoid the relaxation because during the measurement the asymmetric stress needs to be replaced by a DC voltage on both the inputs. That means these techniques can not hold the gate voltage constant (asymmetric) during both the stress and the measurement period to avoid recovery. Therefore, a scheme that

implies a definite technique to avoid recovery of the BTI effect is required.

Figure 2. The offset of an OTA, subjected to asymmetrical stress, is increasing over time.

B. Proposed Measurement Concept

The offset voltage of an OTA can be classified as systematic offset and random offset. As systematic offset mainly occurs due to the non-idealities of a circuit (or layout), it can be solved by good design. On the other hand random offset occurs due to mismatches in matched devices. During the life cycle of the device this mismatch can change due to BTI. BTI is typically observed as a threshold voltage shift, which can introduce significant V_{TH} mismatch between the input transistors of the OTA, especially with asymmetric stress.

Since the offset voltage (V_{OS}) is related to the differential input, it follows that:

$$V_{OS} = \Delta V_{G,P1} - \Delta V_{G,P2} = \Delta V_G \approx \Delta V_{GS} = \frac{\Delta I}{g_m} \quad (2)$$

where ΔI is the difference in current at the branches of the input transistors P1 and P2 of the OTA (see Fig.3(a)) due to V_{TH} variation, and g_m is the transconductance of the MOSFET devices. According to (2), it is necessary to find ΔI and g_m in order to get the offset voltage.

Let us say, initial threshold voltage of transistors P1 and P2 is V_{TH} . Then, after asymmetric stress due to the BTI effect the device mismatches are incorporated to the corresponding threshold voltage of P1 and P2 as:

$$V_{TH,P1} = V_{TH} + \Delta V_{TH} \quad (3)$$

$$V_{TH,P2} = V_{TH} \quad (4)$$

Drain current will be,

$$I_{P1} = \frac{\beta}{2} (V_{GS,P1} - (V_{TH} + \Delta V_{TH}))^2 \quad (5)$$

$$I_{P2} = \frac{\beta}{2} (V_{GS,P2} - V_{TH})^2 \quad (6)$$

where $V_{GS,P1}$ and $V_{GS,P2}$ are the gate to source voltages of transistor P1 and P2. For a symmetric OTA (Fig.3(a)) $V_{GS,P1}=V_{GS,P2}=V_{GS}$. For simplicity, it is assumed that $V_{GS} \gg \Delta V_{TH}$. Then we can write:

$$I_{P1} \approx \frac{\beta}{2} (V_{GS,P1} - V_{TH})^2 (1 - \frac{2\Delta V_{TH}}{(V_{GS,P1} - V_{TH})}) = \frac{I_{P3}}{2} - \frac{I_{P3}}{2} \times \frac{2\Delta V_{TH}}{(V_{GS} - V_{TH})} \quad (7)$$

$$I_{P2} \approx \frac{\beta}{2} (V_{GS,P2} - V_{TH})^2 = \frac{I_{P3}}{2} \quad (8)$$

In Fig.3(a) I_{P3} , I_{P1} , I_{P2} are the current through transistors P3, P1, P2 respectively where, $I_{P3}=2I_{P1}=2I_{P2}$

Due to the V_{TH} variation, the difference in current through transistor P1 and P2 is:

$$\Delta I = I_{P2} - I_{P1} \quad (9)$$

From (7), (8) and (9) we can get:

$$\Delta I = I_{P3} \times \frac{\Delta V_{TH}}{(V_{GS} - V_{TH})} \quad (10)$$

The transconductance of transistors P1 and P2 is:

$$g_m = \frac{I_{P3}}{(V_{GS} - V_{TH})}, \text{ as } I_{P3}=2I_{P1}=2I_{P2} \quad (11)$$

Then from (2), (10), (11) we can find:

$$V_{OS} = \frac{\Delta I}{g_m} = \Delta V_{TH} \quad (12)$$

Equation (12) shows analytically that the random offset voltage degradation due to aging can be defined as the threshold voltage deviation of the input transistors (P1 and P2 in Fig.3(a)).

The propagation delay (t_p) of an OTA is related to the slew rate (SR). It follows that,

$$t_p = \Delta t = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2SR} \quad (13)$$

where V_{OH} is the logic high voltage and V_{OL} is the logic low voltage.

$$\text{The Slew Rate, } SR = \frac{I_{P3}}{C_L}, \quad (14)$$

where C_L is the load capacitance .

Then from Eq. (13) and (14),

$$t_p = \frac{(V_{OH} - V_{OL})C_L}{2I_{P3}} = \frac{(V_{OH} - V_{OL})C_L}{4I_{P1}} = \frac{(V_{OH} - V_{OL})C_L}{4\frac{\beta}{2}(V_{GS} - V_{TH})^2} \quad (15)$$

where V_{TH} is the threshold voltage of transistor P1/P2..

Therefore from (15) and (12) the normalized propagation delay deviation ($\Delta t_p/t_p$) is :

$$\frac{\Delta t_p}{t_p} = \frac{2\Delta V_{TH}}{(V_{GS} - V_{TH})} = \frac{2V_{OS}}{(V_{GS} - V_{TH})} \quad (16)$$

$$\text{OR: } V_{OS} = \frac{(V_{GS} - V_{TH})}{2t_p} \times \Delta t_p \quad (17)$$

So, this proves that the offset voltage degradation of the comparator has a linear relation with the propagation delay degradation. Using this linear relation we can measure the offset degradation as a function of the propagation delay degradation. This relation allows us to develop a differential measurement

scheme for the offset degradation, which can efficiently avoid BTI recovery to get an accurate measurement. Now, if we apply a triangular or pulse wave to one of the input nodes and a fixed DC voltage to the other input node, then an asymmetrical stress is applied to the input pair of the OTA. As a result, the matched input transistors of the OTA potentially suffer from time-dependent mismatch and will introduce input offset degradation. As a result, the output of the OTA will shift in the time scale (see Fig.3(b)). Therefore, the output transition is shifted by Δt_p , which is known as propagation delay degradation of the OTA. According to the above analytical expression, this ' Δt_p ' is the depiction of the offset degradation and hence of the aging (17).

Figure 3. (a) Symmetric OTA under test. (b) Simulated timing diagram of the measurement circuit.

According to the above concept and the mathematical expression we need to measure the propagation delay degradation to realize and measure the offset voltage degradation of the comparator (symmetric OTA) and the aging of the input transistors. In the next subsection we explain in detail an efficient measurement scheme which is based on the concept discussed above.

C. Proposed Measurement Scheme

One of the focuses of this measurement scheme is to avoid the recovery. To avoid recovery, one effective way is to do the measurement during the stress period. In other words the devices should be in stress during the measurement period. A differential measurement structure, using two identical symmetric OTA, has been used here. This differential measurement scheme is also designed to avoid all common-mode variations, as these can influence the measurement. During the stress period, one OTA (STRESS OTA) is stressed by applying a high supply voltage and an asymmetric stress voltage signal to its inputs. The another OTA (FRESH OTA) is in the off state by cutting off the

supply voltage rail. Hence, the STRESS OTA will experience an accelerated degradation but not the FRESH OTA (Fig. 4). During the measurement period the STRESS OTA remains in the stress condition and only the FRESH OTA starts to work with the nominal supply voltage and the asymmetric input. As the STRESS OTA is still in the stress condition we can effectively avoid the recovery during measurement by using this test condition.

Figure 4. Aging-induced offset degradation measurement scheme

A basic block diagram of the proposed measurement scheme is shown in Fig.4. It also includes two voltage comparators. These two comparators will work at nominal supply voltage which will not introduce any degradation. The comparator pair (i.e. comp1 and comp2) compare the output (Vout1 and Vout2) of the two OTAs with Vref1 and Vref2, where Vref1 and Vref2 are set as 50% of nominal supply voltage. The output of comp1 goes high when Vout1 crosses Vref1, as depicted in Fig.3(b). Similarly the output of comp2 goes high when Vout2 exceeds Vref2. These two comparator output signals Comp1_out and Comp2_out can directly be fed to the multichannel oscilloscope. For the rise transition of the output of both OTAs, Comp1_out should go high earlier than Comp2_out (Fig.3(b)). Comp2_out is delayed because of the BTI effect. That delay can be measured easily by the oscilloscope. This measured delay is the direct representation of the offset degradation of the STRESS OTA. The above discussed scheme can fully be implemented on-chip using on-chip comparators.

IV. SIMULATION RESULTS

Figure 5. The offset as well as the propagation delay degradation of an OTA changes linearly with respect to the Vth shift

The measurement circuit has been designed and implemented in 28nm technology.. In Fig.3(b), the simulated output of the two

OTAs and the two off-chip comparators has been depicted. It is clearly shown how the propagation time is shifted by Δt_p . As the offset voltage degradation due to the BTI effect has a linear relation with the Vth shift (12), we have used a varying voltage source at one of the inputs of the STRESS OTA to realize and simulate the Vth shift as well as the offset voltage degradation. Fig.5 shows that the propagation delay degradation has a linear relationship with the Vth shift and that the offset of an OTA varies linearly with the Vth shift.

V. CONCLUSION

In this paper a new aging-induced offset degradation measurement scheme has been proposed. The proposed scheme is validated by circuit simulations. This scheme is efficient to avoid relaxation to measure more accurately the impact of BTI degradation on analog circuits. The circuit concept can also be used to measure the effect of BTI degradation on other analog parameters. This work will help to find good BTI mitigation techniques.

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