18.3 Bidirectional Communication in an HF Hybrid Organic/Solution-Processed Metal-Oxide RFID Tag

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The ambition of printing item-level RFID tags is one of the driving forces behind printed electronics research. Organic RFID tags have been shown, initially using p-type organic semiconductors [1–4]. The introduction of n-type organic semiconductors with reasonable performance made organic CMOS conceivable [5] and organic CMOS RFID tags were shown [6]. However, all currently reported organic RFID tags are based on a tag-talks-first principle: as soon as the tag gets powered from the RF field, its code is transmitted at a data rate determined by an internal ring oscillator. Practical RFID systems will need to be able to read multiple RFID tags within the reach of the reader antenna. Existing anti-collision protocols implemented in organic RFID tags [2,4] are limited to about maximum 4 tags and come at the cost of a slow reading time. In this paper, we for the first time realize a reader-talks-first low-temperature thin-film transistor (TFT) RFID circuit. We use a complementary hybrid organic/oxide technology. As organic transistors with reasonable channel lengths ($\geq 2\mu\text{m}$) have a cut-off frequency below 13.56MHz, the base carrier frequency of HF communication, present technologies on foil do not yet allow to extract the circuit clock as a fraction of the base carrier. We solve this by introducing an original uplink (reader-to-tag) scheme, in which a slow clock (compatible with our transistors' speed) is transmitted as amplitude-modulation on the base carrier while data is encoded on this clock by pulse width modulation (PWM).

In TFT technology, the p-type and n-type transistors require different semiconductors. Stable p-type organic semiconductors with charge carrier mobility up to $3\text{cm}^2/\text{Vs}$ now exist, but their n-type counterparts are still quite immature. Meanwhile, solution-processable n-type oxide semiconductors are emerging. The hybrid organic/oxide technology used in this work combines a 250°C solution-processed n-type metal-oxide TFT with typical charge carrier mobility of $2\text{cm}^2/\text{Vs}$ with an evaporated pentacene p-type TFT with mobility of up to $1\text{cm}^2/\text{Vs}$. We use a high-k Al_2O_3 dielectric, which increases the transistors' current drive. Output characteristics of both devices are shown in Fig. 18.3.1a. Fig. 18.3.1b shows the typical inverter characteristics for different supply voltages and the process cross-section is shown in Fig. 18.3.1c. Further process details on the hybrid integration of both devices can be found in [7].

Low-cost tags will need to be passive, i.e., draw the power for the circuit from the RF field by means of a rectifier operating at HF (13.56MHz). We designed double half-wave transistor rectifiers [8] using solution-processed metal-oxide TFTs. These rectifiers operated up to frequencies beyond 100MHz, owing to both the high mobility ($\mu > 2\text{cm}^2/\text{Vs}$) and the low zero- V_{GS} current of the oxide TFTs (see Fig. 18.3.2). Two different double half-wave transistor rectifiers are used in our tag design (see Fig. 18.3.3). A slower rectifier provides the DC power voltage to the tag. The faster rectifier is designed with a time constant faster than the amplitude-modulated clock sent in the uplink, and thus allows detecting this uplink data clock as explained further.

Typical logic gates in the digital building blocks combine pentacene transistors ($W/L=280\mu\text{m}/5\mu\text{m}$) with oxide transistors ($W/L=140\mu\text{m}/5\mu\text{m}$), with a 2:1 ratio (p:n). Transistors are proportionally scaled when higher drive current is needed. The delay gate (ΔT in Fig. 18.3.3b) comprises a dedicated pentacene transistor ($W/L=40\mu\text{m}/10\mu\text{m}$) and oxide transistor ($W/L=50\mu\text{m}/50\mu\text{m}$).

In order to obtain bi-directional data communication with the above-explained uplink protocol, a dedicated reader has been developed that allows amplitude modulation for the up-link data transfer using pulse width modulation, i.e. having a different duty cycle for logical 0 (75% active low) and 1 (25% active low) in the different code sequences.

The overall schematic of the tag is shown in Fig. 18.3.3a. The tag comprises a resonant antenna at 13.56 MHz, two different rectifiers, a 4-bit input decoder cir-

cuit, an 8-bit code sequencer (similar to [3,4]) and a load modulator. The code sequencer generates 8 data bits, followed by a sequence of 8 ones. Figure 18.3.3b presents the data extractor schematic for the input decoder, which extracts both the data and the clock from the rectified RF signal. After 3 inverter stages for restoring the input signal to the logic levels, a dedicated delay gate is used (ΔT in Fig. 18.3.3b). The logic one (25% active high on after 3 inverter stages) will discharge the 106pF capacitor less as compared to the logic zero (75% active high on after 3 inverter stages) and hence a different signal is stored in the D-Flip-Flop at the next falling edge of the incoming signal. Two different 4-bit input decoders (code A=0010, code B=0110) and two different 8-bit code sequencers (code 1= 01010011, code 2=010111001) have been designed and tested. Figure 18.3.4 shows that different input decoders can detect their corresponding codes from an input stream comprising different codes.

We screened all reader data rates at which the correct hit was decoded and no false positives were found when other codes were applied. We also scanned the generated output sequence data rate. Both data rates are scanned for supply voltages from 3.75V to 10V (see Fig. 18.3.5). It was empirically determined that 420bit/s is an appropriate reader modulation frequency when low internal voltages are obtained in the tag, and 1200 bits/s when higher power voltages are obtained in the tag. At 420bit/s, two independent tags can be read in 100ms, and even 5 independent tags can be read without collision at 1200bits/s. A reader operating at 13.56MHz, and alternating its modulation data rate between 420bits/s and 1200bits/s can screen all internal power voltages at which the tag can operate, up to 10V.

Figure 18.3.6 shows the internal RFID tag voltages during system testing using a set-up as indicated in Fig. 18.3.3.a. An input decoder for detecting the uplink code A and an output sequencer for generating code 2 are used during this test. The external RFID reader can toggle the code generator on (b) and off (c). One observes that the internal power voltage of the tag (slow rectifier) substantially drops during amplitude modulation at the reader, but the use of hybrid CMOS still ensures the correct operation at these low power voltages.

Figure 18.3.7 shows the die micrographs of two input decoders ($3579\times 4228\mu\text{m}^2$) and two code generators ($5983\times 6064\mu\text{m}^2$). In addition, we used antennas, resonant capacitor foils and rectifiers corresponding to what has been reported in [3,4], although different processes have been used. The overall bi-directional tag comprises 368 metal oxide transistors and 365 pentacene transistors closely integrated on the same substrate.

In conclusion, we have demonstrated a viable route towards bi-directional communication at 13.56MHz by low-cost RFID tags in a complementary, hybrid solution-processed metal-oxide/organic thin-film transistor technology. As these transistors do not allow a clock to be decoded directly from the HF base carrier, the up-link clock is transmitted as amplitude modulation of the carrier, and uplink data by pulse width modulation of this clock. Our solution will enable true anti-collision protocols for low-cost HF RFID tags.

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Figure 18.3.1: (a) output characteristics of typical solution-processed oxide and evaporated pentacene transistors, (b) inverter characteristics of the hybrid technology at different power voltages. The inset shows a photograph of an inverter. (c) Cross-section of the hybrid technology process.

Figure 18.3.2: Rectified voltage of double half-wave rectifiers as a function of frequency at a 5V AC amplitude. The rectifiers comprise 2 capacitors and 2 solution-processed oxide transistors. The inset shows the current voltage characteristics of the oxide transistor-diode.

Figure 18.3.3: (a) schematic overview of the different building blocks of the hybrid RFID tag, (b) detailed schematics of the uplink data extractor and shift register.

Figure 18.3.5: (left) Uplink shmoo plot of the reader data rate range versus the tag internal supply voltage for the input decoders A and B. (right) The corresponding code sequencer data rate (downlink) for different supply voltages.

Figure 18.3.4: (top) toggling of the hit signals from both decoders (A and B) as a consequence of an input stream comprising multiple codes; (bottom) output of code sequencer 1 operated at 5V as a consequence of a hit signal at the input.

Figure 18.3.6: (a) Measurements of the internal voltages of the bi-directional hybrid RFID tag when powered by the 13.56 MHz signal of the reader. (b-c) show a zoom of the hit and the kill transients.

Figure 18.3.7: (top) Die photographs of the input decoders A (left) and B (right); (bottom) Die photographs of the code sequencers 1 (left) and 2 (right).