Abstract—A fully integrated Dual-Output capacitive DC-DC converter providing a total output power of 1 mW is presented. The converter realizes both a 2/3 and a 1/3 voltage conversion, from 1.2 V to respectively 0.755 V and 0.32 V. A hysteretic controller regulates both output voltages, independently of the power distribution between both outputs. It achieves an efficiency of 68.6% for the nominal case, and a maximum efficiency of 75.3%. The validity of the developed model and used design strategy were verified by a test chip implemented in a 90 nm bulk CMOS technology.

I. INTRODUCTION

The need for low-power integrated systems has pushed designers towards the use of multiple supply voltages, especially in System on Chip (SoC) applications [1]. Both dynamic and static power consumption can be reduced by lowering the supply voltage. Especially leakage power is becoming a major problem in today’s sub-micron technologies. Due to the limited amount of scavenged energy in wireless sensor node applications, the power consumption of such integrated systems has reached very low levels (< 1 µW [2]). Low-power design is therefore becoming a necessity.

The need for multiple supply voltages requires efficient (preferably on-chip) DC-DC conversion. Unfortunately the no on-chip high quality inductors are available [3], which impedes the integration of classic inductive buck/boost converter topologies. On-chip capacitors on the other hand are easier to model and tend to have reasonably good characteristics, that even seem to improve in newer technologies. Therefore the use of capacitive converter topologies in high efficiency integrated DC-DC converters has gained momentum [4].

An additional advantage, in both area and regulator overhead, arises from using a single converter to generate multiple voltages. Only inductive solutions (so called ‘Single-Inductor Multiple-Output’ (SIMO)) have been explored, mostly using external inductors. In this paper an integrated capacitive DC-DC down-converter with 2 outputs and a total power supply capacity of 1 mW is presented. A Hysteretic Controller is used to maintain a constant output voltage, independent of load variations and power distribution.

Due to the multiple-output nature the selection of the converter topology needs special attention. Chip area is mainly determined by the amount of integrated capacitance. The use of additional capacitors has to be avoided. If feasible the additional switches, required by the added outputs, should take part in the regular operation of the converter. Each additional switch results in increased resistive and switching losses. The resistive losses can be alleviated by increasing the size of the transistor used as switch, resulting in increased switching losses. The extra transistors ideally have negligible resistance, and would therefore be very large. This reduces the area available for on-chip capacitors, complicating full integration.

The paper starts by describing the selected topology, including the working principles and modeling of the converter. Next the working principles of the hysteretic regulator are described. It has to guarantee correct converter operation at all times. The correct operation of the system and validity of the developed model were verified by a test chip in a 90 nm CMOS technology. The final section summarizes the measurement results of the fabricated DC-DC converter.

II. MULTIPLE-OUTPUT CONVERTER TOPOLOGY

The converter topology has to be suitable for continuous power distribution to both outputs. The followed design methodology, adapted to deal with multiple outputs, is presented.

A. Topology

The converter uses a modified Ladder topology (Fig. 1). Both a 2/3 \( V_{in} (V_{out1}) \) and a 1/3 \( V_{in} (V_{out2}) \) conversion are available. The fixed capacitor of a classic Ladder topology is split into two different capacitors, \( C2_1 \) & \( C2_2 \). These capacitors are both constantly connected to one of both outputs. The other 2 capacitors, \( C1_1 \) & \( C3 \), are jointly used by both outputs.

This topology has a serious area benefit when 2 output voltages able to deliver maximal power are required, but with a joint power consumption (across both outputs) that never exceeds the maximal power. Alternatively a separate converter for each output can be used, both designed for maximal power. The proposed solution uses approximately half the area needed by 2 separate converters.

The amount of power delivered to each output can be varied by means of the period during which \( C2_1 \) (\( T_1 \)) or \( C2_2 \) (\( T_2 \)) is connected to the rest of the topology (2). This is due to the law of conservation of energy. Conservation of energy also makes clear that the converter has to be designed for maximal (\( P_{tot} = 1 \text{ mW} \)) output power conditions (1). In practice periods \( T_1 \) & \( T_2 \) are determined by the on-time of the output signals, with period \( T \). Output signals \( \Phi_{11}, \Phi_{12} \) and \( \Phi_{21}, \Phi_{22} \) power the
switches $S_{11}$, $S_{21}$, respectively $S_{22}$, $S_{22}$ that connect $C_{21}$, respectively $C_{22}$ to the rest of the converter.

$$E_{\text{tot}} = P_{\text{tot}} T = (P_1 + P_2) T = P_{\text{tot}} (T_1 + T_2)$$

$$E_1 = P_1 T = P_{\text{tot}} T_1 \Rightarrow P_1 = P_{\text{tot}} \frac{T_1}{T}$$

A capacitive DC-DC converter operates in at least 2 phases [5]. $\Phi_1$ & $\Phi_2$ (with a switching frequency of $f_{sw} = 1/T_s$). The period of the output control signals therefore has to be selected carefully (Fig. 2). At all times each of the outputs should run through both phases, which means the on-times $T_1$ & $T_2$ of the output signals have to contain a whole number of switching frequency periods ($T_s$). The frequency of the output control signals ($f_o = 1/T$) is therefore chosen equal to the greatest common divider (gcd) of both power distribution factors (3).

The power distribution factor $P_{\text{dis}}$ gives the relative amount of power going to the second output. The power distribution factor of the first output is therefore equal to $1 - P_{\text{dis}}$.

$$f_o = \gcd (P_{\text{dis}}[\%], (1 - P_{\text{dis}})[\%])$$

$$P_{\text{dis}} = \frac{P_2}{P_{\text{tot}}}$$

Figure 2 gives the timing diagram corresponding to a full load condition, with $2/3$ of the power being delivered to the first output. It illustrates the timing constraints that have to be met in order to guarantee correct converter operation.

B. Design Methodology

1) Output impedance model: A capacitive DC-DC converter can be described by the output impedance model [5], [6]. The topology determines the maximal achievable output voltage ($V_{\text{id}}$), which under loaded conditions is lowered by the output impedance ($R_{\text{out}}$) of the converter. $R_{\text{out}}$ is determined by the capacitors at low frequencies ($R_{\text{SSL}}$) and by the switches at high frequencies ($R_{\text{FSL}}$) [5]. Both $R_{\text{SSL}}$ (5) and $R_{\text{FSL}}$ (6) were calculated by means of charge multiplier vectors ($\vec{a}_c$ and $\vec{a}_r$), that can be determined by inspection of the topology [5].

$$R_{\text{out}} = \sqrt{R_{\text{SSL}}^2 + R_{\text{FSL}}^2}$$

$$R_{\text{SSL}} = \sum_i \frac{a_{c,i}^2}{C_i f_{sw}} \Rightarrow \vec{a}_c = [a_{c,1}, \ldots, a_{c,N}]$$

$$R_{\text{FSL}} = \sum_i \frac{R_i a_{r,i}^2}{2} \Rightarrow \vec{a}_r = [a_{r,1}, \ldots, a_{r,N}]$$

Based on the required output voltages and load conditions, the required output impedances are determined. The density of on-chip capacitors is fixed. The chip area thereby determines the maximal amount of integratable capacitance. The design procedure therefore starts by making an assumption for the maximal available converter capacitance, given the available area. Using equation (7) the required switching frequency for each output is determined. Equation (6) also shows that both output resistances, and therefore output voltages, can not be chosen independently. The highest of both switching frequencies is therefore selected, resulting in the lowest $R_{\text{FSL}}$ (6) for both outputs. The total capacitance ($C_{\text{tot}}$) and conductance ($G_{\text{tot}}$) are then distributed among the capacitors and switches [5] according to equation (7) and equation (8) respectively, making use of the charge multiplier vectors corresponding to the selected output. The output impedance of the other output can then be determined by using (5), (6) & (4). This output impedance is used to determine the corresponding optimal output voltage.

In order to reduce the area impact, $C_{21}$ and $C_{22}$ are chosen to have half the theoretically optimal size. Simulations show that this has a negligible impact on converter efficiency. On average, the efficiency is only 0.97% lower than for the optimal capacitance distribution.
The hysteretic controller (Fig. 3) aims to keep the output voltages constant, independent of load conditions. The regulator only passes the switch control signals ($\Phi_1, \Phi_2$; respectively $\Phi_1', \Phi_2'$) controlling each output, if the corresponding output voltage is less than the nominal voltage ($V_{ref}$). The regulator uses 4 comparators to compare the output voltages to the desired voltages, 2 for each output, controlled by $Clk_{out}$ and $\overline{Clk}_{out}$. During control phase $Clk_{out}$ preference is given to the regulation of output 1, during control phase $\overline{Clk}_{out}$ on the other hand the regulation of output 2 is preferred (Fig. 2). If the output voltage is high enough during the corresponding preferential phase, the other output can ‘steal’ this control phase if required ($\text{Steal}_{C1}$ & $\text{Steal}_{C2}$). $\text{Steal}_{C1}$ and $\text{Steal}_{C2}$ are generated by NOR-ing the comparator results of each output. This ‘steal’-cycle system automatically adapts the on-time of the output-signal to the load conditions, enabling the regulation of both outputs (based on condition (2)).

In order to preserve correct converter operation, the control-signals $Clk_{out}$ and $\overline{Clk}_{out}$ have to contain an integer number of converter switching periods ($T_s$). Condition (3) should therefore also be met at design conditions. As the converter is designed for $P_{dis} = 0.5$, the frequency of the control-signals ($f_{sw}$) is taken equal to half the switching frequency ($f_{sw}$). As long as $Clk_{out}$ and $\overline{Clk}_{out}$ consist of an integer multiple of $T_s$, the on-time of the output signals will always meet condition (3). Correct converter operation is therefore guaranteed, irrespective of output loading. $\Phi_1, \Phi_1', \Phi_2,$ and $\Phi_2'$ are generated by simply AND-ing the converter phases ($\Phi_1$ & $\Phi_2$) with the appropriate control signals. Two inverting driver stages are used, generating both a regular and an inverse signal, in order to drive the transistors without a significant delay. If the converter is not operating at maximal load, switches $S_1$ and $S_2$ don’t always have to be driven. $\Phi_1'$ and $\Phi_2'$ are therefore generated by OR-ing the output signals of both outputs.

IV. MEASUREMENT RESULTS

A proof of concept chip was fabricated in a 90 nm bulk CMOS technology (Fig. 4). The non-overlapping converter clock phases ($\Phi_1$ & $\Phi_2$) are derived from an external clock by an on-chip non-overlapping clock generator (Fig. 1). The output control signals $Clk_{out}$ and $\overline{Clk}_{out}$ are derived from the external clock by an on-chip clock divider (Fig. 1).

MOS-capacitors made from low-leakage low-Vt PMOS-transistors were used to implement the on-chip capacitors. In the available technology, these capacitors showed to have the highest density combined with a reasonably low parasitic ground-coupled capacitance. The density of MOS-capacitors also decreases rapidly around $V_t$ [7]. The converter topology uses relatively low capacitor voltages, which makes the use of low-Vt transistors beneficial. The converter core uses 5 nF of on-chip capacitance. An extra 6 nF of on-chip capacitance...
is used for in- and output decoupling. On top of the MOS-capacitors additional MIM-capacitors were placed for extra decoupling. The entire chip uses a total area of 1.65 mm$^2$.

Figure 5 shows the converter efficiency in function of the power distribution between both outputs ($P_{\text{dis}}$), for 1000 µW (maximal load), 800 µW and 500 µW load conditions. Both a 2/3 and a 1/3 down-conversion are performed, from an input voltage of 1.2 V to 0.755 V and 0.32 V respectively. It achieves an efficiency of 68.6% for the nominal design case of equal power distribution between both outputs $P_{\text{dis}} = 0.5$ at maximal load. The test chip measurements show this efficiency to be almost constant across load conditions.

The efficiency clearly decreases with increasing power delivery to the lowest output voltage. This can be attributed to the lower $\gamma$-factor ($\gamma = \frac{V_{\text{id}}}{V_{\text{out}}}$) corresponding to this output [5]. Nevertheless, both outputs achieve a substantial efficiency improvement upon a linear regulator at full load conditions. If only one output is considered, the efficiency can be compared to a linear regulator by means of the Efficiency Enhancement Factor (EEF) introduced in [8]. The EEF at full load of the 0.755 V ($P_{\text{dis}} = 0$) and 0.32 V ($P_{\text{dis}} = 1$) output, are equal to respectively 16.5% and 56.7%.

Figure 6 shows the efficiency of the converter when the load is distributed equally between both outputs ($P_{\text{dis}} = 0.5$). The total load is varied from 25 µW up to 1000 µW due to the hysteretic regulator, the efficiency should remain constant irrespective across load variations. The output impedance losses and the parasitic losses both reduce proportionally with power consumption. The measurements nevertheless shows a small decrease in efficiency with lowering power demand. This is caused by the static power consumption of the comparators and clock generating circuits.

The output voltage variation across the load sweep from 25 µW up to 1000 µW ($P_{\text{dis}} = 0.5$), is also shown. Both output voltages are kept constant by the on-chip hysteretic control loop. Output voltage variations of 40.6 mV and 19.5 mV are observed, for the 0.755 V and 0.32 V output respectively.

V. CONCLUSION

In this work a fully integrated Dual-Output capacitive DC-DC converter is presented. The converter is able to deliver 1 mW of total output power and realizes both a 2/3 and a 1/3 voltage conversion, from 1.2 V to 0.755 V and 0.32 V respectively. It achieves an efficiency of 68.6%, when output power is distributed equally between both outputs. A peak efficiency of 75.3% is reached, when full load is applied to the 0.755 V output. The output voltages are kept fixed, irrespective of load conditions, by means of an on-chip hysteretic controller. The entire system is implemented in a 90 nm bulk CMOS technology.

The converter has an area benefit of almost 50% (compared to 2 separate converters) when 2 outputs with a maximal joint output power of 1 mW are needed, regardless of power distribution between both outputs.

REFERENCES


