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A 60 GHz Dual-Mode Power Amplifier with 17.4 dBm Output Power and 29.3% PAE in 40-nm CMOS

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Abstract—A 60 GHz dual-mode power amplifier (PA) is implemented in 40-nm bulk CMOS technology. The PA consists of two unit PAs with a transformer-based power combiner at the output. To reduce the power consumption and hence extend battery life time, one unit PA is tuned off in low-power mode. A switch is employed to short the output of this off-state unit PA and thus improves the back-off efficiency. The PA achieves a saturated output power (P_{SAT}) of 17.4 dBm with 29.3% PAE in high-power mode and a P_{SAT} of 12.6 dBm with 19.6% PAE in low-power mode. The PA with the power combiner only consumes an active area of 0.074 mm². The reliability measurements are also performed and the PA has an estimated lifetime of 80613 hours.

I. INTRODUCTION

The 9 GHz unlicensed band around 60 GHz (57 to 66 GHz) has permitted multi-Gbps wireless communications, invoking the standardizations (e.g., IEEE802.15.3c, IEEE 802.11ad and ECMA-387) and industry-led consortia (e.g., WiGig and WirelessHD). To enable the commercialization of the 60 GHz consumer electronics (especially the mobile devices), it is important to design low power 60 GHz radios and thus extend the battery lifetime. IEEE 802.15.3c [1] specifies the single carrier (SC) mode PHY Class 1 to address low power applications with a relatively high speed of 1.5 Gbps where only $\pi/2$ BPSK and (G)MSK are supported. WiGig specification [2] also defines the mm-wave low power SC PHY mode, which provides lower processing power requirements for mm-wave transceivers.

The mm-wave power amplifier is the most power-hungry block in 60 GHz transceiver, which is supposed to deliver at least 10 dBm output power to set up a communication range of 1 m. As the operating frequencies approach a fraction of the transistor's f_T/f_{MAX} , the decreasing transistor power gain and lossy passive components limit the output power and efficiency of the PA. To achieve sufficient output power at mm-wave frequencies, the power combining technique is commonly used [3], [4]. The on-chip power combiner at PA output sums up the output power of several unit PAs and matches the PA output to 50 Ω . In addition, it also provides the feasibility of switching off some of the unit PAs to reduce

the power consumption at back-off region, when only a short-range or low data rate communication is requested.

Although the dual-mode PA [5], [6] that allows low power operation is popular at low-GHz frequencies, it has not been demonstrated at mm-wave frequencies before due to the implementation challenges in both the combiner design and the layout floor planning. This paper presents the first 60 GHz dual-mode PA in 40-nm bulk CMOS technology, which features a P_{SAT} of 17.4 dBm with 29.3% PAE in high-power mode and a P_{SAT} of 12.6 dBm with 19.6% PAE in low-power mode. Compared to other prior linear PAs at 60 GHz, this PA achieves the highest reported PAE in silicon-based technologies. Furthermore, the proposed dual-mode PA doubles the efficiency at back-off power.

The paper is organized as follows. Section II details the design strategies of the dual-mode PA. Section III presents the experimental results while Section IV discusses the long term reliability of the proposed PA. The conclusions are given in Section V.

II. DUAL-MODE POWER AMPLIFIER

The schematic of the 60 GHz dual-mode PA is shown in Fig. 1. The design incorporates two unit PAs with a transformer-based power combiner at the output. Each unit PA is a three-stage differential amplifier while the transistor sizes of three gain stages are scaled by a factor of two. The common-source (CS) stage is chosen as the last two amplifier stages for its superior power gain at mm-wave frequencies (i.e., 2 dB higher in maximum power gain at 60 GHz compared with common-gate stage). The common-gate (CG) stage works as the input stage, which has 10 times lower input impedance than CS stage at 60 GHz. It simplifies the design of the input matching network and reduces its insertion loss which compensates for the relatively low power gain of the CG stage. The neutralization technique is adopted by cross-connecting the interdigitated metal-oxide-metal (MOM) capacitors between the drain and gate terminals to improve the stability and reverse isolation at mm-wave frequencies. The improved reverse isolation also helps to reduce the iterations of matching network design and load-pull simulation. Thanks

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Figure 1. Simplified schematic of the dual-mode PA.

to the advanced CMOS technology that provides sufficient power gain (i.e., 10 dB) for a single amplifier stage, the PA is biased in class AB mode to ensure high efficiency. In low-power mode, the gate bias of one unit PA is switched off to save approximately 50% power consumption.

The transformer-based combiner (encircled in Fig. 1) is employed for power combining and ensures a compact layout. It is implemented in an overlay structure with the top two metals. Both metal layers have a thickness of only 0.9 μm . The combiner achieves an insertion loss of 1.2 dB, including the loss of output interconnects and pad parasitics. The supply currents are fed through the center-tap (virtual-ground) of the primary windings. However, when one unit PA is switched off in low-power mode, the combiner loss can be as high as 5 dB due to the extra loading at combiner primary side caused by the parasitic capacitance of the off-state PA. In this paper, we propose to employ a MOS transistor switch to short the output differential terminals of this off-state PA, which significantly reduces the insertion loss of the combiner in low-power mode. Fig. 2 shows the insertion loss of the combiner by sweeping the on-resistance (R_{ON}) of the switch. An R_{ON} of 10 Ω is used in the design, which reduces the insertion loss from 5 to 2.3 dB. In addition, to compensate the 1 dB difference in the insertion loss of the power combiner between high-power and low-power modes, the input matching network (i.e., a transformer and differential transmission lines) is optimized

Figure 2. Insertion loss of the power combiner vs. switch R_{ON} in low power mode.

Figure 3. Die microphotograph.

for the low-power mode so that the PA can provide similar power gain in both modes.

To minimize the parasitic capacitance introduced by the switch, the thin-oxide transistor with gate length of 40 nm is used. To ensure the reliable operation, the gate of the switch transistor is biased at 0.5 V for the on-state PA and 2 V for the off-state PA with a supply voltage of 1 V. The maximum voltage across the gate oxide of the switch in both states is approximately 1 V, which leaves sufficient margin to avoid gate oxide breakdown. The long-term reliability of the PA will be further discussed in Section IV.

III. EXPERIMENTAL RESULTS

The 60 GHz dual-mode PA with output power combiner is implemented in 40-nm bulk CMOS technology. Fig. 3 shows the chip microphotograph and the active area of the PA is only 0.074 mm^2 . The measurements are performed on a high-frequency probe station with the DC and low-frequency pads wire-bonded to a PCB. The PA consumes 153 and 80 mW in high-power and low-power modes, respectively, from a supply voltage of 1 V.

Fig. 4 shows the gain and output power of the PA in both modes, measured by a V-band power sensor and a high precis-

TABLE I. 60GHz CMOS PA PERFORMANCE COMPARISON

	This Work (High/Low)	[3]	[4]	[7]	[8]
PAE _{MAX} [%]	29.3/19.6	3.6	15.1	14.4	25.7
P _{SAT} [dBm]	17.4/12.6	18.1	18.6	14.5	14.5
P _{IdB} [dBm]	14.0/9.5	11.5	15.0	11.2	12.7
P _{DC} [mW]	153/80	1504	480	180	90
V _{DD} [V]	1	1.8	1	2	1.8
Tech. [nm]	40	65	65	45	65(SOI)
Area [mm ²]	0.074	0.462	0.12*	0.04	0.3*

* Estimated from the chip micrograph.

Figure 8. Measured lifetime of the PA under stress and predicted lifetime.

IV. RELIABILITY

The long term reliability of a linear PA (e.g., class A, AB) is restricted by hot-carrier injection [9]. The device degradation due to hot-carrier injection can be fit with a commonly used empirical model [10] and thus lifetime of a PA can be estimated by applying DC and RF stress at room temperature. To accelerate the degradation of the device characteristics, excessive supply voltage was applied to the PA with an output power of 14 dBm (P_{IdB} at 1 V supply) during the measurement. Note that even under stress voltage, the hot-carrier injection is still the dominant mechanism of the device degradation because typical gate oxides break down with an electric field of 10 MV/cm due to Fowler-Nordheim tunneling. This corresponds to approximately 2 V for the gate oxide thickness used in this 40-nm CMOS technology.

The lifetime is defined as the time when the drain current of the PA output stage is dropped by 10%. It can be estimated by the following reliability model [10]:

$$\text{Lifetime} = b \times \exp(c / V_{DSpeak}) \quad (1)$$

where b and c are fitting parameters and V_{DSpeak} is the simulated peak drain-source voltage across the CS transistor of the output stage with 14 dBm output power. When the drain

current (I_d) of the output stage is dropped by 10%, the measured output power is reduced by less than 0.5 dB. Fig. 8 shows the measured lifetime of the PA under DC and RF stress conditions with different excessive supply voltages. By extrapolation, the PA shows a predicted lifetime of 80613 hours (9.2 years) when it continuously works at 14 dBm output power and 1 V supply voltage. In practical wireless communication, the peak to average ratio of the modulated signals varies between 3 and 10 dB, which further ensures the long term reliability of the proposed PA.

V. CONCLUSION

A 60 GHz dual-mode PA with a power combiner is designed using 40-nm bulk CMOS technology. The PA can be switched to low-power mode and thus saves approximately 50% power consumption. In the design, circuit level optimization and trade-off are performed to ensure the good performance in both modes. The PA achieves a P_{SAT} of 17.4 dBm with 29.3% PAE in high-power mode and a P_{SAT} of 12.6 dBm with 19.6% PAE in low-power mode. The reliability measurements are also conducted and a lifetime of 80613 hours is estimated based on a commonly used empirical model.

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Figure 4. Measured gain and output power vs. input power in high-power mode (black), low-power mode with switch short (solid gray) and low-power mode with switch open (dashed gray) at 61 GHz.

Figure 5. Measured PAE and DC power consumption vs. output power in high-power and low-power (gray) modes at 61 GHz.

ion power meter. The small-signal gain is 21.2 dB in high-power mode and 21.6 dB in low-power mode at 61GHz. The gain difference between two modes is less than 0.5 dB, thanks to the design approaches discussed in section II. The PA delivers a P_{SAT} of 17.4 dBm with 14.1 dBm P_{1dB} in high-power mode while it shows 12.6 dBm P_{SAT} with 9.5 dBm P_{1dB} in low-power mode. When both switches are open in low-power mode, the gain and the output power drop by about 5 dB (see dashed gray curves in Fig. 4), indicating the necessity to short the output of the off-state PA.

Fig. 5 shows the PA achieves the peak PAEs of 29.3% and 19.6% in high-power and low-power modes, respectively. Compared to the high-power mode, the PA doubles the PAE in low-power mode when the output power is less than 12 dBm, clearly showing the benefits of the dual-mode PA. Fig. 5 also shows the power consumption is reduced by about 50% in low-power mode, thus affording significant savings of battery power.

The peak PAE and P_{SAT} of both modes are measured across 57-66 GHz frequency band, as shown in Fig. 6. In high-

Figure 6. Measured PAE and P_{SAT} vs. frequency in high-power (black) and low-power (gray) modes.

Figure 7. Measured P_{1dB} and OIP3 vs. frequency in high-power (black) and low-power (gray) modes.

(low-) power mode, the PAE is $26.1 \pm 3.2\%$ ($17.7 \pm 4.2\%$) while P_{SAT} reaches 17.0 ± 0.4 dBm (12.5 ± 0.6 dBm).

The linearity of the dual-mode PA versus frequency is shown in Fig. 7. From 57 to 66 GHz, the P_{1dB} and OIP3 achieve 12.4 ± 1.7 dBm and 21.7 ± 2.2 dBm in high-power mode while they are 8.3 ± 1.6 dBm and 16.8 ± 1.8 dBm in low-power mode. The two-tone signals are generated by two V-band signal sources with a magic tee hybrid coupler.

Table I summarizes the performance of the proposed dual-mode PA and compares it with the other state-of-the-art 60 GHz PAs in CMOS. Ref. [3] uses 8-way power combiner and operates at a relatively high supply voltage to achieve high output power, which compromises the efficiency and consumes relatively large active area. The proposed PA achieves the highest PAE in both modes and it only consumes half of the DC power when operating in low-power mode. Note that as the proposed PA is optimized for both modes, the performance of the PA in high-power mode is thus compromised. For instance, a combiner as in [4] cannot be used in the design which has relatively low insertion loss.