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(article begins on next page)

A 265V_{RMS} Mains Interface Integrated in 0.35 μ m CMOS

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Abstract—A fully integrated 265V_{RMS} input AC-DC interface is demonstrated in a 0.35 μ m CMOS technology, needing only 1 external low voltage SMD capacitor for improved performance. The converter can directly interface the universal line voltage (50-60Hz) and converts this into a regulated DC voltage of 3.3V. High input voltage operation is made possible through custom layout of high voltage capable passive components. A model of an ideal AC-DC capacitive step-down converter is presented and the proposed circuit architecture is designed to approach maximum attainable power throughput. The prototype converter demonstrates a maximum output power of 287 μ W on a die area of 6mm² and enables integrated circuits to be supplied straight from the ubiquitous mains voltage. Hereby circumventing the need for traditional converters using high voltage discrete components.

I. INTRODUCTION

In everyday integrated circuits a DC supply voltage is assumed to be available. But where does it come from? The power source can either be harvested power or the mains grid as batteries are just energy carriers and need to be recharged.

For the first option it is possible to harvest RF radiation, kinetical, thermal or solar energy. However the power output of a harvester is related to the power available in its environment and therefore is subjected to uncertainty. Hereby system down times may occur which can last for extended periods of time.

Alternatively the mains grid proves to be a very reliable source of power and is widely available. Unfortunately for integrated circuits the mains grid distributes power in the form of a high voltage low frequency sine wave, specified in regional standards. This generally requires converters employing a discrete rectifier and a transformer [1], taking up significant PCB area.

In this work an integrated system is proposed, eliminating the need for high voltage rated external components, drastically reducing footprint. This approach encompasses the monolithic integration of a capacitive step-down interface that separates the active circuit from the high input voltage, enabling integrated circuits to operate straight from the mains. This is a promising feature that opens up the mains as possible power source for various new application domains where the otherwise needed discrete converter makes the solution infeasible or too expensive.

This paper is organized as follows. The system architecture and operation are discussed in Section II. Section III presents a model for an ideal capacitive AC-DC step-down converter,

(a) System architecture of the proposed AC-DC converter

(b) Operation waveforms

Fig. 1.

followed by the prototype implementation details in Section IV. Measurements results are reported in Section V and final conclusions are drawn in Section VI.

II. SYSTEM ARCHITECTURE AND OPERATION

The converter topology, shown in Fig. 1(a), consists of 2 high voltage capable passive components R_{in} , C_{in} and a full wave rectifier [2] forming the capacitive step-down AC-DC stage. The output voltage of the AC-DC stage however is determined by the post regulation stage which contains a shunt

path and a series regulator to remove any remaining ripple from V_{DC} .

A. Capacitive AC-DC step-down

To understand the operation it is assumed for the sake of simplicity that $R_{in} = 0$, the rectifier is ideal ($V_{th,M1-M2} = 0$, $V_{D,D1-D2} = 0$), C_{DC} is infinite and charged to a voltage V_{DC} . With a mains RMS voltage V_{AC} present at the input terminals ($V_{C_{in}} = 0$) and $V_{AC,plus}$ referred to $V_{AC,minus}$ increases from 0V up to V_{DC} devices $M1$, $D1$ and $D2$ remain off while $M2$ is on. Next for $V_{DC} \leq V_{AC,plus} \leq \sqrt{2}V_{AC}$, $D1$ turns on and current flows to C_{DC} . Immediately after the mains peak, $D1$ turns off followed soon after by $M2$ since the low terminal of C_{in} starts to float and decreases at the same rate as $V_{AC,plus}$ until a drop of $2V_{DC}$ has taken place. At that time $V_{AC,minus} - V_{AC,plus} = V_{DC}$ and $D2$ turns on, while $M1$ has already turned on just before, providing another current towards C_{DC} . This continues until the negative peak at which $D2$ turns off. The above operation continues to alternate.

Input series capacitor C_{in} separates the active circuit from the high input mains voltage. While the high terminal of C_{in} is subjected to the full mains voltage, meaning a peak-to-peak voltage $V_{ptp,high}$ of $2\sqrt{2}V_{AC}$, this is not true for the low terminal ($V_{AC,low}$). The low terminal is bound by the rectified voltage V_{DC} resulting in a $V_{ptp,low} = V_{DC}$. An input series resistor is added, in addition to C_{in} , to protect the circuit against inrush currents that occurs when the system is connected to the mains at the time of a high voltage or peak while C_{in} is not charged. Without resistor R_{in} a potentially destructive current rushes in to charge C_{in} , only limited by the parasitic series resistance located between $V_{AC,plus}$ and $V_{AC,minus}$.

B. Shunt overvoltage protection and series regulation

Until now it was assumed that C_{DC} was infinite and fixed at V_{DC} , limiting $V_{AC,low}$ with respect to ground during both positive and negative mains half cycle. In practice this is guaranteed by the parallel combination of the shunt path and a low dropout (LDO) series regulator passing the current to the load. At full load the shunt path is inactive and all power passing the rectifier is consumed by the load. The resulting equilibrium of V_{DC} is given in Eq. (1), in which V_{OD} is the time averaged C_{in} overdrive (as given in Eq. 5 and discussed in Section III on modelling) and Z_{out} equals the series combination of LDO and load impedance $Z_{LDO} + Z_{load}$.

$$V_{DC} = \frac{Z_{out}}{Z_{out} + Z_{C_{in},f=f_{mains}}} V_{OD} \quad (1)$$

When load power decreases Z_{out} will quickly increase due to the fact that a reduced load current requires a proportional increased Z_{LDO} to keep V_{reg} regulated at a fixed DC. Consequently V_{DC} will rise according to the newly formed voltage divider (still Eq. 1) and exceed a safe operation voltage limit. For this reason a shunt path was included through M_{sh} in parallel with the series regulator in order to limit V_{DC} to a maximum of $V_{pro} + V_{th,M_{sh}}$ at less than nominal loads.

Fig. 2. Schematical representation of ideal model with AC input voltage, an impedance over which a voltage is dropped, an ideal rectification and a DC output voltage

Fig. 3. Trade-off in achievable output power [μW] as function of parameters C_{in} and V_{DC} for $V_{in,RMS} = 230V$ and $f_{mains} = 50Hz$

III. CONVERTER MODEL

The capacitive step-down introduces an impedance bottleneck resulting from a low mains frequency and a low capacitance value for C_{in} . The latter is caused by the high voltage nature of C_{in} leading to a low capacitance density. This section investigates the maximum attainable power throughput for an ideal AC-DC step-down stage, considering the model depicted in Fig. 2. The power throughput is analyzed given the following set of system parameters: the mains amplitude V_{AC} , the mains frequency f_{mains} , the amount of series input capacitance C_{in} and the V_{out} output voltage.

$$V_{in}(t) = \sqrt{2}V_{in} \sin(2\pi f_{mains}t) \quad (2)$$

$$V_1(t) = V_{in}(t) - V_{out} \quad (3)$$

$$t_1, t_2 \in \{V_1(t) = 0\} \quad (4)$$

$$V_{OD} = \frac{2}{T} \int_{t_1}^{t_2} V_1(t) dt \quad (5)$$

$$I_{C_{in}} = V_{OD} 2\pi f_{mains} C_{in} \quad (6)$$

$$P_{out} = I_{C_{in}} V_{out} \quad (7)$$

Eq. (2) equals the input voltage as function of time. In order to calculate the average capacitor overdrive voltage V_{OD} in Eq. (5), V_{out} is deducted from Eq. (2) and its positive part is

then averaged over a half mains cycle period. Now the average capacitor current and output power can be calculated according to Eqs. (6)-(7).

As seen in Fig. 1(b), the proposed architecture constitutes voltages $V_{AC,low}$ and $V_{AC,minus}$ to exhibit block pulse like behaviour approaching the case of the ideal model, i.e. an AC square wave output of the capacitive AC-DC step-down topology. This is opposed to previous work [3] in which a capacitive voltage divider is employed to reduce the $V_{AC,mains}$ in amplitude to a much lower value $V_{AC,divided}$. This divided voltage is then rectified, showing suboptimal power throughput due to the fact that power can only be transferred when the rectifier diodes turn on ($V_{AC,divided} > V_{rectified}$). For the block pulse behaviour rectifier input of the proposed architecture, the rectifier diode on times are significantly longer than for the sine wave rectifier input of [3], hence improving power throughput.

Since the mains voltage is already standardized, both system parameters V_{AC} and f_{mains} are fixed. Fig. 3 shows the output power capability of an ideal AC-DC stage as function of the 2 remaining degrees of freedom. A trade-off between input capacitance C_{in} and the output voltage V_{out} is observed.

On one hand when V_{out} is fixed, the average capacitor overdrive voltage V_{OD} is also fixed. C_{in} then linearly influences the average input capacitor current according to Eq. (6) and consequently the output power given by Eq. (7).

Alternatively, when keeping the series input capacitor constant, a higher output voltage V_{DC} results in a lower average input capacitor overdrive voltage by Eq. (3)-(5). Due to the asymmetry in capacitor input impedance and load impedance, the output power relation as function of time scales almost linearly for V_{DC} values below 50V.

IV. IMPLEMENTATION

C_{in} bridges the high voltage gap between the high voltage mains input and the low voltages on-chip, as discussed in Section II. While the active circuits do not come in contact with high voltage, the input capacitor C_{in} and input resistor R_{in} are subjected to a maximum voltage of $\sqrt{2}V_{AC}$ totalling up to 375V in the case of $V_{AC,rms} = 265V$. With the oxide in the metal stack having a breakdown of at least $1 \frac{MV}{cm}$ [4], a minimal spacing of $3.75\mu m$ is needed to ensure breakdown will not occur. The input capacitor layout was implemented as a metal-metal fringe capacitor with at least $4\mu m$ of oxide between the capacitor plates. On top of that metal corners were rounded to alleviate the point effect as much as possible.

The input resistor is implemented using a series connection of vias and the top 2 metals in the stack, ensuring a large spacing to the substrate. Oxide spacing exceeds $6\mu m$ to ground and therefore short spikes in the mains input, resulting into additional inrush current events, cause a voltage drop across R_{in} attenuating the voltage spike and relieving C_{in} .

A desired regulated output voltage V_{reg} of 3.3V after linear regulation of the rectified voltage V_{DC} superposed by an LDO dropout voltage V_{LDO} sets the minimum allowed value of V_{DC} . Achieving this headroom for series regulation

while keeping $V_{DC,max}$ constrained to a safe operation value requires sufficient decoupling after the rectifier. Besides its necessity for safe operation it also increases system efficiency as less noise needs to be regulated by the LDO. For these reasons the prototype converter was externally decoupled with a low voltage $1\mu F$ SMD capacitor. Transistors $M1$ and $M2$ are implemented with available thick oxide DMOS devices, as part of a set smart power devices rated up to 25V available in the technology, to ensure safe rectifier operation while Schottky diodes $D1$ and $D2$ do not cause overvoltage issues towards substrate.

The post regulation stage has a dual function. First, it is responsible for limiting the active circuit operation voltage by means of the shunt path. Secondly a series regulator chops off any noise that remains after the previous rectification.

1) *Shunt path*: Transistor M_{sh} is a thick oxide PDMOS device biased with an overvoltage protection control signal V_{pro} . When load power is decreased and V_{DC} increases above $V_{pro} + V_{th,M_{sh}}$ the PDMOS will start to conduct and will limit the maximum of the rectified voltage to a safe value.

Alternatively this shunt path can be addressed to shut down the converter. From Fig. 3 it follows that setting V_{DC} towards zero makes the output power P_{out} also collapse towards zero, achieving shut down.

2) *Low dropout Regulator*: The LDO regulates the rectified voltage into a noise free output voltage V_{reg} . Considering the limited power budget available at the output from the AC-DC stage, it is of significant importance that power consumption of this regulator is low compared to the full budget in order to minimize the impact on system efficiency. To that end static currents in the error amplifier and feedback path were chosen to be $100nA$ and $50nA$ respectively. A Gain-bandwidth of 100kHz was achieved when loaded by the gate capacitance of M_{pass} . The feedback path was chosen to be implemented by a diode connected stack of 6 subthreshold biased PMOS devices in order to create a 1/3 voltage divider on a small chip area.

V. CHIP MEASUREMENTS

The converter prototype was measured for various mains voltage, frequency specifications. Fig. 4 shows the maximum achievable output power as function of the input mains RMS voltage ranging from 85V, 120V, 230V up to 265V and this for both 50Hz and 60Hz cases. It can be seen that the achievable load power scales linearly with the input RMS voltage. When the input voltage frequency is 50Hz, the load power scales from $69\mu W$ for a 85V input up to a maximum of $268\mu W$ at 265V. Similarly with a 60Hz frequency input the load power varies from $87\mu W$ up to $287\mu W$.

Fig. 5 shows the system voltage waveforms of V_{DC} and V_{reg} for the typical EU mains input case. For an input voltage and frequency of $230V_{RMS}$ and 50Hz the converter supplies $208\mu W$. After series regulation of the 900mV ripple peak-to-peak clearly visible in V_{DC} the regulated output voltage V_{reg}

TABLE I
SPECIFICATION COMPARISON TO PRIOR ART

Reference	[3]	This work	This work
Tech node	0.13 μm	0.35 μm	0.35 μm
V_{RMS}	120V	120V	230V
f_{mains}	60Hz	60Hz	50Hz
Power/area	0.43 $\mu\text{W}/\text{mm}^2$	21.5 $\mu\text{W}/\text{mm}^2$	34.6 $\mu\text{W}/\text{mm}^2$
η_{AC-DC}	59%	68%*	57%*
$\eta_{AC-DC+LDO}$	not available	41%*	32%*
V_{reg}	4V	3.3V	3.3V
$P_{out,max}$	1.5 μW	129 μW	208 μW

* Simulation

exhibits a noise of only 120mV peak-to-peak, which is 3.6% of V_{reg} .

For all tested input cases the output voltage V_{reg} can be regulated at a fixed 3.3V over the full load power range from zero up to the maximum achievable load power P_{load} as presented in Fig. 4. This is to be expected from the operation of the shunt path provided by M_{sh} and allows for overvoltage free and stable operation over the full load power range.

A chip microphotograph is given in Fig. 6 and shows the die measuring 6mm². Most of the area is occupied by the integrated high voltage capable passive components C_{in} and R_{in} . For area efficiency a moscap decoupling device routed up to metal 1 was placed underneath the actual high voltage series input capacitor C_{in} fabricated using the metals above. Stacking of these devices was possible without oxide breakdown because only the *high* terminal of C_{in} is subjected to high voltage and was constrained to topmetal.

Finally a comparison of the proposed converter with a prior state-of-the-art integrated AC-DC converter is given in Table I. The measurement results of this converter show improvement on the field of both power density and efficiency, demonstrating the enhanced converter architecture proposed in this work. On top of that the input voltage range has been extended from 120V_{RMS} up to the a maximum of 265V_{RMS}.

VI. CONCLUSION

In this work a high voltage capable capacitive AC-DC step-down interface is fully integrated in 0.35 μm CMOS, altering the external components requirement from multiple high voltage devices to a single low voltage SMD. The presented converter architecture ensures an optimal operation because voltages $V_{AC,low}$ and $V_{AC,minus}$ approach the AC square wave behaviour, as is the case of the ideal model, enabling maximal rectifier diode on times and hence maximal power throughput. The prototype measurements show achievable load powers of 129 μW and 208 μW in the most typical cases of 120V_{RMS}, 60Hz and 230V_{RMS}, 50Hz respectively. This while a fixed 3.3V regulated output can be supplied with a peak-to-peak voltage ripple of 3.6% over the full output power range.

Fig. 4. Maximum output power for a regulated 3.3V output as function of mains specification

Fig. 5. Converter output waveforms for $V_{RMS} = 230\text{V}$, $f_{mains} = 50\text{Hz}$ input and 3.3V output at nominal output power $P_{load} = 208\mu\text{W}$

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Fig. 6. Chip microphotograph