Monolithic Integration of a Class DE Inverter for On-Chip Resonant DC-DC Converters

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***Abstract*— A fully-integrated series resonant class DE inverter is realized in a 130 nm 1.2 V CMOS technology with an on-chip spiral inductor and an integrated MIMcap. It is used as the first stage in fully-integrated class DE DC-DC resonant converters. The inherent soft switching yields high conversion efficiency at high switching frequencies. Low switching peak-voltages are present in the circuit, alleviating the need for on-chip high-voltage techniques. The use of on-chip passives reduces the bill of materials (BOM) considerably. The maximum output power of the series resonant class DE inverter is 11.6 mW. The maximum power efficiency is 65.2 %. The measurement results confirm and improve previous simulations.**

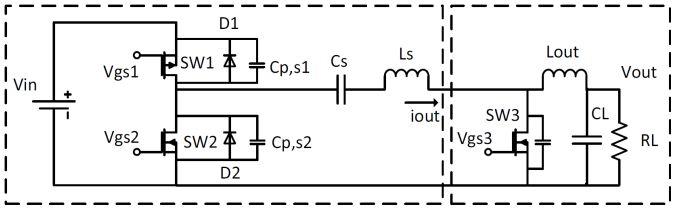
I. Introduction

One of the major techniques to reduce cost, size and power consumption in state-of-the-art applications is the monolithic integration of electronic systems. This trend was first observed in the successful integration of RF mixed-signal building blocks [1]. A following step in this integration paradigm is the integration of another building block: the power supply. Recent research efforts cleared the path to develop fully-integrated DC-DC converters in standard CMOS [2].

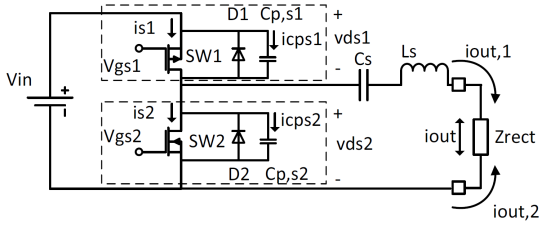
When all the building blocks are integrated on a single die, multiple supply voltages are required. For example, the digital circuitry will need a lower supply voltage than the on-chip power amplifier which must deliver enough power into the communication medium. Therefore, multiple voltage domains need to be created to accommodate for all different supply voltages.

Because of the continuing miniaturization, battery-powered portable wireless applications result. The battery voltage is usually too high for the deep-submicron technologies used. Therefore, the supply voltages need to be decreased. This is typically done using low efficient linear regulators. To reduce the powerlosses, on-chip switching power supplies can be used, increasing the efficiency and battery lifetime. An interesting application is the supply for digital memories, requiring low supply voltages to reduce the dynamic losses.

Among the switching power supplies, the resonant switching DC-DC converters achieve high efficiency using a resonant circuit and high frequency inverters. Examples are class E inverters [3] and class DE inverters [4] achieving high efficiency at high switching frequencies due to the inherent decreased switching losses in these topologies. These reduced switching losses are inherent for resonant circuits as will be explained later. In a class E inverter, high peak switching voltages are present, up to four times the supply voltage. However, the breakdown voltage for transistors in deep-submicron technologies is low, requiring measures to prevent degradation or breakdown of the switches. For a class DE inverter on the other hand, the peak switch voltage will be limited to the supply voltage. It is thus more suitable for integration in deep-submicron technologies.



(a) Class DE DC-DC converter with series resonant class DE inverter (left) and class E synchronous rectifier (right).



(b) Equivalent circuit used for the design of the series resonant class DE inverter.

Fig. 1. Class DE DC-DC converter circuit and equivalent schematic.

This paper presents a resonant class DE DC-DC converter, using a fully-integrated series resonant class DE inverter as a first stage. The architecture and operation principles of the converter are described in section II. The implementation of the most important components of the series resonant class DE inverter is discussed in Section III. Section IV describes the measurement results. Finally, conclusions are drawn in section V.

II. Architecture

A. Class DE DC-DC converter

Figure 1(a) illustrates the schematic of a resonant class DE DC-DC converter with ideal components.

It consists of a series resonant class DE inverter and a synchronized class E rectifier. The inverter is loaded with the

input impedance Z_{rect} of the rectifier. This is shown in Figure 1(b) as an equivalent circuit which is useful for analysis and is used for the design of the series resonant class DE inverter.

A resonant power converter has some advantages over switching PWM converters. These PWM converters will suffer from switching losses and low efficiency at high frequencies [5]. The chief advantage of resonant converters is their reduced switching loss. This is achieved via mechanisms known as zero-current switching (ZCS) and zero-voltage switching (ZVS). The turn-on and turn-off transitions of the various converter switches can occur at zero crossings of the resonant converter quasi-sinusoidal waveforms. This will reduce switching losses, meaning that resonant converters can be operated at higher switching frequencies than PWM converters. Zero-voltage switching can also eliminate some of the sources of converter-generated electromagnetic interference.

The series resonant class DE inverter generates an AC voltage which is fed into a series resonant LC-tank, formed by L_s and C_s. Thereafter, it is fed into the synchronized class E rectifier. The DC output voltage of the rectifier is filtered by output capacitor C_L and is also the output voltage V_{out} of the converter. The voltage conversion ratio $k(f_{SW})$ of the converter is calculated by means of the transfer function $||H(f_{SW})||$ between the input and the output. This is further elaborated in [6], but out of scope to be discussed in this paper.

B. Series resonant class DE inverter

Figure 1(b) illustrates the schematic of a series resonant class DE inverter with ideal components. It consists of two MOS transistors $SW1$ and $SW2$, a MIM-capacitor C_s, an inductor L_s and a resistive output load Z_{rect}. The capacitor, inductor and resistor form the series resonant tank. The capacitors $C_{p,s1}$ and $C_{p,s2}$ are the parasitic output capacitances of the MOS transistors. Diodes $D1$ and $D2$ are the intrinsic body-drain pn-junction diodes. These will be used as anti-parallel diodes. The switches turn on and off periodically. This is controlled by a non-overlapping clock: there is a dead-time between the switch on-times to prevent short-circuit currents flowing through both transistors. The operation is described as follows. During the first switching stage $SW1$ is closed and $SW2$ is open. The current $i_{out,1}$ through the inductor and capacitor now starts to flow. During the second stage $SW1$ is open and $SW2$ is closed. The current $i_{out,2}$ due to the stored magnetic and electric energy in the resonant tank now flows in the opposite direction of $i_{out,1}$. Over one complete period, the current i_{out} through this resonant tank is nearly a sine wave. The output load Z_{rect} sees this sinusoidal current that changes direction every clock cycle, this yields an AC voltage across the load resistor. This principle of operation is also explained by the waveforms, sketched in Figure 2.

1) Inherent reduced switching losses: An interesting feature of this topology is the inherent reduced switching loss compared to a classic pulse-width modulated (PWM) switch-mode power supply. Figure 2 shows the waveforms for the operation at, below and above the resonant frequency of the series resonant converter. For operation at the resonant frequency,

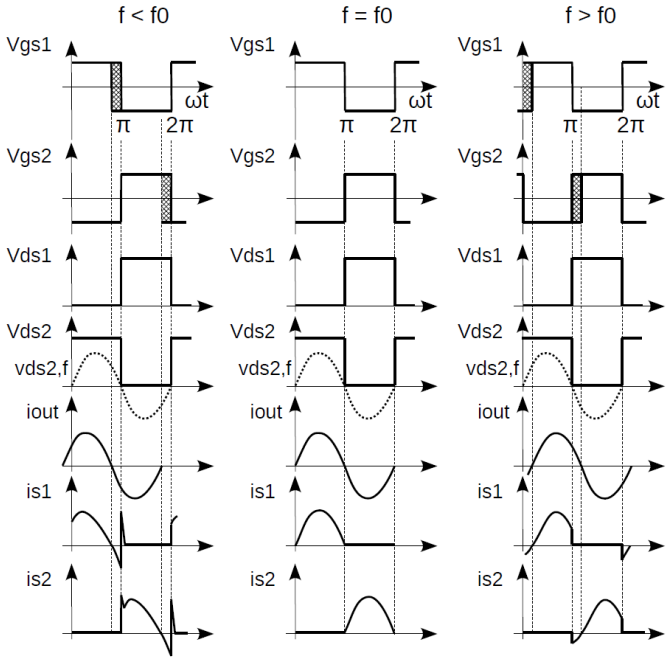


Fig. 2. Waveforms for operation at $f < f_0$, $f = f_0$ and $f > f_0$.

$f = f_0$, the transistors turn on and off at zero current, resulting in low switching losses and high efficiency. In many cases, the operating frequency f is not equal to the resonant frequency f_0 since the output voltage and power can be controlled by varying the operating frequency f. Each transistor should be turned off for $f < f_0$ and turned on for $f > f_0$ during the time interval when the switch current is negative. During this time, the current can flow through the anti-parallel diode. To prevent short-circuit currents, a non-overlapping clock with sufficient dead-time must be used.

When the inverter is operated below resonance, zero-current switching (ZCS) will occur. The series resonant circuit will represent a capacitive load [7], this means that the current i through the resonant tank will lead the fundamental component $v_{ds2,f}$ of the voltage v_{ds2}. In this case, the transistor current goes to zero before the transistor is turned off. The circuit inherently causes the turn-off transition to be lossless. However, when the transistor is turned on, its parasitic output capacitance is discharged through its on-resistance, causing a switching loss.

When the inverter is operated above resonance, zero-voltage switching (ZVS) will occur. The series resonant circuit now represents an inductive load. The circuit naturally causes the transistor voltage to become zero before the transistor is turned on. The current i lags $v_{ds2,f}$. The turn-on transition is now lossless. Both the switch voltage and current waveforms overlap during turn-off, causing a switching loss.

2) Exploiting the parasitic output capacitances: To assist the turn-off process above resonance, small shunt capacitors can be introduced in parallel with the transistors. The transistors used in this circuit are sufficiently large to use the output capacitances $C_{p,s1}$ and $C_{p,s2}$ as shunt capacitors. These shunt capacitors eliminate the turn-off switching loss

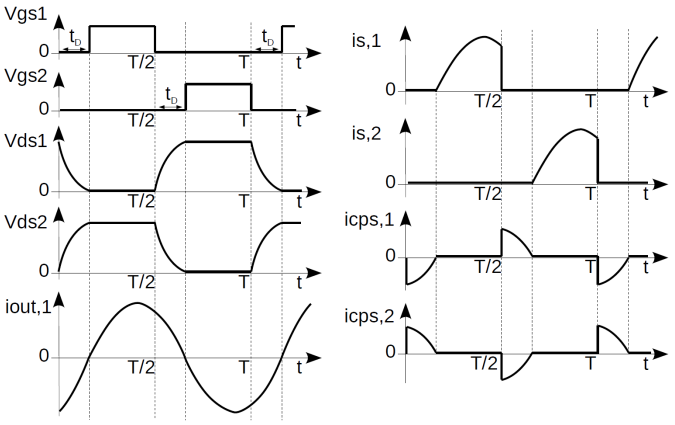


Fig. 3. Waveforms for the series resonant class DE inverter.

during operation above the resonant frequency. This principle is depicted in Figure 3. There is again a dead time in the gate-to-source voltages, during which both transistors are off. During the dead time, shunt capacitors become part of the resonant circuit. One shunt capacitor is charged and the other is discharged during the dead time. These capacitors introduce commutation intervals at transistor turn-off. When $SW1$ is turned off, the tank current flows through capacitance $C_{p,s1}$ instead of $SW1$ itself and the voltage across $SW1$ and $C_{p,s1}$ increases. If the turn-off time is sufficiently fast, the transistor is turned off before the drain voltage rises too much above zero. A negligible switching loss is now incurred. This series resonant converter achieves the class E switching conditions [3], which means zero-voltage switching and zero-voltage slope switching. This topology enables higher efficiency since it eliminates switching power losses during the transition time of the switches.

C. Class E synchronous rectifier

The right part of the resonant DC-DC converter in Figure 1(a) is the class E synchronous rectifier. This is a resonant rectifier [8]: a sinusoidal input current i_{out} will be translated into a DC output current. This current will be limited by the output inductor L_{out}. Instead of a diode in a typical class E rectifier, a synchronized switch $SW3$ is used. This circuit can operate efficiently at high frequencies because the switch turns on and off at zero voltage (low dv/dt) and turns off at zero current (low di/dt). This reduces the switching losses significantly. High efficiencies are reported for this type of monolithic synchronous rectifiers [9].

III. Implementation

The series resonant class DE inverter is implemented as a part of a resonant class DE DC-DC converter. The implementation of the synchronous class E rectifier is omitted here. In this paper, the focus is on the efficient design of the series resonant class DE inverter as a fully-integrated building block to achieve high frequent and highly efficient resonant DC-DC converters. The design and layout of the different components in the series resonant class DE inverter are discussed in this section. Since the class DE inverter is integrated on-chip

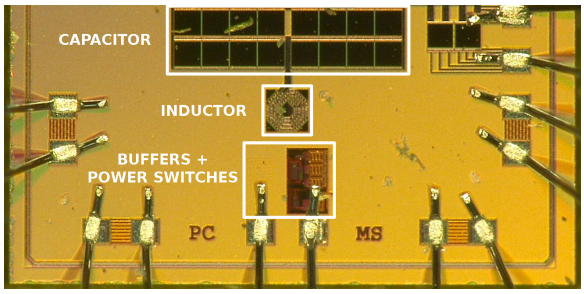


Fig. 4. Die photograph of the chip.

without rectifier, an external load resistor is needed to serve as an input impedance. This corresponds to the load Z_{rect} in Figure 1(b).

The inductor is implemented as an octagonal metal track, hollow spiral inductor. A standard metal layer, a thick top metal layer of $2\mu m$, and an aluminium layer of $1.2\mu m$ are used to reduce the parasitic series resistance. It consists of 2 windings of $20\mu m$, resulting in a total on-chip inductance of $1.7nH$. The load is connected off-chip using a bondwire, this introduces extra inductance. The total measured extracted inductance equals $5.1nH$. The series resistance at a frequency of 500MHz is $0.5\ \Omega$, and is taken as an upper limit since the inverter is designed to be used around 100MHz. The inductor area is $125\mu m$ by $125\mu m$. This can be seen in the middle of Figure 4.

The capacitor in the presented class DE inverter is implemented by means of a MIMCAP. In the used technology this yields a capacitance density of $2fF/\mu m^2$. A total capacitance of $145.6pF$ is realised. The electrical series resistance was estimated using the sheet resistances of the two metal layers, resulting in 0.8Ω. The capacitor can be seen in the top part of Figure 4.

The power switches, $SW1$ and $SW2$ are implemented using a fingered layout. The width of the power switches is $1.8mm$ and $0.75mm$ respectively. This width yields an optimal trade-off between losses in the buffers driving the switches and the conduction losses. The switches are driven by two buffer trains. The buffers apply the non-overlapping clock to the pMOS ($SW1$) and nMOS ($SW2$) transistor. These buffers and power switches are located in the bottom part of Figure 4.

IV. Measurements

A series resonant class DE inverter is implemented in a $130\ nm$ $1.2\ V$ CMOS technology. It measures $1.5\ mm$ x $0.75\ mm$. Figure 4 shows a die photograph. Figure 5 shows the efficiency of the inverter as a function of the output power at varying resistive loads. The maximum efficiency is $65.2\ \%$ at a load of $6.9\ mW$ with an output peak amplitude of $585\ mV$ at a switching frequency of 100 MHz. A maximal output power of $11.6\ mW$ is achieved at an efficiency of $47\ \%$ with an output peak amplitude of $312\ mV$. Figure 6 shows the efficiency of the inverter in function of the switching frequency for a load of $25\ \Omega$. An efficiency of 65.2% is achieved. At

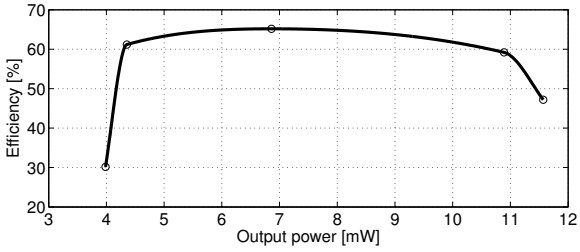


Fig. 5. The efficiency of the series resonant class DE inverter for varying loads.

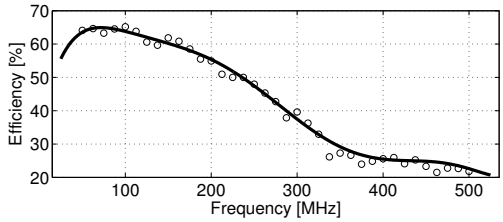


Fig. 6. The efficiency at increasing frequency for a 25 Ω load.

a higher switching frequency, the efficiency decreases. It is paramount to control the switching frequency as to achieve the highest efficiency. This point is shifted depending on the output load. For this integrated circuit, the efficient switching frequency will be around 100 MHz, depending on the load used. In Figure 7 the output voltage sine wave at 100 MHz is presented for a load of 25 Ω. The peak amplitude of the output waveforms is given in Figure 8 in function of the switching frequency. There is a peak around 100 MHz. It is seen that the amplitude of the output waveform can be controlled by the switching frequency. This range of amplitudes is interesting for the on-chip supply for digital memories. Table I summarizes the measurement results and makes a comparison with existing simulations of an integrated series resonant class DE inverter [4]. The measurements of the discussed monolithic series resonant class DE inverter confirm these simulation results. Moreover, the performance is increased compared to the simulated results.

V. Conclusion

A fully-integrated series resonant class DE inverter is realized in a 130 nm 1.2 V CMOS technology with an on-chip spiral inductor and an integrated MIMcap. This circuit

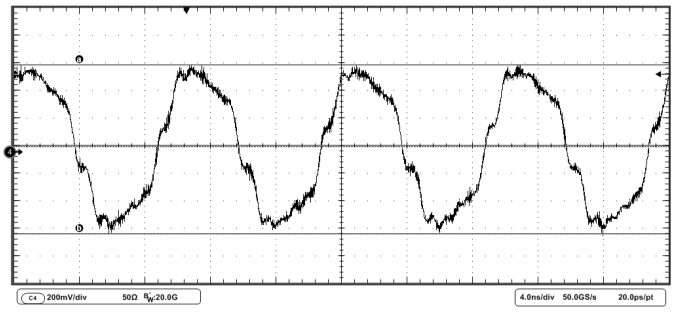


Fig. 7. Measured output voltage waveform at 100 MHz for a 25 Ω load.

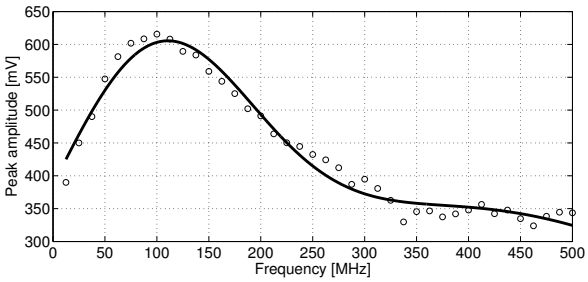


Fig. 8. Peak output amplitude as a function of switching frequency.

TABLE I

Summary of the measurement results

Reference	[4]	this work
Process (μm)	1.2 μm	0.13 μm
Input voltage	2 V	1.2 V
Maximum output peak amplitude	320 mV	600 mV
Maximum efficiency	48 %	65.2 %
Power at maximum efficiency	6.4 mW	6.9 mW
Switching frequency	500 MHz	100 MHz
Maximum output power @ efficiency	not available	11.6 mW @ 47 %
Notes	simulation only	fully-integrated

is intended for a resonant class DE DC-DC converter. The inherent soft switching yields high conversion efficiency at high switching frequencies. The use of on-chip passives reduces the bill of materials considerably. A maximum output power of 11.6 mW is achieved and a maximum efficiency of 65.2 % without the need for external components. The output voltage peak amplitude lies around 600 mV at a switching frequency of 100 MHz. These results confirm and improve previous simulations.

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