A 186 to 212 GHz Downconverter in 90 nm CMOS

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Abstract The design and measurements of a 200 GHz downconverter in 90 nm standard CMOS are presented. A positive conversion gain of +6.6 dB, a noise figure of 29.9 dB and an output bandwidth of 3 GHz are measured for an LO power of −14.9 dBm. The conversion gain remains within 3 dB for an RF frequency between 186 and 212 GHz. Downconversion of BPSK and QPSK signals is demonstrated with eye diagrams and constellation plots with data rates over 4 Gbit/s. A mathematical analysis is made of the MOSFETs in the triode region and a new small-signal parameter κ is introduced, which enables the design of the mixing transistors for minimum conversion loss.

Keywords Millimeter wave · Terahertz · Data communication · BPSK · QPSK · Receivers · CMOS · MOSFET-C · Mixers

1 Introduction

Thanks to the high level of integration, CMOS is the preferred technology for high volume and low-cost consumer market applications. That is the main motivation for research on millimeter wave and terahertz circuits in CMOS, even though CMOS provides a lower performance compared to SiGe and the III-V compound semiconductors when it comes to high frequency operation.

Besides circuits in III–V [1], [2] and SiGe [3], several publications have presented circuits in CMOS [4–10], working in the millimeter wave range, with possible applications in imaging, radar and high speed data communication [11]. This work pushes the frequency boundary even further by demonstrating the first CMOS chip capable of receiving Gbit/s signals at 200 GHz [4].

The paper is structured as follows: Section 2 starts with identifying the main design goals and an in-depth noise analysis of the system. Then a thorough analysis of the MOSFET in the linear region and its operation as a linear mixer follows, which allows to choose the

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design parameters for minimum noise figure. Next, the design of the 200 GHz transformers and of the baseband circuitry are discussed. Measurement results are given in Section 3, starting with important performance metrics and proceeding with a demonstration of Gbit/s BPSK and QPSK downconversion. Section 4 concludes the paper with a comparison to other publications and a summary.

2 Circuit architecture and design

The architecture of the complete downconverter chip is shown in Fig. 1. The core of the circuit is an active MOSFET-C downconverter [12], consisting of four mixing transistors and a transimpedance amplifier (TIA). To achieve mixing behavior at 200 GHz, the MOSFETs are used as variable resistors. They are biased in the linear region ($V_{DS}=0$) and are arranged as a double balanced structure. The LO is applied to the drains and the RF is applied to the gates. This way, a parasitic baseband signal is avoided in the presence of mismatch [12]. The gate voltage varies the MOSFET's channel resistance, resulting in a current which is proportional to the product of the LO and the RF voltages, as can be seen from the well known equation for a MOSFET in the linear region:

$$i_{DS} = \mu C_{ox} \frac{W}{L} \left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] \quad (1)$$

The double balanced structure cancels the unwanted mixing products, while the input capacitance of the TIA (explicitly shown in Fig. 1) acts as an RF short so that only the IF signal remains [12].

The gain stages behind the TIA amplify the IF voltage and the buffers are implemented as source followers to drive the external load.

Fig. 1 Circuit diagram of the complete 200 GHz downconverter chip.

2.1 Design goals

The $f_{\max}$ of the devices in the 90 nm process is just slightly above 200 GHz. It is therefore impossible to put an LNA in front of the mixer. In a conventional receiver, the mixer's noise figure is suppressed by the gain of the LNA so that the receiver noise figure is mainly determined by the LNA performance. In this design however, the system noise figure is determined by the mixer's noise figure. Hence, the goal is to minimize the mixer's noise figure and this automatically means minimizing its conversion loss.

To boost the downconverted signals for measurement, voltage gain stages are added, with a total gain of 20 dB. These are designed for maximum bandwidth (simulated 8 GHz), in order to demonstrate Gbit/s data communication at 200 GHz.

Of equal importance is the use of a low LO power, considering the difficulty to generate high LO amplitudes at these frequencies. Therefore, the LO power is minimized during the design of the mixer.

2.2 Noise analysis

Figure 2 shows the downconverter as a cascaded system of the mixing transistors, followed by the TIA, the voltage amplifiers and the source followers. The Friis equation [13] can be used to analyze the contribution of the different blocks to the system noise figure. Let G_{mix} (<1) and F_{mix} be the available power conversion gain and noise factor of the mixing transistors. G_{TIA} and F_{TIA} are the available power gain and noise factor of the transimpedance amplifier. G_V and F_V are the available power gain and noise factor of the voltage gain stage and the source followers combined. Referring to Fig. 2, let P_{RF} be the available signal power presented to the RF input of the downconverter. $P_{\text{n,RF}}$ is the available noise power from the RF source: $P_{\text{n,RF}} = kTB$. At the output of the mixing quad, P_{IF} is the available signal power at the IF frequency and $P_{\text{n,IF}}$ is the available noise power. $P_{\text{n,IF}}$ is the sum of the attenuated input noise ($P_{\text{n,RF}} G_{\text{mix}}$) and the noise generated within the circuit. Since the attenuation of the mixing quad is large ($G_{\text{mix}} \approx -30$ dB), the contribution of $P_{\text{n,RF}}$ can be neglected and only the noise from the mixing transistors plays a role. This is again just thermal noise. There is no $1/f$ -noise since $V_{\text{DS}} = 0$ so $P_{\text{n,IF}} = kTB$. For the noise factor of the mixing quad, this results in:

$$F_{\text{mix}} = \frac{\text{SNR}_{\text{RF}}}{\text{SNR}_{\text{IF}}} = \frac{P_{\text{RF}}}{P_{\text{IF}}} = \frac{1}{G_{\text{mix}}} \quad (2)$$

The noise factor of the complete system is then [13]:

$$F = \frac{1}{G_{\text{mix}}} + \frac{F_{\text{TIA}} - 1}{G_{\text{mix}}} + \frac{F_V - 1}{G_{\text{mix}} G_{\text{TIA}}} \quad (3)$$

Fig. 2 The downconverter as a cascade of different blocks. All indicated powers are available powers.

From this equation, the importance of a low $1/G_{\text{mix}}$ becomes evident. Not only does it directly contribute to the total noise figure, it also amplifies the noise figure of the subsequent stages. As an example, Table 1 shows the contributions of the different blocks to the total noise figure with realistic values from simulations. The noise figures are determined at baseband (0–3 GHz). This example stresses the importance of a low conversion loss in the mixing transistors and a low noise figure of the TIA.

Noise simulations are performed on the final design. Figure 3 shows the contributions of the different blocks to the input referred noise power spectral density. It's clearly seen that the $1/f$ -noise is caused by the TIA and that beyond the $1/f$ corner (≈ 10 MHz), both the mixing MOSFETs and the TIA contribute significantly.

2.3 Analysis and design of the mixing MOSFETs

The four mixing transistors are designed for maximum G_{mix} and minimum LO power. In this subsection, the influences of the device size and the gate bias voltage are analyzed. After choosing $V_{\text{DS}}=0$ and a minimal gate length $L=90$ nm, the only design parameters left are the gate width W and the gate bias voltage V_{GS} .

The mixing behavior of the MOSFET in the linear region comes from the modulation of the channel conductance by the gate voltage, resulting in a linear multiplication of the small signal drain-source and the gate-source voltages.

As indicated in Fig. 4a, v_{rf} is the differential voltage at the gates and v_{lo} the differential voltage at the drains (V_{RF} and V_{LO} in the frequency domain). The internal voltages in the transistors can be written in the frequency domain as:

$$V_{\text{gs}} = \pm \frac{1}{2} \frac{1}{(1 + j2\pi f_{\text{RF}} R_{\text{g}} C_{\text{g}})} V_{\text{RF}} \quad (4)$$

$$V_{\text{ds}} = \pm \frac{1}{2} V_{\text{LO}} \quad (5)$$

Where R_{g} is the gate resistance and C_{g} is the gate capacitance of one transistor. The drain and source contact resistances are neglected.

In the time domain, the internal gate-source voltage is denoted by $v_{\text{GS}}=V_{\text{GS}}+v_{\text{gs}}$, the drain-source voltage is $v_{\text{DS}}=V_{\text{DS}}+v_{\text{ds}}$ and $i_{\text{DS}}=I_{\text{DS}}+i_{\text{ds}}$ is the total channel current. We will now write the channel current of the MOSFET as a general function of v_{GS} and v_{DS} . By definition:

$$g_m \equiv \frac{\partial i_{\text{DS}}}{\partial v_{\text{GS}}} \quad (6)$$

$$g_{\text{ds}} \equiv \frac{\partial i_{\text{DS}}}{\partial v_{\text{DS}}} \quad (7)$$

Table 1 Contribution of different blocks to the total NF.

Block	NF (dB)	F	G_{A}	Contribution to noise figure in (3)
Mixing quad	30	1000	−30	1000
TIA	2	1.6	20	600
V-gain+Buffer	6	4	/	30
Total	32.1	1630	/	/

Fig. 3 Simulation of input referred noise PSD, showing contributions from different blocks. The mixing quad and the TIA are the main contributors to the noise.

Fig. 4 (a) Double balanced mixing transistors and (b) AC equivalent at RF and IF frequencies.

The channel conductance g_{ds} is modulated by v_{GS} . A Taylor expansion on $i_{DS}(v_{GS}, v_{DS})$ around the DC point (V_{GS} , V_{DS}) gives:

$$i_{DS} \simeq I_{DS} + g_m v_{gs} + g_{ds} v_{ds} + \frac{1}{2} v_{gs}^2 \frac{\partial g_m}{\partial v_{GS}} + v_{gs} v_{ds} \frac{\partial g_{ds}}{\partial v_{GS}} + \frac{1}{2} v_{ds}^2 \frac{\partial g_{ds}}{\partial v_{DS}} \quad (8)$$

By arranging the MOSFETs in a double-balanced configuration and summing the currents of the four transistors, all unwanted terms cancel and only the $v_{gs}v_{ds}$ term of each transistor remains.

Since v_{gs} and v_{ds} are related to v_{rf} and v_{lo} through (4) and (5), the short circuit current i_{sc} in Fig. 4a is proportional to the product of the RF and LO voltages. This current contains a sum frequency and a difference frequency, so let i_{if} be the difference frequency component of i_{sc} . As will be seen later on, the low pass behavior at the gate has the same cut off frequency for any value of W , and the influence of V_{GS} on the gate impedance is negligible. That means that the ratio between V_{RF} and V_{gs} does not vary with W or V_{GS} , so it is convenient to write:

$$|I_{IF}| \propto \kappa |V_{RF}| |V_{LO}| \quad (9)$$

With

$$\kappa \equiv \frac{\partial g_{ds}}{\partial v_{GS}} \quad (10)$$

κ is the sensitivity of g_{ds} with respect to v_{GS} .

Each factor in (9) is a function of W and V_{GS} . Since we are interested in the available power conversion gain, we need to know the available output power, which is determined by I_{IF} and the output conductance. The output conductance of the mixing quad is equal to the small-signal output conductance of one transistor, g_{ds} . The capacitive part of the output admittance can be neglected at the IF frequency. While g_{ds} is around 1 mS to 100 mS, depending on the size and on V_{GS} , the drain-source capacitance is around 1 fF to 10 fF. This results in a susceptance of 6 μ S to 60 μ S at 1 GHz.

Then the available IF power from the mixing transistors is:

$$P_{IF} = \frac{|I_{IF}|^2}{8g_{ds}} \propto (\kappa |V_{RF}| |V_{LO}|)^2 \frac{1}{g_{ds}} \quad (11)$$

Figure 4b shows the AC equivalent circuit for the mixing transistors. V_{LO} and V_{RF} are the small signal drain and gate voltages at $f_{RF}=200$ GHz. Z_g and Z_d are the impedances at the gates and drains. They are equal to the gate and drain impedance of one transistor. The output is specified at the difference frequency f_{IF} .

Formulas (6) to (11) can be made concrete using the transistor equations for the linear region in weak inversion and strong inversion [14].

In strong inversion:

$$i_{DS} = \mu C_{ox} \frac{W}{L} \left[(v_{GS} - V_T) v_{DS} - \frac{v_{DS}^2}{2} \right] \quad (12)$$

$$g_{ds} \simeq \mu C_{ox} \frac{W}{L} (v_{GS} - V_T) \quad (13)$$

$$\kappa = \mu C_{ox} \frac{W}{L} \quad (14)$$

In weak inversion:

$$i_{DS} = \frac{W}{L} I'_M e^{(v_{GS}-V_M)/n\phi_t} (1 - e^{-v_{DS}/\phi_t}) \quad (15)$$

$$g_{ds} = \frac{W}{L} I'_M e^{(v_{GS}-V_M)/n\phi_t} e^{-v_{DS}/\phi_t} \quad (16)$$

$$\kappa = \frac{W}{L} \frac{1}{n\phi_t} I'_M e^{(v_{GS}-V_M)/n\phi_t} e^{-v_{DS}/\phi_t} \quad (17)$$

In these equations, $\phi_t = kT/q$. The quantities I'_M , V_M and n are functions of technology related parameters and the constant source-bulk voltage, as defined in [14] and can be considered as constants in this analysis. Which one of these sets of equations is applicable, depends on V_{GS} . In Fig. 5, i_{DS} , g_{ds} and κ of the same transistor are shown versus V_{GS} . The transition between the two regions can be clearly seen. The effect of mobility degradation at large gate bias is seen in the lower graph.

Equation (11) expresses P_{IF} in terms of the RF and LO voltages. In order to analyze the conversion loss and noise figure, the analysis must be made in terms of powers. Therefore, P_{IF} is maximized for constant P_{RF} and P_{LO} . First, V_{RF} and V_{LO} are expressed in terms of P_{RF} , Z_g and P_{LO} , Z_d . For this analysis, it is assumed that the impedances of the RF and LO sources are perfectly matched to the mixer inputs. In reality, the matching will not be perfect and the matching network will introduce extra losses. This effect will be taken into account in section 2.4.

Fig. 5 $\log(I_{DS})$, g_{ds} , and $\kappa = \partial g_{ds} / \partial v_{GS}$ versus V_{GS} for $V_{DS}=0$ V. The transition between weak and strong inversion occurs at $V_{GS}=0.4$ V. Mobility degradation is observed for larger V_{GS} .

When a power P is dissipated in the real part of an impedance $Z=R+jX$, the voltage across the impedance is:

$$|V| = \sqrt{\frac{2P \cdot |Z|^2}{R}} \quad (18)$$

Which is true for both the RF and the LO voltage. This basically means that if the real part of the gate and drain impedance is small compared to the total impedance, for the same LO and RF power, a higher IF power can be achieved. We are now ready to analyze the effect of gate width and V_{GS} on the available conversion gain G_{mix} , for a fixed LO power.

2.3.1 Influence of gate width W

From equation (9), with (14) and (17), it is expected that the IF current will benefit from bigger transistors. But for constant power, V_{RF} and V_{LO} decrease with increasing W because Z_g and Z_d are inversely proportional to W . Simulations with RF models are shown in Fig. 6. Note that both the real parts and the imaginary parts scale linearly with $1/W$, thus justifying the claim that $R_g C_g$ in (4) does not vary with W . Then from (18):

$$|V_{RF}| \propto \sqrt{\frac{P_{RF}}{W}}; |V_{LO}| \propto \sqrt{\frac{P_{LO}}{W}} \quad (19)$$

Inserting this into equation (9) and knowing that $\kappa \propto W$, it follows that I_{IF} is independent of W , for fixed P_{RF} and P_{LO} . Equations (13) and (16) however, show that the output conductance is proportional to the device width. This is also shown in Fig. 6.

The conclusion from equation (11) is then that the available IF power is inversely proportional to the device width. Note that this result does not depend on whether the transistors are operated in weak or in strong inversion.

Simulations were performed in which $P_{RF}=-20$ dBm and $P_{LO}=-20$ dBm were held constant, being the actual powers flowing into the gates and drains, respectively. The total gate width was changed. The expected $P_{IF} \sim 1/W$ behavior is shown in Fig. 7. It should then be concluded that small transistors give more available output power.

Fig. 6 Real and imaginary parts of the gate ($Z_g=R_g+jX_g$) and drain ($Z_d=R_d+jX_d$) impedances at 200 GHz and g_{ds} versus W of the mixing transistors. $V_{GS}=0.4$ V and $L=90$ nm. Simulations on RF models.

Fig. 7 Simulated available IF output power of mixing transistors in function of gate width with $P_{RF} = -20$ dBm and $P_{LO} = -20$ dBm, the power flowing into the gates and the drains.

Very small transistors are not practical however. Figure 8 shows the drain and gate impedance on a $50\ \Omega$ Smith chart. For very small transistors, in the high impedance region, the points are close to the edge of the Smith chart. These impedances will result in more power loss, as will be explained in section 2.4. For this reason, the gate width is chosen to be $6\ \mu\text{m}$.

2.3.2 Influence of V_{GS}

The DC gate voltage works in three ways. First, it directly affects g_{ds} , as can be seen from (13) and (16): small V_{GS} gives higher output resistance. Second, it has an influence on the impedances Z_g and Z_d . The effect on the gate impedance is negligible, but the drain impedance is largely determined by g_{ds} thus affecting V_{LO} . Third, κ is a strong function of V_{GS} . The different factors that determine P_{IF} as in (11) are drawn in Fig. 9, normalized and on a decibel scale in order to compare their effects. From this graph, it is clear that it's mainly κ and the output resistance that determine the behavior in function of V_{GS} and that $V_{GS} \approx 330$ mV is the optimum. An important conclusion is that best mixing performance is achieved by operating the MOSFET in weak inversion.

Fig. 8 Z_g and Z_d for $W = 2 \rightarrow 32\ \mu\text{m}$ (steps of $2\ \mu\text{m}$). $V_{GS} = 0.4$ V and $L = 90$ nm.

Fig. 9 Influence of V_{GS} on the different factors in (11). P_{IF} reaches a maximum for $V_{GS}=0.33$ V.

2.3.3 Layout of mixing transistors

The transistors are implemented with 6 fingers of $1\ \mu\text{m}$ each, to reduce gate resistance. In drawing the layout for the mixing transistors and the surrounding connections to the transformers, symmetry is very important in order to maintain balanced differential signals. Furthermore, a lot of care is taken to minimize resistive losses, since every dB of loss adds directly to the noise figure. For accurate knowledge of the loss and Z_g and Z_d , a parasitic extraction is done for the mixing quad and finite element simulations in Momentum are performed for the connection structures around it.

2.4 Transformer design

The transformers at the RF and LO inputs have three important functions [9]. First, they act as baluns, making a balanced signal from the single-ended signal from the probe. Second, they allow to bring the desired DC voltage on the gates and the drains of the mixing transistors, through the common-mode point in the secondary inductor. Third, they can be used to provide a power match between the $50\ \Omega$ probes (source impedance for the transformer) and Z_d and Z_g (load impedance of the transformer).

Figure 10 shows the layout of the transformers. They consist of a single turn in the primary and secondary coil. The traces are made in the top metal, because it has lowest

Fig. 10 Layout of the transformers.

resistivity and least capacitive coupling to the substrate. The design parameters are the diameters and trace widths of both inductors, which affect the resistive loss, the self resonance frequency and the leakage inductance [15]. When looking at the two port parameters of the transformer, the minimum loss of the transformer is expressed by G_{MAX} . Through careful design, $G_{MAX} > -1$ dB can be achieved at 200 GHz.

The leakage inductance of the transformer can be used to tune out the capacitive part of the transistor impedances. In this way, a simultaneous conjugate match between the input and output of the transformer can be made. Because of the bilateral nature of the transformer ($s_{12} = s_{21}$), there is only one combination of source and load impedance that can lead to a simultaneous conjugate match. It is nearly impossible to design a transformer for which these impedances correspond exactly to the transistor impedance and the $50\ \Omega$ source impedance. The design of the transformers is based on the operating gain (G_P) and available gain (G_A) circles of the transformers. The G_P circles indicate how load mismatch affects the loss compared to G_{MAX} , assuming a perfect match at the input. Similarly, the G_A circles indicate how source mismatch affects the loss compared to G_{MAX} , assuming a perfect match at the output.

Then, a transformer is designed with sufficiently high G_{MAX} and for which the $G_P = -1$ dB circle encloses the load impedance (Z_d or Z_g) and the $G_P = -1$ dB circle encloses $50\ \Omega$. In Fig. 11, the G_P and G_A circles of -0.75 dB and -1 dB are drawn for the transformer at the gates of the mixing transistors. The gate impedance that is drawn here, is from simulations with parasitic extraction of the transistors and Momentum simulations of the connection structures. The impedances fall just outside the -1 dB circles, resulting in $s_{11} = -7.7$ dB with a $50\ \Omega$ reference. The ratio of power delivered to the gates to the available RF power (defined as the transducer gain) is simulated to be $G_T = -1.1$ dB. Similarly, the transformer at the drain side leads to $s_{11} = -5.1$ dB and $G_T = -2.7$ dB.

Note that the G_P and G_A circles lie closer and closer together when approaching the edge of the Smith chart, as can be seen on Fig. 11. Load impedances (Z_d or Z_g) in this region of the Smith chart are more likely to fall outside the lower loss circles. In this design, it has not been possible to design transformers that provide a good match between the smallest transistors ($W = 2 \rightarrow 4\ \mu\text{m}$) and $50\ \Omega$. Choosing $W = 6\ \mu\text{m}$ is the best compromise between optimal G_{mix} and matching. The transformers in the final lay-out have the following sizes: for the transformer at the gate, the diameter of the inner turn is $36\ \mu\text{m}$ and of the outer turn $48\ \mu\text{m}$. For the transformer at the drain, the diameter of the inner turn is $46\ \mu\text{m}$ and of the outer turn $60\ \mu\text{m}$.

Fig. 11 G_P and G_A circles of the transformer at the gate. The source and load impedances fall just outside the -1 dB circles.

Fig. 12 Chip micrograph with indication of the active area.

2.5 Baseband circuits

The transimpedance amplifier converts the IF current from the mixing quad into a differential voltage, which is then amplified by additional gain stages. Source followers finally drive the off chip $50\ \Omega$ load. The TIA consists of a cascade of two voltage amplifiers with feedback resistors R_f . The schematic of these amplifiers is shown in Fig. 1. The pMOSTs have their gates connected to ground and serve as load resistors. The design of the voltage amplifiers and the number of cascaded stages is a trade-off between gain and bandwidth [16]. In the final design, a single voltage amplifier has a gain of 10 dB and a bandwidth of 8 GHz. For the design of the TIA, loop stability has to be taken into consideration and as explained in section 2.2, the noise figure must be minimized. Taking $R_f = 1\ \text{k}\Omega$ and using two voltage amplifiers gives the best trade-off between transimpedance, bandwidth, stability and noise.

Parasitic extractions were performed for all baseband circuits in order to minimize the effect of parasitics on gain and bandwidth.

2.6 Biasing of mixing transistors and TIA

Since for the mixing transistors, $V_{DS} = 0$, the gates of the input pair of the TIA can be biased by applying the wanted DC voltage to the drains of the mixing transistors. This voltage V_{DC} is applied to the common mode point on the secondary turn of the transformer. The TIA is designed

Fig. 13 Photograph of the measurement setup for the IC on an FR-4 PCB on the probe station.

Fig. 14 The measured conversion gain increases linearly with P_{LO} . The LO 1 dB compression point is -15.6 dBm.

in such a way that the DC voltage at its output is also V_{DC} and no DC current flows through the feedback resistors. In order to avoid the bulk effect in the mixing quad, these transistors are laid out in a triple well structure, so that their body voltage can be set to V_{DC} independently from the rest of the chip. This technique avoids the use of complicated biasing circuits.

2.7 Layout

The downconverter is fabricated in a 90 nm standard CMOS process. The total chip area is 0.375 mm^2 , including bond pads, probe pads and decoupling capacitors. The active area as indicated in Fig. 12 is only 0.04 mm^2 . The rest of the area is occupied by decoupling capacitors for the DC lines and ESD protection devices.

3 Measurements

For measurements, the chip is glued to an FR-4 PCB. The 200 GHz LO and RF signals are generated by millimeter wave source modules and applied to the chip through G-band waveguide probes. The IF output is brought off-chip through bondwires, connected to a differential transmission line on PCB. The measurement setup on the probe station is shown in Fig. 13.

The total power consumption of the downconverter chip is 63.3 mW from a 1.2 V supply.

Fig. 15 Measurement and simulation of P_{IF} and IM_3 versus P_{RF} with indication of $IIP_3 = -5.4$ dBm.

Fig. 16 The measured IF output bandwidth is 3 GHz. This includes also the effects of the bondwires and the PCB. The simulated bandwidth of the chip alone is 6.4 GHz.

3.1 Performance metrics

For an LO with a frequency of 200 GHz and a power of -14.9 dBm and an RF with a frequency of 200.5 GHz and a power of -16.6 dBm, the 500 MHz IF is measured with a power of -10.0 dBm. The conversion gain is thus $+6.6$ dB. Figure 14 shows that the conversion gain varies linearly with the applied LO power, demonstrating the linear multiplication in the MOSFET-C mixer. The 1 dB compression point for the LO power is measured to be -15.6 dBm.

Linearity is evaluated by measuring the first harmonic (P_{IF}) at 500 MHz and the third harmonic (P_3) at 1.5 GHz at the output, while increasing the RF power. A two-tone test could not be performed. However, the third order intermodulation product (IM_3) can be calculated from P_3 through the equation: $IM_3 = P_3 + 9.54$ dB [17]. Figure 15 shows measured P_{IF} and IM_3 . The input third order intermodulation intercept point is $IIP_3 = -5.4$ dBm. Simulations are added for comparison.

The IF output bandwidth is measured by changing f_{RF} while keeping f_{LO} fixed at 200 GHz. Figure 16 shows that the IF bandwidth is 3 GHz. The bandwidth is limited by the baseband circuits, the bondwires and the transmission line on FR-4. The simulated IF bandwidth of the chip is 6.4 GHz.

The LO frequency can be swept along with the RF frequency from 186 GHz to 212 GHz while the conversion gain stays within 4.5 dB to 7.5 dB. This is shown in Fig. 17. Thanks to the wideband 200 GHz transformers, the circuit can operate in an RF range of 26 GHz.

Fig. 17 The measured conversion gain is between 4.5 dB and 7.5 dB for LO frequencies between 186 and 212 GHz. The IF frequency is 500 MHz.

Fig. 18 The measured and simulated output noise density. The 1/f noise corner is around 10 MHz, the average noise level in a band from 10 kHz to 3 GHz is -137.5 dBm/Hz.

The output noise measurement is shown in Fig. 18. The measurements are performed with a spectrum analyzer, using noise markers. This way, the output noise power is measured taking into account the resolution bandwidth and with corrections for the spectrum analyzer's log amplifier and detector. The 'average' function is used in order to come to a more accurate result. In the white noise region, the resolution bandwidth can be chosen up to 10 MHz, but in the pink noise region, the resolution bandwidth must be chosen small enough to capture the variation of the noise over frequency.

The simulations are also added for comparison. It is observed that the noise analysis of section 2.2 gives a good match to the measurements. The average noise level in a band from 10 kHz to 3 GHz is -137.5 dBm/Hz. The 1/f noise corner frequency is around 10 MHz. Compared to the 3 GHz bandwidth, the 1/f noise can be neglected. From the integrated noise, the noise figure can be calculated:

$$NF = 10 \times \log\left(\frac{N_o}{kTB}\right) = 29.9\text{dB} \quad (20)$$

Where N_o is the integrated output noise power in the band, calculated from the measured data. G is the measured conversion gain and kTB is the available input noise power. This is a

Fig. 19 Setup for the generation of 200 GHz phase or frequency modulated signals [18].

Fig. 20 Measured eye diagrams for BPSK with data rates of 2 Gbit/s (**a**) and 4 Gbit/s (**b**), downconverted to baseband.

single sideband (SSB) noise figure since it assumes a signal on one side of the LO frequency only. This noise figure is comparable to a MOSFET-C downconverter working at 1.5 GHz [12].

3.2 Modulated signals

As a demonstration of the IC's high-speed data communication capability at millimeter wave frequencies, a test setup was conceived to generate 200 GHz BPSK and QPSK modulated signals to apply to the RF input [18]. It consists of an IQ modulator made out of discrete microwave components, followed by an OML source module (frequency multiplier with a multiplication factor of 12), as shown in Fig. 19.

The output is measured with a Tektronix DPO72004B oscilloscope with a 20 GHz bandwidth. By choosing $f_{\text{RF}} = f_{\text{LO}}$, the downconverted BPSK signal can be visualized on the oscilloscope as an eye-diagram. This is shown in Fig. 20. For $f_{\text{RF}} \neq f_{\text{LO}}$, the IF signal can be demodulated in the oscilloscope, producing constellation diagrams as shown in Fig. 21.

Fig. 21 Measured downconverted constellation diagrams for BPSK with data rate of 2 Gbit/s (**a**) and QPSK with data rate of 2 Gbit/s (**b**), at different IF frequencies.

Table 2 Performance summary and comparison to other work.

Reference	Blocks	Process	RF (GHz)	IF (MHz)	Conv. Gain (dB)	NF (dB)	P _{LO} (dBm)
[3]	LNA+Mixer	0.13 μm SiGe HBT	202–230	–	+18	13 DSB	0 (110 GHz)
[2]	LNA+Mixer	0.1 μm GaAs mHEMT	210–225	2000	+2	8.4 DSB	–
[19]	Active Mixer	45 nm SOI CMOS	130–185	–	–12	–	+2.8
[19]	Passive Mixer	45 nm SOI CMOS	145–161	–	–4	–	+2.8
[7]	Mixer	65 nm CMOS	102	2000	–4	22	+1
[10]	Mixer	0.25 μm CMOS	650	0–1.6	–	68 SSB	–32.5
This Work	Mixer	90 nm CMOS	186–212	0–3000	+6.6	29.9 SSB	–14.9

The downconversion of 200 GHz phase modulated signals with data rates up to 4 Gbit/s is thus demonstrated with good eye patterns.

4 Conclusion

This paper presents a CMOS downconverter working between 186 and 212 GHz, with a conversion gain of +6.6 dB, a noise figure of 29.9 dB and an IIP_3 of -5.4 dBm, for an LO power of -14.9 dBm at 200 GHz. The output bandwidth is 3 GHz, allowing downconversion of high data rate phase modulated signals as demonstrated up to 4 Gbit/s.

A mathematical analysis is made of the 200 GHz mixing MOSFETs in the linear region. A new small signal parameter κ is introduced, which is the sensitivity of the channel conductance with respect to the gate voltage. This analysis reveals that for best performance, the MOSFETs are operated in weak inversion and that small devices provide lower conversion loss and noise figure.

In Table 2, this work is compared to other publications of receivers and mixers above 100 GHz, in various technologies. This work is the first silicon based receiver able to achieve Gbit/s data rates at 200 GHz or higher. It proves that CMOS, despite its speed limitations, is a viable candidate for integrated circuits at millimeter wave and even terahertz frequencies.

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