Design and Assessment of a 6 ps-Resolution Time-to-Digital Converter With 5 MGy Gamma-Dose Tolerance for LIDAR Application

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Abstract—Time-to-Digital Converters (TDCs) are key building blocks in time-based mixed-signal systems, used for the digitization of analog signals in time domain. A short survey on state-of-the-art TDCs is given. A novel multi-stage noise-shaping (MASH) delta-sigma ($\Delta\Sigma$) TDC structure is proposed for applications in continuous-time pulsed time-of-flight (TOF) rangefinders for nuclear reactor remote sensing, which requires both high resolution and multi MGy gamma-dose radiation tolerance. The converter, implemented in 0.13 μm , achieves a time resolution of 5.6 ps and an ENOB of 11 bits, when the oversampling ratio (OSR) is 250. The TDC core consumes only 1.7 mW and occupies an area of 0.11 mm². Owing to the usage of circuit level radiation hardened-by-design techniques, such as passive RC oscillators and constant- g_m biasing, the TDC exhibits enhanced radiation tolerance. At a low dose rate of 1.2 kGy/h, the frequency of the counting clock in the TDC remains constant up to at least 160 kGy. Even after a total dose of 3.4 MGy at a high dose rate of 30 kGy/h, the TDC still achieves a time resolution of 10.5 ps with an OSR of 250.

Index Terms—CMOS, delta-sigma, gamma-dose radiation, MASH, noise-shaping, time-to-digital converter (TDC), total ionizing dose (TID).

I. INTRODUCTION

HIGH resolution time-to-digital converters (TDCs) are highly demanded in digital PLLs, ADCs, and time-of-flight (TOF) measurement units, which are widely used for nuclear instrumentation. Demonstrating applications can be found in an accelerator driven system (ADS) like the multi-purpose hybrid research reactor for high-tech applications (MYRRHA): in the spallation target the position of the liquid lead-bismuth free surface needs to be monitored by a laser

detection and ranging (LIDAR) system. Pulsed LIDAR systems are widely used in a variety of remote sensing applications, including marine, space target tracking, and safety control of nuclear reactors. A standard LIDAR system consists of a laser transmitter, two receiver frontend channels and a TDC [1]. The TDC compares the time difference between an emitted laser pulse and the reflected signal. The distance from the LIDAR detector to the object can be determined based on the TOF theory. In order to be able to sense a distance difference of 1 mm, a TDC with a time resolution of 6.7 ps is required.

Conventional TDCs were built based on the CMOS gate-delay-line structure, whose resolution is determined by the intrinsic delay of a CMOS inverter gate. As a mainstream integrated circuit fabricating process, commercial CMOS technology has been successfully implemented under ionizing radiation up to 1 MGy, by laying out the NMOS transistors in enclosed geometry [2]. Recent research also shows a trend in advanced CMOS technologies toward increased total dose hardness, due to downscaling of the CMOS gate oxide thickness [3]. This makes modern deep-submicron CMOS technology more suitable for radiation tolerant design. However, for upcoming applications in the International Thermonuclear Experimental Reactor (ITER), electronic components are required to stand for higher than 5 MGy total dose radiation level [4], where the delay of a transistor undergo dramatic changes (on the scale of picoseconds) [5]. In this case, special precautions need to be taken on both system and layout level to secure the circuit's performance.

Previous efforts have successfully implemented a laser driver [6] and a transimpedance amplifier (TIA) [7] in CMOS technology with high radiation tolerance, which could partially form a radiation hardened integrated LIDAR system apart from the absence of a high resolution TDC. This work presents a radiation tolerant multi-stage noise-shaping (MASH) delta-sigma ($\Delta\Sigma$) TDC. It adopts the noise-shaping concept, which can improve the effective resolution of a coarse quantizer, but requires no precisely matching analog components. The MASH TDC employs a low counting clock (55 MHz) to achieve better than 10 ps time resolution, by shaping the quantization noise out from the interested baseband to high frequency. The on-chip generated counting clock has a frequency depending primarily on passive components, which shows intrinsic process, voltage, temperature (PVT) stability and radiation tolerance. Moreover, on the layout level, guard-rings are extensively used for all NMOS and PMOS cells to prevent single event latchup (SEL). The only

Manuscript received October 10, 2011; revised February 27, 2012; accepted March 30, 2012. Date of publication May 16, 2012; date of current version August 14, 2012. This work was carried out at the ESAT-MICAS laboratory, Katholieke Universiteit Leuven, and supported by SCKCEN, the Belgian Nuclear Research Centre.

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TNS.2012.2193598

drawback of the $\Delta\Sigma$ TDC is that it requires a repeated measurement at a sampling rate, a few orders above the signal frequency. Therefore, it can not be directly used for applications which require a fast single-shot measurement, like the High Energy Physics (HEP) experiment at CERN: ALICE. Unless an additional sample-and-hold circuit is added at the front of the TDC, it preserves the time information obtained from the single-shot measurement, and keeps it for the later time signal processing. However, for other remote sensing applications including the LIDAR, multi-shot measurement can be easily performed and it helps the TDC to achieve excellent time resolution at the cost of measurement time.

The remainder of this paper is organized as follows. First, a brief review on existing TDCs is given in Section II. Section III explains the proposed MASH TDC in detail. In Section IV the Pre-Rad measurement results are shown. Section V discusses the radiation assessment results at both low (1.2 kGy/h) and high (30 kGy/h) dose rate. A conclusion is drawn in Section VI.

II. A SHORT SURVEY ON TIME-TO-DIGITAL CONVERTERS

Quantizing the time interval between a start signal and a stop signal, and representing it as a digital code, is the basic task of a TDC. The early first TDCs were actually performed in two steps: time-to-voltage conversion (TVC), and then followed by voltage-to-digital conversion (VDC), as in [12], [13]. The time signal is mapped into an analog voltage in the first phase, by using a charge pump. The amplitude of the voltage corresponds to the width of the time frame. In the second step, this voltage is translated into a digital code by a conventional analog-to-digital converter (ADC). A 30 ps resolution is the best that has ever been reported based on this configuration [12]. The performance is mainly limited by the nonlinearity in the TVC unit and the resolution of the ADC. Moreover, as technologies scale down, this approach becomes less attractive. The strongly scaled supply voltage but relatively unchanged threshold voltage, raises significant challenges in the design of a high performance ADC, and restricts the input range of the TDC.

As opposed to the traditional analog method, a TDC could be also designed in time domain, where a circuit gains most profits from technology downscaling in terms of speed, power consumption and area. The simplest time domain TDC is a counter. By using a high-speed low-jitter reference clock, the counter can digitize a time signal with moderate resolution. However, when the requirement for the TDC resolution is increased to a few picoseconds, the reference clock frequency becomes unreasonably high (>100 GHz) with respect to power consumption and system complexity. Therefore, a real TDC employs phase-aligned parallel counting clocks to achieve high resolution rather than using one single external reference clock. A CMOS gate delay-line can serve this purpose. Many TDC architectures based on a delay-line core are reported in the last decade, and some achieve better than 10 ps resolution, as introduced in [8]–[11] and [14]–[17]. They can be summarized into following categories:

- Flash TDC [8], [9], [14]–[16],
- Pipeline TDC [10],
- Successive approximation TDC [17],
- Noise-shaping TDC [11].

Fig. 1. Basic structure of a delay-line based Flash TDC.

Fig. 2. Basic structure of a Vernier delay-line TDC.

Similar to their ADC counterparts, each type of TDC performs well in one area, e.g., resolution, bandwidth, robustness, or power consumption, and lacks in another, as will be discussed below.

A. Flash TDC

A Flash TDC uses a linear delay-cell ladder with a D flip-flop (DFF) at each rung of the ladder to compare the input time signal to successive reference time units [8], as shown in Fig. 1. A start signal propagates along the delay-line, and the state of each delay element is sampled on the rising edge of the stop signal. A thermometer code is then generated at the DFFs' output, which represents the time difference between the start and stop signal. The advantages of this circuit are obvious: It employs a very simple structure with only delay cells and DFFs. Hence, it is very area efficient. The resolution is determined by the intrinsic CMOS gate delay, which scales according to the technology scaling factor. But practically, the TDC resolution does not continue to improve with technology downscaling, due to the worsened mismatch problem between delay cells. Therefore, the finest achievable resolution of the basic delay-line TDC is limited to around 20 ps.

In order to obtain sub-gate-delay resolution, the Vernier method [9] is commonly used, as shown in Fig. 2. Instead of using only one delay chain, the Vernier TDC utilizes two independent delay lines on both start and stop signal paths to improve the time resolution. The delay elements on the stop path are designed slightly faster than those on the start path. Both start and stop signals propagate along two delay lines with an initial time difference of T_{in} . The conversion is completed only after the stop signal outruns the start signal. The resolution of the Vernier TDC is then given by $t_{Delay1} - t_{Delay2}$. However, along with the resolution, the sensitivity of the Vernier TDC to mismatch has also been amplified. Although calibration can be applied to compensate for this error [14], significant efforts are needed since each delay element in the TDC has to be corrected individually.

Fig. 3. Conceptual diagram of the TA-based Pipeline TDC.

Another technique to improve TDC resolution below that of a gate-delay is to subdivide the coarse time interval given by an inverter delay line. This concept can be realized by placing a resistor divider between two nodes of an inverter, as presented in [15]. The divider interpolates the input and output signals of the digital gate, and creates new intermediate signals which effectively divide the gate-delay into smaller intervals. The improvement in resolution for the interpolation architecture over the gate-delay is similar to that of the Vernier architecture, and is practically limited by the non-linear impedance of the delay elements during signal transients.

Since a Flash TDC works at the Nyquist conversion rate, a large signal bandwidth can be obtained. High resolution is achievable at the cost of increased power consumption and area penalty. In practice, the random variations among delay elements set up an upper bound for the resolution of a Flash TDC. To obtain well controlled delay cells, the basic delay-line core can be placed in a delay-locked-loop (DLL), as suggested in [16].

B. Pipeline TDC

It is well-known that, a Pipeline ADC uses two or more steps of subranging and residue amplification technique to achieve high resolution. The same idea can also be realized in the design of TDCs, with the help of a time amplifier (TA). Fig. 3 shows the conceptual diagram of a Pipeline TDC, which was proposed in [10]. First, the input time signal is digitized by a coarse Flash TDC. The conversion result is then converted back to a reference time and subtracted from the original input. The residue time is then applied to another Flash TDC after amplification. The effective resolution of the second Flash TDC is thereby improved by a factor of the gain of the TA. However, unlike voltage, the residue time cannot be stored unless it is transformed to other forms such as voltage or current. Therefore, in a Pipeline TDC, every possible time residue must be created and amplified separately. This significantly increases the system latency, and limits the input range of the TDC, since the linear working region of the TA is quite restricted. Moreover, the gain of the TA is also very sensitive to its working environment, mismatch and process variation.

Fig. 4. Signal flowchart of the successive approximation TDC.

C. Successive Approximation TDC

Successive approximation has been widely used in the design of ADCs to reach high resolution at the cost of conversion time. In the time domain, a successive approximation TDC [17] resolves the time difference between the start and stop signal one bit at a time in N cycles using binary search, as illustrated in Fig. 4. Due to the irretrievable nature of a time signal, the bidirectional adjustment required by the binary search is implemented by making both signal paths adjustable, rather than adjusting only one signal back and forth. The two delayed versions of input signals, $fb1$ and $fb2$, propagate cyclically in two separate loops formed by digital-to-time converters (DTCs), whose delays are controlled by the successive approximation register (SAR). At the beginning of the conversion, the DTC at the start path has a delay of $T_{REF}/2$. The relative timing of $fb1$ and $fb2$ is compared with a phase detector (PD) to determine which signal is lead. The SAR will adjust its value according the output of the PD. Whenever the signals $fb1$ and $fb2$ are aligned within one LSB, the conversion is complete. The fine resolution of the SAR TDC is obtained by interpolation. For an 8-bit operation, 128 unit interpolators (e.g. capacitors) are needed in one DTC, which occupies large area. In order to achieve wide input range, the SAR TDC has to be configured as a coarse-fine architecture, which has more severe matching problems and consumes more power.

D. Noise-Shaping TDC

For TDCs described above, they are all following the Nyquist criterion. The TDC resolution relies on either a minimized CMOS gate-delay or good matching between delay cells. Looking to the evolution of ADCs, the $\Delta\Sigma$ ADC achieves high resolution by noise-shaping, and it is insensitive to component mismatch. This makes the $\Delta\Sigma$ TDC a preferable choice for applications in radiation environment.

A Gated-Ring-Oscillator (GRO) TDC with first-order noise-shaping has been reported in [11]. In the GRO TDC, the input time signal is used to enable/disable a ring oscillator, as illustrated in Fig. 5. One single measurement is done by counting all the phase transitions in the oscillator during the enabling phase. The quantization error, which refers to the intermediate state of the oscillator, is preserved between measurements. This results in a first-order noise-shaping on the quantization noise. After digital low-pass filtering, the signal can be reconstructed with strongly reduced quantization error. The theory of time domain

Fig. 5. Basic structure of the GRO TDC.

noise-shaping will be discussed more in details in Section III. One issue in the GRO TDC, which could completely disrupt the noise-shaping behavior, is the existence of large skew error. Caused by charge redistribution during the ‘silent’ phase of the TDC, the skew error results in imperfect preservation of the quantization error. Another drawback of the GRO TDC, is the difficulty of achieving high-order noise-shaping with this structure, which could principally further improve the TDC resolution and reduce the need for fast delay elements.

III. DESIGN OF A THIRD-ORDER MASH $\Delta\Sigma$ TDC

The MASH $\Delta\Sigma$ TDC, which has been briefly described in [18], achieves high resolution by using oversampling and third-order noise-shaping. The quantization step size of the TDC is 18 ns, which is generated by an on-chip relaxation oscillator. The input timing pulse, which has the start signal on its rising edge and the stop signal on its falling edge, enables the oscillator during the measurement interval. A coarse conversion is hence performed by counting the number of periods of the oscillator clock. When the stop signal arrives, the oscillation is stopped and the quantization error is preserved as a voltage. First-order noise-shaping can be achieved by forwarding this error information into the next measurement phase, hence canceling the low frequency quantization noise. The reduced baseband quantization noise power will be further suppressed by oversampling. Principally, this is similar with the GRO TDC, but the skew error caused by charge redistribution is negligible here due to the large capacitance that is used for the quantization error storage. This first-order noise-shaping can also be easily extended to a higher order. A third-order noise-shaping TDC implemented in IBM 0.13 μm CMOS is demonstrated in this work.

A. System Architecture

The system architecture of a 1-1-1 MASH $\Delta\Sigma$ TDC is shown in Fig. 7. All three stages have the same structure and are followed by a digital processing block. Each stage works as a relaxation oscillator, controlled by the input time signal. It works as follows: The time signal T_{in} controls a current to charge one of the two capacitors during its active phase. For instance, vinp1 starts rising when vinn1 stays at vlow , as illustrated in Fig. 6. When vinp1 exceeds the threshold voltage V_{REF} , the comparator output becomes ‘1’. This reverses the state of

Fig. 6. Timing diagram of the MASH $\Delta\Sigma$ TDC.

the SR-latch, and triggers the oscillation. The output of the oscillator is connected to a 4-bit counter. The final result in the counter is a digitized copy of the input signal with large quantization error. After the stop signal arrives, the charging current is disconnected from the capacitors. By preserving the residue voltage on the capacitor at the end of each measurement interval, the quantization error $q[1]$, which refers to the phase of the oscillator clock, is also preserved. When the following measurement is initiated, the previous quantization error will be subtracted from the next input, since the counter is only driven by the rising edge of the clock. The overall quantization error introduced into this measurement can then be described as

$$q_{\text{err}}[2] = q[2] - q[1]. \quad (1)$$

If the quantization error from each measurement interval is adequately scrambled to a random noise, this will result in first-order noise shaping of the quantization error.

The third-order noise-shaping is obtained by cascading all three stages. The time signal which feeds into a following stage is generated by subtracting the quantization error from the input of the previous stage. This is done by taking the first rising edge of the counting clock as the new start signal, and keeping the same stop signal as the TDC's initial input. The output of the 1-1-1 MASH TDC is given by

$$D_{\text{out}} = T_{\text{in}} + (1 - z^{-1})^3 \cdot q_{\text{err}3}. \quad (2)$$

where $q_{\text{err}3}$ is the quantization error of the third stage. All digital blocks used for signal processing are synchronized by the falling edge of the input time signal. The theoretical *rms* value of the quantization noise power [19] can be described as

$$q_{\text{err}rms} = \frac{T_d}{\sqrt{3}} \frac{\pi^L}{\sqrt{2L+1}} (\text{OSR})^{-(L+1/2)}, \quad (3)$$

where T_d is the quantization step size, OSR is the oversampling ratio, and L is the order of noise-shaping function. Oversampling ratio (OSR) is the ratio of the conversion rate to the Nyquist frequency. An example TDC using a T_d as 18 ns, OSR as 25, and L as 3, will then ideally have *rms* quantization error of 1.6 ps. If a higher OSR is employed, and the other parameters remain the same, the theoretical *rms* quantization error can be reduced to only 0.5 fs, which is far below the physical noise floor of the TDC.

Fig. 7. System architecture of the 1-1-1 MASH $\Delta\Sigma$ TDC. Fig. 8. Schematics of the constant- g_m biased threshold-detection comparator.

B. Circuit Design

The on-chip relaxation oscillator provides the counting clock for the $\Delta\Sigma$ TDC, whose frequency therefore needs to be stable over process and temperature. The period of the relaxation oscillator can be expressed as $(V_{REF} \cdot 2C)/I_{REF} + 2t_{cmp}$. If the comparator delay t_{cmp} is small enough comparing to the whole clock period, the oscillator frequency becomes $I_{REF}/(V_{REF} \cdot 2C)$. By correlating V_{REF} and I_{REF} as $V_{REF} = I_{REF} \cdot R$, its frequency becomes only dependent on passive components, which is $1/(2 \cdot RC)$. Thus, it exhibits inherent PVT variation tolerance. In this design,

$I_{REF} = 50 \mu A$, $R = 14 \text{ k}\Omega$, and $C = 0.64 \text{ pF}$, which gives a counting frequency of 55 MHz.

Practically, a comparator always has a non-zero delay. When the oscillator needs to be started and stopped, a phase skew error might occur, since the comparator state can not be perfectly preserved due to the hysteresis. This will introduce extra noise into the preserved quantization error, and it can only be suppressed by oversampling. Compared to the timing jitter in the oscillator, the comparator delay is usually much larger. In order to achieve a higher SNR, either the comparator delay has to be limited to a small amount or calibration needs to be applied. Fig. 8 shows the schematic of a threshold-detection comparator used in the

Fig. 9. Measured PSD with 18 kHz -3 dBFS input (OSR = 25).

Fig. 10. (a) Measured PSD and (b) output waveform after 100 kHz LPF, with 22 kHz -40 dBFS input (OSR = 250).

relaxation oscillator. It is built in a multi-stage structure, for high speed consideration. Each of the first three stages has a gain of 10 dB and consumes 40 μA current. The last stage provides a higher gain of 20 dB with a power consumption of 80 μA . Input differential pairs of all stages formed by transistors M1a, M1b, M2a, M2b, M3a, M3b, M4a and M4b, are optimized for both

Fig. 11. Measured counting clock frequencies of 5 different samples. These measurements were obtained from the low dose rate experiment.

Fig. 12. Measured ENOB and total current consumption of the $\Delta\Sigma$ TDC, obtained from the high dose rate experiment.

matching and speed. Two comparators in each stage, controlled by the enabling signal *pwd*, are turned off alternately to save power, when its connected capacitor is not being charged. The switch M6 in the last stage, controlled by *EN*, is added to reduce the skew error caused by the comparator delay. Polysilicon resistors, which are radiation hard [20], are employed as loads for each stage. Additionally, in order to obtain robust voltage gain against radiation damage, a constant- g_m biasing circuit is used to provide biasing current for the comparator. It adjusts the biasing current adaptively according to the threshold voltage variation of the MOS transistor, and keeps the transconductance constant.

Due to the fact that the system is operating in a single-ended mode, the demand for matching within one single stage is more relaxed than for a differential system. Moreover, since all noise in a following stage will be suppressed by the total gain of its preceding stages, the inter-stage matching is only important between the first and second stage, and it can be easily improved by using large value capacitances and resistances. On the layout level, guard rings are extensively used for all NMOS and PMOS cells to prevent single event latchup, and also provide better noise isolation.

Fig. 13. Setup of the high dose rate gamma irradiation experiment. Photos of the substrate and the die before (left) and after (right) irradiation are shown.

IV. PRE-RAD MEASUREMENT

A pulse-width-modulation (PWM) signal, modulated by a sine wave, is employed to evaluate the performance of the TDC. The conversion rate can be varied from 5 MHz to 50 MHz. For a signal bandwidth of 100 kHz, it turns to an OSR of 25 to 250. The TDC is configured first in a low conversion rate (5 MHz) mode. The full scale input range determined by the conversion rate is then 200 ns. An 18 kHz -3 dBFS PWM signal is applied to the input of the TDC. The output spectrum is shown in Fig. 9. It shows an SNDR of 60.3 dB and 50 ps resolution. The resolution of the TDC is mainly limited by the skew error introduced by the comparator delay. It can be reduced by increasing the OSR.

In the second measurement, the OSR is increased to 250. This requires a higher conversion rate, which is now 50 MHz. The input full scale range is hence reduced to 20 ns. One should notice that, although increasing the OSR can reduce the skew error in the comparator, and further improve the TDC's SNDR, the effective quantization bits of the counter are also reduced at the same time, since the quantization step size is remaining constant. Consequently, the full scale SNDR and ENOB of the TDC will stay nearly unchanged regardless of the value of OSR. Therefore, a trade-off between time resolution and input range exists in the TDC. The power spectrum and waveform of the TDC output shown in Fig. 10, are carried out with a 22 kHz -40 dBFS input, which has a peak to peak amplitude of 200 ps. An effective number of bits (ENOB) of 11 bits and a resolution of 5.6 ps are achieved, respectively.

V. GAMMA-DOSE RADIATION ASSESSMENT

Radiation assessments have been performed at the Belgian Nuclear Research Centre, SCK·CEN. The low dose rate irradiation experiment was carried out from the "RITA" facility, where five TDC samples were irradiated with ^{60}Co gamma source. The measured dose rate was 1.2 kGy/h. The frequencies of the relaxation oscillators in five TDC samples are monitored continuously during the whole 130 h irradiation period. Fig. 11 shows

the real-time results obtained from a digital oscilloscope. The five frequencies differ from each other due to the die to die variation. From 0 to 160 kGy total ionizing dose (TID), no degradation on the frequencies has been found. Only small ripples exhibit, which are mainly caused by the jitter noise coupling into the cable (10 meters long). This approves the radiation hardness of the RC relaxation oscillator.

An on-line dynamic measurement under high dose rate radiation has also been done, proving the TDCs robustness. The experiment was carried out from the "Brigitte" facility, at a dose rate of 30 kGy/h. Fig. 13 shows the setup of the experiment. The ceramic substrate with the bonded TDC is carried by a container, which is placed in the under water gamma irradiation facility. The substrate is connected to all measurement equipment by a cable with 10 meters length. The on-line measurement results are shown in Fig. 12. When the system is working in the high conversion rate (50 MHz) mode, the ENOB of the TDC drops only 1 bit after a total dose of 3.4 MGy. This means that a resolution of 10.5 ps can still be achieved. The TDC works functionally till at least 5 MGy. For the TDC working in the low conversion rate (5 MHz) mode, it shows less drop in performance, which can be clearly seen from Fig. 12. This is because the timing noise converted from the radiation introduced noise voltage is relatively small compared to the quantization noise in the low conversion rate mode. The current consumption of the TDC system is nearly unaffected during the whole irradiation period. Photos of the substrate and the die before and after 5 MGy total dose irradiation are also shown in Fig. 13.

VI. CONCLUSION

This paper addresses several practical issues regarding the application of TDCs in harsh environments. Based on a review of some state-of-the-art TDCs, we conclude the noise-shaping TDC as the preferable choice for continuous-time pulsed LIDAR application in nuclear reactors. We have also presented a third-order MASH $\Delta\Sigma$ TDC with 6-ps time resolution. Unlike

conventional Nyquist TDCs, its resolution is not limited by the matching property of the technology. PVT variation tolerance is made inherent to the design, which guarantees the TDC's robustness. The proposed TDC is implemented in 0.13 μm CMOS. It consumes only 1.7 mW from a 1.2 V supply, and occupies an area of 0.11 mm².

Gamma radiation assessments with both a low dose rate of 1.2 kGy/h and a high dose rate of 30 kGy/h have been performed, proving the TDC's radiation hardness. The system power consumption is almost not affected and even after an extremely high radiation dose of 3.4 MGy, the ENOB drops only 1 bit and, for an OSR of 250, a 10.5 ps time resolution is still achieved.

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