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1-1-1 MASH $\Delta\Sigma$ Time-to-Digital Converters with 6 ps Resolution and Third-Order Noise-Shaping

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Abstract—Two 1-1-1 MASH $\Delta\Sigma$ Time-to-Digital converters (TDCs) are presented in this paper. Third-order time domain noise-shaping has been adopted by the TDCs to achieve better than 6 ps resolution. Following a detailed analysis of the noise generation and propagation in the MASH $\Delta\Sigma$ structure, the first prototyping TDC has been realized in 0.13 μm CMOS technology. It achieves an ENOB of 11 bits and consumes 1.7 mW from a 1.2 V supply. In the second MASH TDC, a delay-line assisted calibration technique is introduced to mitigate the phase skew caused by the large comparator delay, which is the main limiting factor of the MASH TDC's resolution. The demonstrated TDC achieves an ENOB of 13 bits and a wide input range of 100 ns. This TDC shows a temperature coefficient of 176 ppm/ $^{\circ}\text{C}$ within a temperature range of -20 to 120 $^{\circ}\text{C}$. It consumes only 0.7 mW and occupies 0.08 mm² area (core).

Index Terms—Time-to-Digital Converter, Delta-Sigma, MASH, noise-shaping, delay-line assisted calibration, temperature-stable.

I. INTRODUCTION

RECENTLY, high resolution time-to-digital converters (TDCs) have gained more and more interest due to their increasing implementation in digital PLLs, ADCs, jitter measurement and time-of-flight (TOF) rangefinders. Specifically, a laser TOF rangefinder which operates by measuring the flight time of a light pulse from a laser transmitter to the target and back to an optical detector, can be applied to many industrial purposes, e.g., positioning of vehicles, detecting particles in atmosphere, measuring level heights in radioactive environments, etc. The accuracy of a TOF rangefinder is mainly determined by the resolution of the TDC employed. For instance, in order to detect 1 mm distance, a TDC with at least 6.7 ps time resolution is required. Furthermore, a TOF rangefinder for nuclear instrument applications typically works in a range of 1 to 30 meters, which corresponds to a TDC measurement range of 3.3 to 200 ns. Upcoming applications in nuclear fusion reactors like the International Thermonuclear

Experimental Reactor (ITER), electronic components are required to achieve good performance in harsh environments facing high temperature and radiation, where the threshold voltage, transconductance, and delay of a transistor undergo dramatic changes. In these cases, the high resolution, accuracy and robustness of the TDC need to be inherent to the design.

Conventional TDCs were built based on the CMOS gate-delay-line structure [1], whose highest achievable resolution is limited by the intrinsic delay of a CMOS inverter gate. In order to get sub-gate-delay resolution, the Vernier method [2], [3] was commonly used. However, the mismatch problem caused by process variation limits its effectiveness. Although calibration can be applied to compensate for the mismatch error [4], huge efforts are needed since each delay element in the TDC has to be tuned individually. Other methods to achieve sub-gate-delay resolution such as time amplification (TA) [5], [6], local passive interpolation (LPI) [7], [8], gated-ring-oscillator (GRO) [9] and successive approximation (SAR) [10], are vulnerable to transistor characteristic changing and temperature variation. Although calibration employing extensively extra feedback circuitries can be applied to maintain a nearly constant gate delay, its tuning ability is quite limited with regard to a wide temperature range of over 200 $^{\circ}\text{C}$ and a multi-MGy total irradiation dose (TID). Moreover, the power consumption of delay-line based TDCs increases linearly with the peak-to-peak amplitude of the input time signal, which is undesirable for wide range measurement.

It is well known that, $\Delta\Sigma$ ADCs, which has been successfully implemented in analog-to-digital conversion for years, are highly immune to environmental noise and component mismatch. Some works brought the same principle into phase-domain data conversion, as in [11], [12], and achieved first-order and second-order noise-shaping, respectively. However, these phase-domain $\Delta\Sigma$ ADCs are analog intensive approaches, and the phase information is converted back to the voltage-domain. As the technology scales down, this becomes less attractive due to the difficulty of achieving high-gain and wide-bandwidth analog blocks under strongly reduced supply but relatively unchanged threshold voltage. Moreover, their performances are highly relying on the linearity of the front-end phase detector, which practically limits the dynamic range of the input time signal.

This work presents a digital intensive third-order MASH $\Delta\Sigma$ TDC, which has been briefly reported first in [13]. It achieves better than 10 ps time resolution when a coarse quantization step of 16 ns is used. The on-chip generated quantization reference clock has a frequency depending primarily

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Fig. 1. Behavior model of the error-feedback structure based TDC.

on passive components, which shows intrinsic PVT variation tolerance. The data conversion is mainly being processed in the time-domain, which benefits most from technology down-scaling. Furthermore, the MASH TDC exhibits low power nature owing to the employment of large quantization steps, which makes it suitable for applications pursuing a wide measurement range. The remainder of this paper is organized as follows. First, the architecture of the third-order MASH $\Delta\Sigma$ TDC is investigated in Section II. Detailed noise analysis of the TDC is given in Section III, regarding mainly the jitter noise in the relaxation oscillator and the phase skew error introduced by the comparator delay. Section IV shows the circuits implementation and measurement results of the first prototyping MASH $\Delta\Sigma$ TDC (Chip I). In Section V, the delay-line assisted calibration technique is introduced to solve the phase skew problem. A demonstrated TDC (Chip II) shows a similar time resolution with Chip I but the input dynamic range has been increased 5 times, when the power consumption is reduced by more than half. A conclusion is drawn in Section VI.

II. ARCHITECTURE OF THE 1-1-1 MASH $\Delta\Sigma$ TDC

A. The first-order Error-Feedback TDC

The commonly used $\Delta\Sigma$ ADC structure which consists of integrators can not be directly adopted by a TDC, due to the difficulty of realizing a time integrator. The error-feedback noise-shaping structure introduced in early 60s is impractical for a $\Delta\Sigma$ ADC since its performance is limited by the inaccuracy of the analog subtractors. However, time subtraction can be easily realized by nand/nor operation, and moreover, the error-feedback structure does not require an explicit integrator in the loop. A first-order noise-shaping TDC can be built in an error-feedback manner, as shown in Fig. 1. The input time signal t_{in} is first digitized by using a reference clock t_{ref} . The quantizer can simply be a counter, which is enabled/disabled by the input signal. A quantization error presents at the output when the input signal is not an integer times of the reference clock period. It can be reproduced by subtracting the input signal from the corresponding reference time of the digital output. A memory element is inserted in the feedback loop to preserve the quantization error before it is being subtracted from the next input signal.

However, directly preserving the quantization error in the time regime is still impossible with current technologies: the

Fig. 2. (a) Schematic and (b) timing diagram of the relaxation oscillator based first-order error-feedback TDC.

time information has to be converted into another intermediate physical quantity such as voltage or charge. A relaxation oscillator (Fig. 2a) can generate a clock by alternatively charging and discharging two capacitors. The phase of the clock corresponds to the voltage on each capacitor. The time can be measured by enabling the oscillator during the measurement interval and counting the number of periods of the generated clock. When the oscillation stops, the phase of the clock, which refers to the quantization error, can be stored on the capacitor as a residue voltage. First-order noise-shaping can be achieved by forwarding this error information into the next measurement phase, hence canceling the low frequency quantization noise. Principally, it is the same as the GRO [9], but the skew error caused by charge redistribution and path leakage during the start and stop of the oscillator is negligible here due to the large capacitance C and the controllable large charging slope (In the case of a not too slow counting clock, e.g., 62.5 MHz in this design).

The first-order error-feedback TDC works as follows: The time signal t_{in} controls a current to charge one of the two capacitors during its active phase. For instance, v_{inp} starts rising when v_{inn} stays at v_{low} , as illustrated in Fig. 2b. When v_{inp} exceeds the threshold voltage V_{REF} , the comparator output becomes '1'. This reverses the state of the SR-latch, and triggers the oscillation. The output of the oscillator is connected to a 4-bit counter. The final result in the counter is a digitized copy of the input signal with large quantization error. After the stop signal arrives, the charging current is disconnected from the capacitors; the counter is first read out and then reset to 0. By preserving the residue voltage on the capacitor at the end of each measurement interval, the quantization error $q[k-1]$, which refers to the phase of the oscillator clock, is also preserved. The quantization error takes on a uniform distribution over the interval $[0, T_d]$, where T_d is

Fig. 3. Behavior models of (a) the classic 1-1 MASH $\Delta\Sigma$ ADC and (b) the 1-1 MASH error-feedback TDC.

the coarse quantization step size. When the next measurement is initiated, the previous quantization error will be subtracted from the next input, due to the fact that the counter is only driven by the rising edge of the clock. The overall quantization error introduced into this measurement can then be described as

$$q_{\text{err}}[k] = q[k] - q[k-1]. \quad (1)$$

If the quantization error from each measurement interval is adequately scrambled to a random noise, this will result in first-order noise-shaping of the quantization error.

B. High-order Noise-Shaping TDC

Similar to design of $\Delta\Sigma$ ADCs, the noise-shaping concept can also be extended to higher orders. Recalling the structure of the classic single-loop second-order $\Delta\Sigma$ ADC, it replaces the quantizer in the first-order modulator with another $\Delta\Sigma$ ADC, which can further suppress the in-band quantization

noise. However, in this configuration, integration of the input signal is unavoidable, which is difficult to perform and undesired in time domain operation. Instead, the $\Delta\Sigma$ ADC configured in a MASH architecture, can obtain the same high-order noise-shaping property but offer more freedom to choose a structure for each stage. For instance, a 1-1 MASH $\Delta\Sigma$ ADC, shown in Fig. 3a, is built by cascading two identical single-loop first-order $\Delta\Sigma$ ADCs. A signal contains the quantization error from the previous stage is fed into the second stage. Two stages are combined together with the help of few additional digital processing blocks to achieve second-order noise-shaping.

In the case of building a 1-1 MASH $\Delta\Sigma$ TDC, two identical first-order error-feedback TDCs can be cascaded together, as shown in Fig. 3b. It is algebraically equivalent to the conventional 1-1 MASH $\Delta\Sigma$ ADC. The time signal which feeds into a following stage is generated by subtracting the quantization error from the input of the previous stage. This is done by taking the first rising edge of the counting clock as the new start signal, and keeping the same stop signal as the TDC's initial input. More details regarding this operation is described in the design of the time regenerator.

By cascading more error-feedback structures, a higher order noise-shaping TDC can be formed. In this work, a third-order MASH $\Delta\Sigma$ TDC is demonstrated. The system architecture of a 1-1-1 MASH $\Delta\Sigma$ TDC is shown in Fig. 4. All three stages have the same structure and are followed by a digital processing block. Each stage works as a relaxation oscillator, controlled by the input time signal. The output of the 1-1-1 MASH TDC is given by

$$Dout = tin + (1 - z^{-1})^3 \cdot q_{\text{err}3}. \quad (2)$$

where $q_{\text{err}3}$ is the quantization error in the third stage. All digital blocks used for signal processing are synchronized by the falling edge of the input time signal. The theoretical *rms* value of the quantization noise power can be written as [14]

$$q_{\text{err}rms} = \frac{T_d}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} (OSR)^{-(L+1/2)}, \quad (3)$$

where OSR is the oversampling ratio, and L is the order of noise-shaping function. An example TDC using a T_d as 16 ns, OSR as 25, and L as 3, will then ideally have *rms* quantization error of 0.7 ps. If a higher OSR of 250 is employed, and the other parameters remain the same, the theoretical *rms* quantization error can be reduced to only 0.2 fs, which is far below the physical noise floor of the TDC.

Although there is no physical limitation for all oscillator-based TDCs' input range, which can be easily extended by cycling the signal in the same TDC core, this is true only when the single-shot measurement is performed. If the input time signal has a non-DC frequency, the measurement range of the TDC is in fact limited by the sampling rate. The reason is that, the stop signal of the current measurement has to come earlier than the next start signal, otherwise two input time signals will conflict. In the MASH $\Delta\Sigma$ TDC, there is also a special relation between the OSR and full scale input range. The bandwidth of the input signal, BW , is set to 100 kHz in this design. The sampling clock of the TDC system is then

Fig. 4. System architecture of the 1-1-1 MASH $\Delta\Sigma$ TDC.

Fig. 5. Relation between OSR, full-scale input range and the effective resolution.

equal to $2BW \cdot OSR$. Due to the input signal's timing nature, the peak-to-peak full scale input signal amplitude T_{fspp} has to be smaller than one period of the sampling clock. For instance, when the OSR is 25, T_{fspp} can not exceed 200 ns. This relation is shown in Fig. 5. When the ideal effective resolution of the MASH TDC improves with a higher OSR, the full-scale input range reduces. Therefore, when the TDC is being designed to achieve the targeted resolution, the SNR also needs to be optimized in order to achieve a wide input range. This design

concept will be kept throughout the paper.

III. NOISE ANALYSIS

When only the quantization noise is considered, the theoretical SNR of the 1-1-1 MASH $\Delta\Sigma$ TDC can be expressed as

$$\begin{aligned}
 SNR &= 10\log\left(\frac{s_{rms}^2}{q_{err,rms}^2}\right) \\
 &= 20\log\left[\frac{(2^N-1) \cdot T_d}{\sqrt{2} \cdot \frac{T_d}{\sqrt{12}} \cdot \frac{\pi^L}{\sqrt{2L+1}} (OSR)^{-(L+1/2)}}\right] \\
 &= 10\log[6(2L+1)] - 10L + 20(L + \frac{1}{2})\log(OSR) \\
 &\quad + 20\log(2^N - 1).
 \end{aligned} \tag{4}$$

In this design, L is set to 3, and N , the bits of the coarse quantizer, is set to 4. For an OSR of 25, the SNR is calculated as 107.7 dB, which turns out to an ENOB of 17.5 bits. However, the finest achievable resolution of the MASH TDC is practically limited by the jitter noise in the relaxation oscillator, phase skew caused by start/stop the oscillator and switching charge injection. Among them, the jitter noise and phase skew draw most attention, since they are at a much

Fig. 6. Representation of noise in the relaxation oscillator based first-order $\Delta\Sigma$ TDC.

higher power level than the switching charge injection noise, which is actually negligible when the charging slop on capacitors is sufficiently large. A detailed analysis of these two noise contributions is stated below. In this analysis, only the noise from the first stage is considered, since in the second and third stages, the circuit noises are reduced by first- and second-order noise-shaping, respectively.

The noise analysis is based on the schematic shown in Fig. 2a. All the noise sources presented in the circuit can be modeled as shown in Fig. 6, where the fully-symmetric relaxation oscillator is presented in the half-circuit mode. Then we have

$$q_{err} = tin + e_{skew} - D \cdot T_d \quad (5)$$

$$T_d = \frac{(VREF + Vn) \cdot 2C}{IREF + In} \quad (6)$$

where e_{skew} is the phase skew error caused by the comparator delay, D is the output code, T_d is the oscillation period, Vn is the equivalent input noise generator which represents the noise in the comparator, and In is the noise in the current source. The delay of the comparator is not included in the oscillation period, since it only adds a DC offset to the oscillation period. And its noise contribution to the system's performance is modeled as e_{skew} .

In and Vn are two primary contributors to the relaxation oscillator's jitter. The latter is generally the dominant cause of jitter, due to its much larger contributing bandwidth [15], [16]. Thus, the output code of the first-order TDC can be described as

$$\begin{aligned} D &= \frac{tin + e_{skew} - q_{err} \cdot (1 - z^{-1})}{\frac{(VREF + Vn) \cdot 2C}{IREF}} \\ &= \frac{tin + e_{skew} - q_{err} \cdot (1 - z^{-1})}{\frac{2(VREF + Vn)}{S}}. \end{aligned} \quad (7)$$

where S is the charging slop of the capacitor. Therefore, apart from the noise-shaped quantization error, two additional noises also appear at the TDC's output. In order to derive

the design specification of the TDC more accurately, it is important to know the impact of those two noises on the TDC's overall performance. Quantitative calculations of the TDC's SNR determined by the oscillator jitter and phase skew error, respectively, are stated below.

A. Timing Jitter

Assuming the timing jitter is the dominant noise in the TDC, the ideal SNR of the TDC can then be described as

$$\begin{aligned} SNR &= 10 \log \left(\frac{T_{fs}^2 / 2}{\sigma_{\Delta T_{OSC}}^2 / OSR} \right) \\ &= 6.02 \cdot ENOB + 1.76. \end{aligned} \quad (8)$$

T_{fs} is the full scale input level, which is half of T_{fspp} , and $\sigma_{\Delta T_{OSC}}$ is the *rms* jitter. Therefore, for an OSR of 25, in order to achieve an ENOB of 14 bits, the *rms* jitter needs to be smaller than 18 ps. Using a formula derived in [16]

$$PN(f_m) = \frac{f_{OSC}}{f_m^2} \cdot \left(\frac{\sigma_{\Delta T_{OSC}}}{T_{OSC}} \right)^2, \quad (9)$$

where $PN(f_m)$ is the phase noise, f_m is the carrier offset frequency, and f_{OSC} is the oscillating frequency (62.5 MHz in this case). To fulfill the *rms* jitter requirement derived above, the oscillator needs to show a phase noise of better than -81.1 dBc/Hz at 100 kHz offset frequency. By substituting (9) into (8), we can get

$$SNR = 10 \log \left(\frac{f_{OSC}^3}{8 \cdot PN(f_m) \cdot f_m^4 \cdot OSR} \right). \quad (10)$$

The relation between the SNR and jitter can also be predicted from a simulation of the MASH TDC behavioral model. The 1-1-1 MASH TDC was modeled in Simulink, which has the same operation behavior as in the real circuits. An additive white noise source is added on the reference voltage, which gives an estimation of the timing jitter in the oscillator. The result is shown in Fig. 7a. With a higher OSR, the SNR drops due to decrease of the full scale input range as explained in Section II. But it has better tolerance to the timing jitter, since the in-band jitter noise power can be reduced by oversampling. For a RC relaxation oscillator, which has a frequency of 62.5 MHz, the minimum achievable phase noise is approximately -100 dBc/Hz at 100 kHz offset frequency [17]. It means that the highest SNR can be achieved by the MASH TDC is 110 dB, when only the jitter noise in considered.

B. Phase Skew

The phase skew, e_{skew} , occurs only when the oscillator needs to be started and stopped. When the relaxation oscillator is turned off, the comparator state may not be perfectly preserved due to the hysteresis. This will introduce extra noise into the preserved quantization error, and it can only be suppressed by oversampling. The phase skew occurs when the stop signal arrives during the time the comparator enters its state-reversing phase, when v_{inn} or v_{inp} just exceeds $VREF$. A delay always exists before the comparator can make a final decision according to its input change. It is impractical to save

Fig. 7. Simulated SNR versus (a) Timing jitter and (b) Comparator delay.

Fig. 8. Illustration of the phase skew introduced by the comparator delay.

all the intermediate states of the comparator when the system enters idle. So the output of the comparator will continue rising till its final state '1' even if the oscillation has been stopped. Therefore, when the next start signal arrives, the SR-latch will immediately reverse its state, and alternates the capacitor being charged. This will result in a change in the counting clock period and introduce extra phase skew error to the preserved quantization residue time. This error is shown by red lines in Fig. 8.

The relation between the SNR and the comparator delay, as shown in Fig. 7b, is predicted by simulating the same Simulink model used in timing jitter estimation. Mathematically, when the stop signal arrives, the time domain representative of the voltage on the capacitor follows a uniform distribution over the interval $[0, T_{OSC}/2)$. When this voltage is aligning between $T_{OSC}/2 - t_{cmp}$ and $T_{OSC}/2$, where t_{cmp} is the comparator delay, the random skew error will occur. The mean value of this error equals $t_{cmp}/2$, and the probability density function of the error is

$$f(e_{skew}) = \frac{1}{T_{OSC}/2}. \quad (11)$$

Therefore, the variance of the phase skew error can be de-

scribed as

$$\begin{aligned} \sigma_{e_{skew}}^2 &= \int_0^{t_{cmp}} (e_{skew} - \frac{t_{cmp}}{2})^2 \cdot \frac{2}{T_{OSC}} de_{skew} \\ &= \frac{t_{cmp}^3}{6 \cdot T_{OSC}}. \end{aligned} \quad (12)$$

Similar to (8), when only the phase skew error is taken into account, the theoretical SNR of the MASH TDC can be calculated as

$$SNR = 10 \log \left(\frac{T_{fs}^2/2}{\sigma_{e_{skew}}^2 / OSR} \right). \quad (13)$$

Thus, for an OSR of 25, if the comparator has a delay of 1 ns, the SNR will be only 70.8 dB. When increasing the OSR, the skew error can be reduced by the same order. However, the full scale input is decreasing at the same time. Eventually, the SNR of the TDC remains almost unchanged. But the time resolution $(T_{fs}/2^{ENOB} - 1)$ can be improved at the cost of a smaller input time range. Comparing to the quantization noise and timing jitter, the phase skew error becomes the dominant noise in the MASH TDC. In order to achieve a higher SNR, either the comparator delay has to be limited to a small amount or calibration needs to be applied.

Other path delays such as the one in the SR latch and the gate delay of the oscillator switches, have less impact on the performance of the TDC. This is due to the fact that the input signals to the SR latch and oscillator switches are already rail-to-rail signals with sharp rising/falling edges, and thus those delays can be made sufficiently small, e.g., <100ps.

IV. CHIP I: FIRST PROTOTYPING OF THE MASH $\Delta\Sigma$ TDC

A. Circuit Design

The main circuit blocks in the 1-1-1 MASH $\Delta\Sigma$ TDC are the relaxation oscillator, the counter, the time regenerator, and digital processing units. Among them, the performance of the relaxation oscillator determines the highest achievable SNR of the TDC. The conventional 2-capacitor relaxation oscillator structure [18] is used in this design, due to its simplicity of controlling. The specification of the relaxation oscillator is derived first according to the noise analysis presented in

Fig. 9. Schematic of the 4-stage threshold-detection comparator.

(a)

(b)

Fig. 10. (a) Timing diagram and (b) schematic of the time regenerator.

Section III, and then a trade-off has been made between the time resolution and power consumption.

1) *Relaxation Oscillator*: The on-chip relaxation oscillator provides the reference clock for the $\Delta\Sigma$ TDC, whose frequency therefore needs to stable over process and temperature. The period of the relaxation oscillator can be expressed as $(VREF \cdot 2C) / IREF + 2t_{cmp}$. If the comparator delay t_{cmp} is small enough comparing to the whole clock period, the oscillator frequency becomes $IREF / (VREF \cdot 2C)$. By correlating $VREF$ and $IREF$ as $VREF = IREF \cdot R$, its frequency becomes only depending on passive components, which is $1 / (2 \cdot RC)$. Thus, it exhibits inherent PVT variation tolerance and the matching between stages is better than for its MASH ADC counterparts. Furthermore, the matching between Q and $\bar{Q}$ path is not important, since only the whole period of the oscillator clock is used as one quantization step, regardless of the duty cycle. In addition to the jitter noise in the relaxation oscillator, charge injection when turning on/off the input control switches

and their associated leakage current also contributes to the overall noise level. In the conversion to time noise the local noise voltage is divided by the charging slope of the capacitor. Thus, a larger slope is mostly desirable. In this design, $IREF = 50 \mu A$, $VREF = 650 mV$, and $C = 0.64 pF$, which gives a charging slope of $80 \mu V/ps$. According to simulation, the relaxation oscillator has a phase noise of $-87 dBc/Hz$ at $100 kHz$ offset frequency, which is adequate to achieve better than 14 bits ENOB.

In order to limit the impact of the phase skew error introduced by the large comparator delay on the overall TDC's performance, fast comparators must be used. Fig. 9 shows the schematic of the threshold-detection comparator used in the relaxation oscillator. It is built in a multi-stage structure, for high speed consideration. Each of the first three stages has a gain of 10 dB and consumes $40 \mu A$ current. The last stage provides a higher gain of 20 dB with a power consumption of $80 \mu A$. Input differential pairs of all stages formed by transistors M1a, M1b, M2a, M2b, M3a, M3b, M4a and M4b, are optimized for both matching and speed. Two comparators in each stage, controlled by the enabling signal *pwd*, are turned off alternately to save power, when its connected capacitor is not being charged. The switch M5 in the last stage, controlled by *EN*, is added to further reduce the effective phase skew caused by the comparator delay. Overall the comparator consumes $200 \mu A$ and has an effective delay of $800 ps$, which is capable to achieve an SNDR of around 65 dB when the OSR is 25, according to simulations. A higher SNDR is achievable by employing a faster comparator. However, it consumes too much power to implement a high speed continuous-time comparator in this technology. A constant- g_m biasing circuit is used to provide biasing current for the comparator. It adjusts the biasing current adaptively according to the threshold voltage variation of the MOS transistor, and keeps the transconductance constant. It also generates the charging current $IREF$ for each stage and the reference voltage $VREF$ for the comparator.

2) *Time Regenerator*: The time regenerator produces the input time signal for a following stage. As explained earlier, it generates a timing pulse whose rising edge is aligned with the first rising edge of the counting clock, and the falling edge comes when the stop signal arrives. As illustrated in Fig. 10a,

Fig. 11. (a) Measured PSD and (b) output waveform after 100 kHz LPF, with 18 kHz -3 dBFS input (OSR=25).

Fig. 12. (a) Measured PSD and (b) output waveform after 100 kHz LPF, with 22 kHz -40 dBFS input (OSR=250).

$tin[0]$ is first digitized, resulting a quantization error q_{err} . This error is subtracted from the second input signal $tin[1]$ to generate the input signal for the second stage. This can be achieved by using an RS latch. In order to inactivate the second, the third, ... rising edges of the counting clock, a D flip flop is placed at the CLK path before the RS latch, as shown in Fig. 10b.

B. Measurement

The 1-1-1 MASH $\Delta\Sigma$ TDC is implemented in $0.13 \mu\text{m}$ CMOS. It consumes 1.7 mW from a 1.2 V supply. The die photo of the TDC is shown in Fig. 14. A time domain sine wave signal is employed to evaluate the dynamic performance of the TDC. The timing pulse containing the start and stop signal at the rising and falling edge respectively, is directly taken from the signal generator. The signal source generates a continuous-time pulse-width-modulated (PWM) square wave, and the width of each pulse (corresponding to the time period) is modulated by a sine signal whose frequency is between DC to 100 kHz. In a real application, an edge combiner can be added on-chip to generate the timing pulse for the TDC core.

Although the edge combiner might fail when the signal width becomes considerably small (e.g., <10 ps), it's not the case for most applications including the TOF rangefinder (with 1 to 30 meters detection range). The dynamic measurement was performed with this PWM signal which has a DC bias of 100 ns down to 10 ns.

The conversion rate of the TDC can be varied from 5 MHz to 50 MHz. For a signal bandwidth of 100 kHz, it turns to an OSR of 25 to 250. The TDC is configured first in a low conversion rate (5 MHz) mode. The full scale input range determined by the conversion rate is then 200 ns. An 18 kHz -3 dBFS PWM signal is applied to the input of the TDC. The output spectrum and waveform are shown in Fig. 11. It shows an SNDR of 60.3 dB. The resolution of the TDC is mainly limited by the phase skew error introduced by the comparator delay. It can be reduced by increasing the OSR. In the second measurement, the OSR is increased to 250. This requires a higher conversion rate, which is now 50 MHz. The input full scale range is hence reduced to 20 ns. The power spectrum and waveform of the TDC output shown in Fig. 12, are carried out with a 22 kHz -40 dBFS input, which has a peak to peak

Fig. 13. Dynamic range of the MASH TDC.

Fig. 14. Die photo of the MASH $\Delta\Sigma$ TDC.

amplitude of 200 ps. An ENOB of 11 bits and an effective resolution of 5.6 ps are achieved, respectively.

One should notice that, although increasing the OSR can reduce the phase skew error in the comparator, and further improve the TDC's SNDR, the effective quantization bits of the counter are also reduced at the same time, since the quantization step size is remaining constant. Consequently, the full scale SNDR and ENOB of the TDC will stay nearly unchanged regardless of the value of OSR. Therefore, a trade-off between time resolution and input range exists in this TDC. For instance, when a mm accuracy is targeted by a TOF rangefinder, the TDC needs to have 6.7 ps resolution. When the signal band of interests is fixed to 100 kHz, this MASH TDC can only offer a measurement range of 20 ns, which corresponds to a detection range up to 3 meters in distance. In order to achieve the same time resolution but a much wider input range, the SNR of the TDC has to be increased when a smaller OSR is adopted. This can be achieved by reducing the comparator delay with more power consumption, or alternatively, by applying calibration to the phase skew error, as will be discussed in Section V.

The system is also compatible with other OSR values, such as 50 and 100. Fig. 13 shows the dynamic range (DR) of the TDC, which is 68 dB. Note that, there is no apparent drop

Fig. 15. One stage of the MASH TDC with delay-line (10 delay cells) assisted calibration.

on SNDR when the input level is close to full scale, since in a TDC system, the maximum input amplitude is physically limited only by the depth of the counter, which can be easily extended to avoid any overloading of the system.

V. CHIP II: THE MASH $\Delta\Sigma$ TDC WITH DELAY-LINE ASSISTED CALIBRATION

A. Delay-Line Assisted Calibration

As explained in Section III, the main origin of noise in the MASH TDC is the phase skew introduced by the comparator delay. According to simulation results, the delay of the comparator has to be limited to 200 ps in order not to degrade the SNDR of the 1-1-1 MASH TDC, when a moderate OSR of 50 is adopted. A threshold-detection comparator at that high speed consumes huge power, and for some old technologies, it is even unrealistic to achieve that delay. Fortunately, this skew error can be calibrated by using a coarse delay-line [19].

One stage of the 1-1-1 MASH $\Delta\Sigma$ TDC with delay-line assisted calibration (TDC-CAL) is shown in Fig. 15. As one can see from it, the RS-latch is controlled by the output of the calibration unit *EN* rather than *tin*, but both have the same 'stop' edge. *lh*, the complementary signal of *tin*, is sent to the delay-line, whose detailed structure is also shown in Fig. 15. Each delay cell has a delay of 150 ps. The delay-line calibration unit becomes active only after the stop signal arrives. When the comparator's output becomes '1' during the inactive phase of the TDC, the state of each delay cell will be sampled by its connected arbiter.

For example, the stop signal arrives when *vinp1* rises above *vref*, as illustrated in Fig. 16. Therefore, the left comparator has entered its state-reversing phase. After *tskew* time, which is the resulting phase skew error, *cmp1* becomes '1'. When *lh* has been sent to the delay-line as the start signal, *cmp1* serves as the stop signal to sample the state of the delay-line. If *lh* has passed through 3 delay cells, the states of all

Fig. 16. Illustration of the delay-line assisted calibration principle.

arbiters will be "1110...0". The switch connected to the third delay cell will also be closed, which charges *sel* to '1'. *sel* will be discharged only after the next start signal has also passed through the same delay cells as the stop signal, then activate *EN*. The resulting waveform on the capacitor is shown in Fig. 16 by blue lines. In this way, the phase skew caused by the comparator delay is compensated at an accuracy of 150 ps. Since the rising edges of *lh* and *sel* have always passed through the same delay cells, the matching between those cells in the calibration unit becomes less important.

However, one problem might limit the effectiveness of the delay-line calibration method, which is the input-dependent delay of the comparator. When the input differential voltage to the comparator is very small, the comparator exhibits a much larger delay. And the relationship between the input voltage and comparator delay is nonlinear. As soon as the input differential voltage exceeds a certain level, which is 10 mV in this case, the difference in delay becomes negligible compared to the minimum detectable delay time by the calibration unit.

In order to avoid this nonlinear behavior of the comparator, an arming comparator has also been added to control each main comparator. It has a different reference voltage v_{tref} which is slightly higher than that for the main comparator (10 mV higher in this case). When the stop signal arrives, it compares the residue voltage with v_{tref} . There are three different cases: (1) the residue voltage is smaller than V_{REF} , (2) the residue voltage is larger than v_{tref} , and (3) the residue voltage is larger than V_{REF} , but smaller than v_{tref} . In case 1, the main comparator isn't in its state-reversing phase, therefore no skew error will occur. In case 2, the main comparator has an input independent delay, and that can be calibrated by the calibration unit. In case 3, the output signal of the arming comparator will disable the input stage of the main comparator. The state of the main comparator will be held as '0' even when the actual input v_{inn} or v_{inp} exceeds V_{REF} . This avoids the comparator's nonlinear-large-delay state caused by very

Fig. 17. Schematic of the comparator.

Fig. 18. Die photo of the MASH TDC with delay-line assisted calibration.

small input. Meanwhile, the introduced phase skew due to this operation is tolerable by the TDC.

B. Physical Implementation and Experiment Results

The TDC-CAL uses the same digital processing block as in chip-I, as well as the counter and time regenerator circuits. In order to better improve the TDC's temperature stability, an on-chip bandgap current reference [20] is implemented to provide 50 μA charge current for each stage. Fig. 17 shows the schematic of the main comparator in the TDC. Unlike the one been adopted in chip-I, this comparator is unnecessary to be high speed. Therefore, a low-power threshold-detection comparator with moderate speed is implemented in the TDC-CAL. The comparator has three stages. The input stage is a low-gain high-bandwidth preamplifier. It tracks the input, and makes fast decision as soon as the threshold condition is reached. The input differential voltage is then amplified and fed into the latch stage. A self-biased differential amplifier [21] is implemented as the output buffer stage. It consumes nearly zero static current, but has the ability to source and sink large currents. One comparator draws 30 μA quiescent current from the supply, and has a total delay of around 1.5 ns. A larger comparator delay is also tolerable by the design, however, this requires a larger detection range of the delay-line calibration unit, which means more circuits complexity and larger area. The arming comparator consists of a preamplifier and a clocked dynamic latch. It has the same preamplifier stage as the main comparator in order to minimize the mismatch between the two comparators.

TABLE I
COMPARISON OF STATE-OF-THE-ART TDCs WITH SIMILAR SPECIFICATIONS

	[5]JSSC08	[8]ISSCC08	[9]JSSC09	[10]JSSC09	[3]JSSC10	[12]CICC10	[13]CHIP-I	CHIP-II
Technique	TA	LPI	GRO	SAR	Vernier	Phase-domain $\Delta\Sigma$	Time-domain $\Delta\Sigma$	Time-domain $\Delta\Sigma$
Sample rate (MS/s)	10	180	50	100	15	156	50	10
Resolution (ps)	1.25	4.7	6/1 ¹	1.22	8	2.4	5.6	6
Bits	9	7	11	15	12	10	11	13
Meas. Range (ns)	0.64	0.6	12	40	32	3.2	20	100
Power (mW)	3	3.6	21	33	7.5	2.1	1.7	0.7
Core area (mm ²)	0.6	0.02	0.04	1.2	0.26	0.12	0.11	0.08
CMOS	90 nm	90 nm	0.13 μm	0.35 μm	0.13 μm	90 nm	0.13 μm	0.13 μm

¹ 6 ps resolution is achieved with a full-scale input; 1 ps resolution is achieved when a small signal is applied.

Fig. 19. Measured PSD with 18 kHz -20 dBFS input.

The TDC-CAL is implemented in 0.13 μm CMOS. The chip consumes 0.7 mW from 1.2 V supply, and occupies 0.08 mm² area (core). The photo of the die is shown in Fig. 18. The same PWM signal described in the previous measurement setup, is again used here to evaluate the performance of the TDC-CAL. The rising edge of the PWM pulse represents the start signal, where the stop signal is located at the falling edge. The carrier frequency is set to 10 MHz, which turns to a full scale peak-to-peak input range of 100 ns. Then for a bandwidth of 100 kHz, the OSR is 50. Fig. 19 shows the output spectrum of the MASH TDC with an 18 kHz 10 ns (-20 dBFS) peak-to-peak input. It shows an SNDR of 55.2 dB and 6 ps effective resolution with 100 kHz bandwidth. It can be clearly seen that, without calibration, the large phase skew caused by the comparator delay will introduce distortion and increase the baseband noise.

The TDC-CAL has also been examined under different temperatures. As illustrated in Fig. 20, with a 41 ns DC input, the total shift of the TDC's output is less than $\pm 1.25\%$ over a wide temperature range of -20 to 120 $^{\circ}\text{C}$, which shows a temperature coefficient of 176 ppm/ $^{\circ}\text{C}$ (7.2 ps/ $^{\circ}\text{C}$) without any calibration. From 25 $^{\circ}\text{C}$ to 120 $^{\circ}\text{C}$, this value is only 76 ppm/ $^{\circ}\text{C}$. During the dynamic measurement, the SNDR of the TDC doesn't drop even when the temperature rises up to 100 $^{\circ}\text{C}$.

Fig. 20. Temperature stability test with a 41 ns DC input (left axis) and an 18 kHz -20 dBFS sine input (right axis).

The performance of two MASH TDCs are summarized in Table I, and a comparison with state-of-the-art TDCs is also shown. Some report higher performances if only small (± 1 LSB) signals are applied, but in order to obtain a correct comparison only the full scale data is used. Thanks to the MASH $\Delta\Sigma$ technique, the TDCs presented in this work achieve 5.6/6 ps effective resolution when only consuming 1.7/0.7 mW for a measurement range of 20/100 ns, at the cost of a smaller bandwidth (100 kHz in this work). Similar performances are achieved for different signal levels varying from 1 LSB to near full-scale. In the MASH TDC with delay-line assisted calibration, the resolution of the TDC can be further improved to sub-ps range by increasing the OSR, at compromise of the input range. Comparing to the GRO TDC [9], which demonstrates an effective resolution of 1 ps in 1 MHz bandwidth, but consumes 21 mW for an input of 12 ns, the MASH $\Delta\Sigma$ TDC with calibration consumes only 0.7 mW for an input of 100 ns. Although lower resolution and smaller bandwidth are obtained by the MASH TDC, the low power feature and better tolerance to PVT variation made it a favorable choice for TOF measurement application.

VI. CONCLUSION

In this work, we have successfully implemented the third-order noise-shaping in time domain. It brings us a new type

of TDCs, whose resolution is not limited by the intrinsic CMOS gate delay and is not sensitive to the analog component mismatch. The first demonstrated 1-1-1 MASH $\Delta\Sigma$ TDC is implemented in 0.13 μm CMOS and achieves a time resolution of 5.6 ps, when the OSR is 250. It consumes 1.7 mW from a 1.2 V supply and exhibits an ENOB of 11 bits. The time resolution of the TDC is mainly limited by the comparator delay, which causes phase skew error when turning on/off the TDC.

Fortunately, this skew error can be calibrated by using an on-line calibration method. The MASH $\Delta\Sigma$ TDC with delay-line assisted calibration (TDC-CAL) presented in this paper digitizes the large comparator delay by using the coarse delay-line, and makes a real-time compensation to the phase skew. Owing to the power saving in the threshold-detection comparators, the TDC-CAL consumes only 0.7 mW, which is the lowest in the present state-of-the-art and achieves an ENOB of 13 bits. A wide input range of 100 ns has also been achieved. Moreover, the resolution of the TDC can be further improved by increasing the OSR, without any significant increase in power consumption.

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